THE DATASHEET OF

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Section I. Arria GX Device Data Sheet

This section provides designers with the data sheet specifications for Arria® GX devices. They contain feature definitions of the transceivers, internal architecture, configuration, and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Arria GX devices.

This section includes the following chapters:

- Chapter 1, Arria GX Device Family Overview
- Chapter 2, Arria GX Architecture
- Chapter 3, Configuration and Testing
- Chapter 4, DC and Switching Characteristics
- Chapter 5, Reference and Ordering Information

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. Arria GX Device Family Overview

AGX51001-2.0

Introduction

The Arria® GX family of devices combines 3.125 Gbps serial transceivers with reliable packaging technology and a proven logic array. Arria GX devices include 4 to 12 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES circuitry designed to support PCI-Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO protocols, along with the ability to develop proprietary, serial-based IP using its Basic mode. The transceivers build upon the success of the Stratix® II GX family. The Arria GX FPGA technology offers a 1.2-V logic array with the right level of performance and dependability needed to support these mainstream protocols.

Features

The key features of Arria GX devices include:

- Transceiver block features
  - High-speed serial transceiver channels with CDR support up to 3.125 Gbps.
  - Devices available with 4, 8, or 12 high-speed full-duplex serial transceiver channels
  - Support for the following CDR-based bus standards—PCI Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO, along with the ability to develop proprietary, serial-based IP using its Basic mode
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - 1.2- and 1.5-V pseudo current mode logic (PCML) support on transmitter output buffers
  - Receiver indicator for loss of signal (available only in PCI Express [PIPE] mode)
  - Hot socketing feature for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Dedicated circuitry that is compliant with PIPE, XAUI, Gigabit Ethernet, Serial Digital Interface (SDI), and Serial RapidIO
  - 8B/10B encoder/decoder performs 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
  - Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
  - Channel aligner compliant with XAUI

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 380 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device
  - High-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced phase-locked loops (PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 47 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory including DDR and DDR2 SDRAM, and SDR SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM})
  - Support for remote configuration updates

Table 1–1 lists Arria GX device features for FineLine BGA (FBGA) with flip chip packages.

Table 1–1. Arria GX Device Features (Part 1 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Package	484-pin, 780-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	484-pin (Flip chip)	780-pin, 1152-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	1152-pin (Flip chip)	1152-pin (Flip chip)
ALMs	8,632	13,408		20,064		24,040			36,088
Equivalent logic elements (LEs)	21,580	33,520		50,160		60,100			90,220
Transceiver channels	4	4	8	4	8	4	8	12	12
Transceiver data rate	600 Mbps to 3.125 Gbps	600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps			600 Mbps to 3.125 Gbps
Source-synchronous receive channels	31	31	31	31	31, 42	31	31	42	47

Table 1–1. Arria GX Device Features (Part 2 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Source-synchronous transmit channels	29	29	29	29	29, 42	29	29	42	45
M512 RAM blocks (32 × 18 bits)	166	197		313		326			478
M4K RAM blocks (128 × 36 bits)	118	140		242		252			400
M-RAM blocks (4096 × 144 bits)	1	1		2		2			4
Total RAM bits	1,229,184	1,348,416		2,475,072		2,528,640			4,477,824
Embedded multipliers (18 × 18)	40	56		104		128			176
DSP blocks	10	14		26		32			44
PLLs	4	4		4	4, 8	4		8	8
Maximum user I/O pins	230, 341	230	341	229	350, 514	229	350	514	538

Arria GX devices are available in space-saving FBGA packages (refer to Table 1–2). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX20C	4	31	29	230	341	—
EP1AGX35C	4	31	29	230	—	—
EP1AGX50C	4	31	29	229	—	—
EP1AGX60C	4	31	29	229	—	—
EP1AGX35D	8	31	29	—	341	—
EP1AGX50D	8	31, 42	29, 42	—	350	514

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 2 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX60D	8	31	29	—	350	—
EP1AGX60E	12	42	42	—	—	514
EP1AGX90E	12	47	45	—	—	538

Table 1–3 lists the Arria GX device package sizes.

Table 1–3. Arria GX FBGA Package Sizes

Dimension	484 Pins	780 Pins	1152 Pins
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	529	841	1225
Length × width (mm × mm)	23 × 23	29 × 29	35 × 35

Document Revision History

Table 1–4 lists the revision history for this chapter.

Table 1–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
May 2008, v1.2	Included support for SDI, SerialLite II, and XAUI.	—
June 2007, v1.1	Included GIGE information.	—
May 2007, v1.0	Initial Release	—

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Transceivers

Arria® GX devices incorporate up to 12 high-speed serial transceiver channels that build on the success of the Stratix® II GX device family. Arria GX transceivers are structured into full-duplex (transmitter and receiver) four-channel groups called transceiver blocks located on the right side of the device. You can configure the transceiver blocks to support the following serial connectivity protocols (functional modes):

- PCI Express (PIPE)
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps)
- SDI (HD, 3G)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

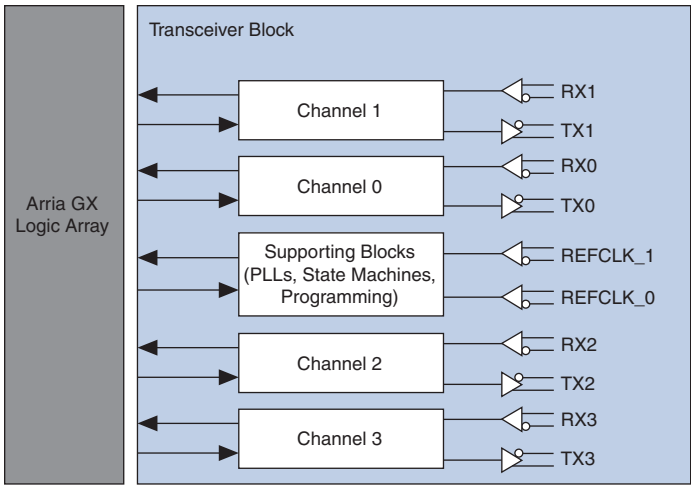
Table 2–1 lists the number of transceiver channels for each member of the Arria GX family.

Table 2–1. Arria GX Transceiver Channels

Device	Number of Transceiver Channels
EP1AGX20C	4
EP1AGX35C	4
EP1AGX35D	8
EP1AGX50C	4
EP1AGX50D	8
EP1AGX60C	4
EP1AGX60D	8
EP1AGX60E	12
EP1AGX90E	12

Figure 2–1 shows a high-level diagram of the transceiver block architecture divided into four channels.

Figure 2–1. Transceiver Block

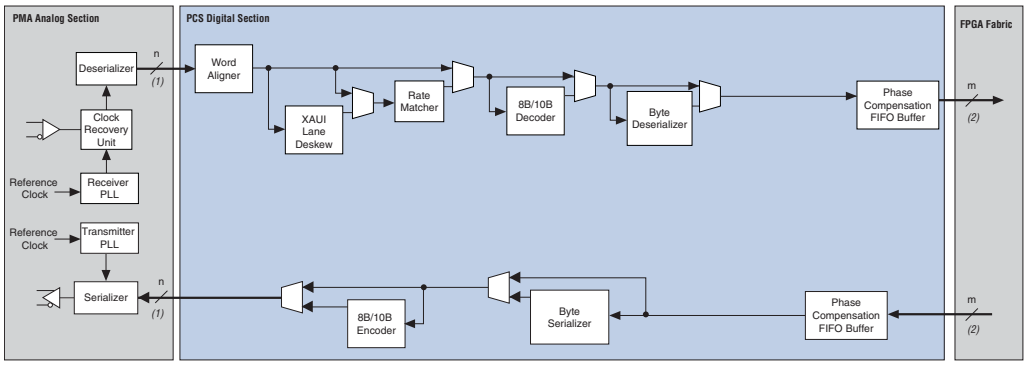


Each transceiver block has:

- Four transceiver channels with dedicated physical coding sublayer (PCS) and physical media attachment (PMA) circuitry
- One transmitter PLL that takes in a reference clock and generates high-speed serial clock depending on the functional mode
- Four receiver PLLs and clock recovery unit (CRU) to recover clock and data from the received serial data stream
- State machines and other logic to implement special features required to support each protocol

Figure 2–2 shows functional blocks that make up a transceiver channel.

Figure 2–2. Arria GX Transceiver Channel Block Diagram



Notes to Figure 2–2:

(1) "n" represents the number of bits in each word that must be serialized by the transmitter portion of the PMA. n = 8 or 10.

(2) "m" represents the number of bits in the word that passes between the FPGA logic and the PCS portion of the transceiver. m = 8, 10, 16, or 20.

Each transceiver channel is full-duplex and consists of a transmitter channel and a receiver channel.

The transmitter channel contains the following sub-blocks:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver channel contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- CRU
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Receiver phase compensation FIFO buffer

You can configure the transceiver channels to the desired functional modes using the ALT2GXB MegaCore instance in the Quartus® II MegaWizard™ Plug-in Manager for the Arria GX device family. Depending on the selected functional mode, the Quartus II software automatically configures the transceiver channels to employ a subset of the sub-blocks listed above.

Transmitter Path

This section describes the data path through the Arria GX transmitter. The sub-blocks are described in order from the PLD-transmitter parallel interface to the serial transmitter buffer.

Clock Multiplier Unit

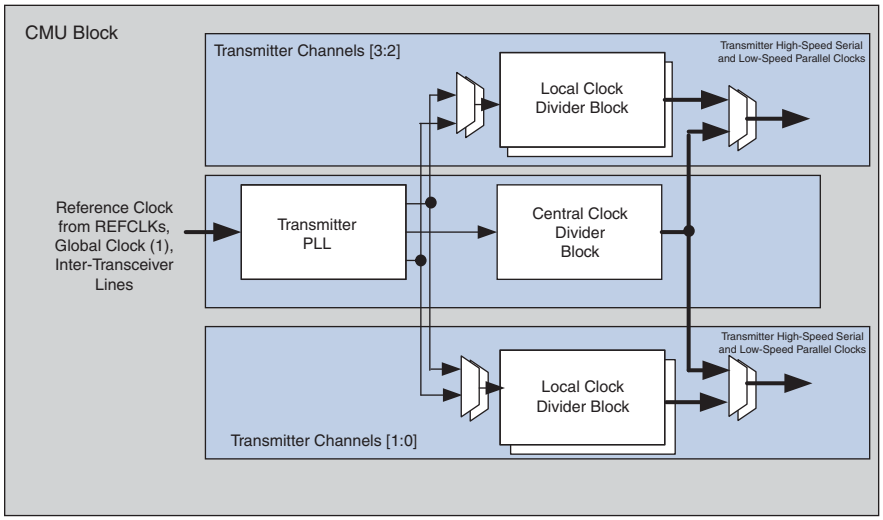
Each transceiver block has a clock multiplier unit (CMU) that takes in a reference clock and synthesizes two clocks: a high-speed serial clock to serialize the data and a low-speed parallel clock to clock the transmitter digital logic (PCS).

The CMU is further divided into three sub-blocks:

- One transmitter PLL
- One central clock divider block
- Four local clock divider blocks (one per channel)

Figure 2–3 shows the block diagram of the clock multiplier unit.

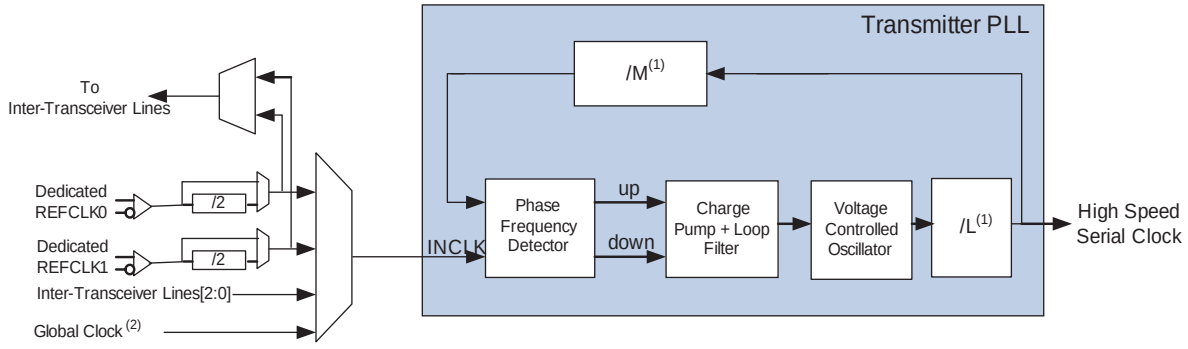
Figure 2–3. Clock Multiplier Unit



The transmitter PLL multiplies the input reference clock to generate the high-speed serial clock required to support the intended protocol. It implements a half-rate voltage controlled oscillator (VCO) that generates a clock at half the frequency of the serial data rate for which it is configured.

Figure 2–4 shows the block diagram of the transmitter PLL.

Figure 2–4. Transmitter PLL



Notes to Figure 2–4:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers (clock multiplication factors).

(2) The global clock line must be driven from an input pin only.

The reference clock input to the transmitter PLL can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)

- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Altera® recommends using the dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) to provide reference clock for the transmitter PLL.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	50 MHz to 622.08 MHz
Data rate support	600 Mbps to 3.125 Gbps
Bandwidth	Low, medium, or high

The transmitter PLL output feeds the central clock divider block and the local clock divider blocks. These clock divider blocks divide the high-speed serial clock to generate the low-speed parallel clock for the transceiver PCS logic and PLD-transceiver interface clock.

Transmitter Phase Compensation FIFO Buffer

A transmitter phase compensation FIFO is located at each transmitter channel's logic array interface. It compensates for the phase difference between the transmitter PCS clock and the local PLD clock. The transmitter phase compensation FIFO is used in all supported functional modes. The transmitter phase compensation FIFO buffer is eight words deep in PCI Express (PIPE) mode and four words deep in all other modes.

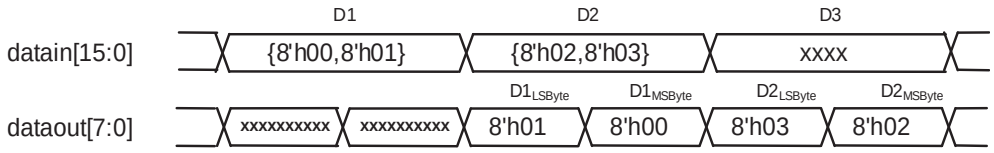
For more information about architecture and clocking, refer to the *Arria GX Transceiver Architecture* chapter.

Byte Serializer

The byte serializer takes in two-byte wide data from the transmitter phase compensation FIFO buffer and serializes it into a one-byte wide data at twice the speed. The transmit data path after the byte serializer is 8 or 10 bits. This allows clocking the PLD-transceiver interface at half the speed when compared with the transmitter PCS logic. The byte serializer is bypassed in GIGE mode. After serialization, the byte serializer transmits the least significant byte (LSByte) first and the most significant byte (MSByte) last.

Figure 2–5 shows byte serializer input and output. `datain[15:0]` is the input to the byte serializer from the transmitter phase compensation FIFO; `dataout[7:0]` is the output of the byte serializer.

Figure 2–5. Byte Serializer Operation *(Note 1)*



Note to Figure 2–5:

(1) `datain` may be 16 or 20 bits. `dataout` may be 8 or 10 bits.

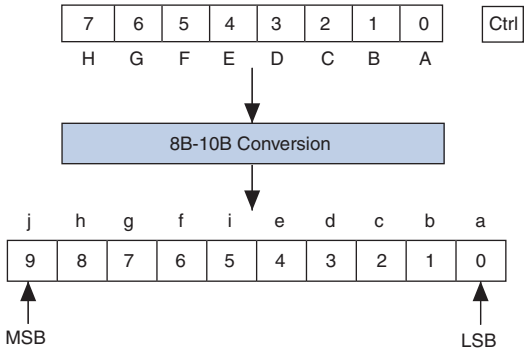
8B/10B Encoder

The 8B/10B encoder block is used in all supported functional modes. The 8B/10B encoder block takes in 8-bit data from the byte serializer or the transmitter phase compensation FIFO buffer. It generates a 10-bit code group with proper running disparity from the 8-bit character and a 1-bit control identifier (`tx_ctrlenable`). When `tx_ctrlenable` is low, the 8-bit character is encoded as data code group (`Dx.y`). When `tx_ctrlenable` is high, the 8-bit character is encoded as a control code group (`Kx.y`). The 10-bit code group is fed to the serializer. The 8B/10B encoder conforms to the IEEE 802.3 1998 edition standard.

For additional information regarding 8B/10B encoding rules, refer to the *Specifications and Additional Information* chapter.

Figure 2–6 shows the 8B/10B conversion format.

Figure 2–6. 8B/10B Encoder



During reset (`tx_digitalreset`), the running disparity and data registers are cleared and the 8B/10B encoder continously outputs a K28.5 pattern from the RD-column. After out of reset, the 8B/10B encoder starts with a negative disparity (RD-) and transmits three K28.5 code groups for synchronizing before it starts encoding the input data or control character.

Transmit State Machine

The transmit state machine operates in either PCI Express (PIPE) mode, XAUI mode, or GIGE mode, depending on the protocol used.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. The /I1/ set consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-), followed by a neutral /D5.6/. The /I2/ set consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–3 lists the code conversion.

Table 2–3. On-Chip Termination Support by I/O Banks

XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Refer to IEEE 802.3 reserved code groups	Refer to IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

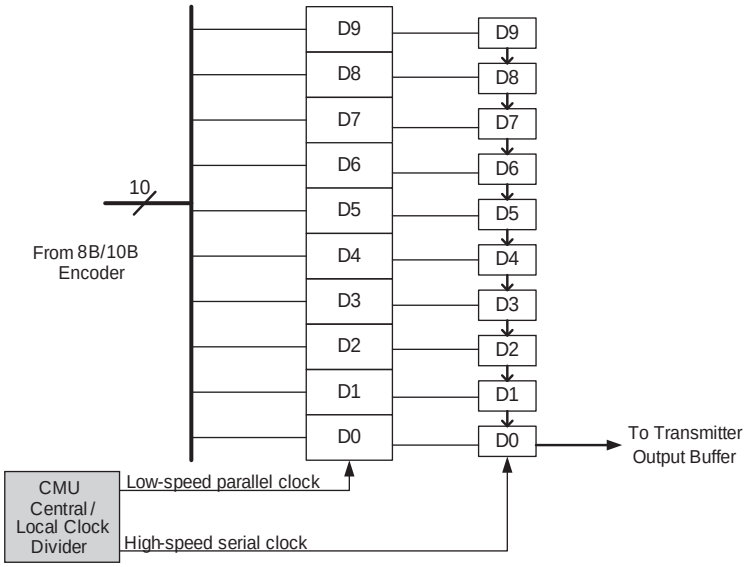
The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an ×7 + ×6 + 1 polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is automatically done by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer block clocks in 8- or 10-bit encoded data from the 8B/10B encoder using the low-speed parallel clock and clocks out serial data using the high-speed serial clock from the central or local clock divider blocks. The serializer feeds the data LSB to MSB to the transmitter output buffer.

Figure 2–7 shows the serializer block diagram.

Figure 2–7. Serializer



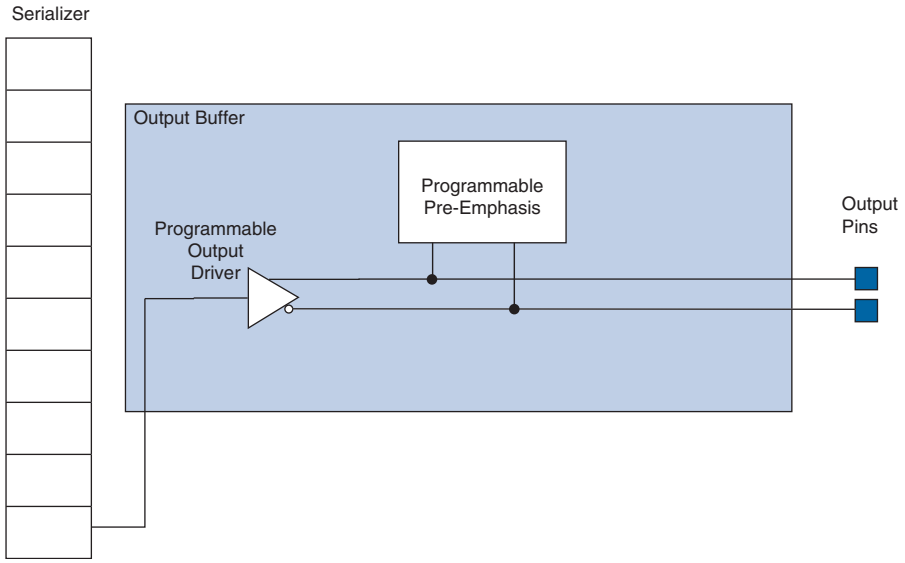
Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage (V_{CM}) of the output driver may be set to 600 or 700 mV.

For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

Figure 2–8. Output Buffer



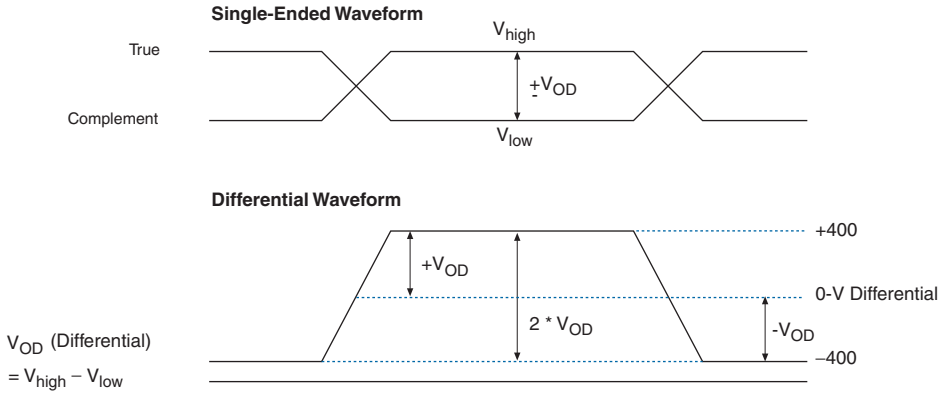
Programmable Output Driver

The programmable output driver can be set to drive out differentially from 400 to 1200 mV. The differential output voltage (V_{OD}) can be statically set by using the ALTGXB megafunction.

You can configure the output driver with 100-Ω OCT or external OCT.

Differential signaling conventions are shown in Figure 2–9. The differential amplitude represents the value of the voltage between the true and complement signals. Peak-to-peak differential voltage is defined as 2 (V_{HIGH} – V_{LOW}) = 2 single-ended voltage swing. The common mode voltage is the average of V_{HIGH} and V_{LOW}.

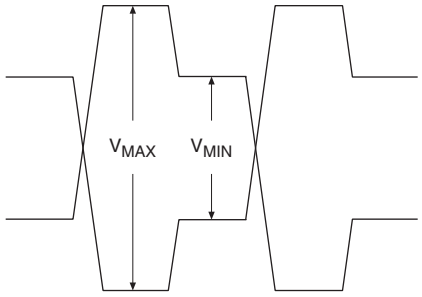
Figure 2–9. Differential Signaling



Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost high frequency components and compensate for losses in the transmission medium, as shown in Figure 2–10. Pre-emphasis is set statically using the ALTGXB megafunction.

Figure 2–10. Pre-Emphasis Signaling



$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1\right) \times 100$$

Pre-emphasis percentage is defined as $(V_{MAX}/V_{MIN} - 1) \times 100$, where V_{MAX} is the differential emphasized voltage (peak-to-peak) and V_{MIN} is the differential steady-state voltage (peak-to-peak).

PCI Express (PIPE) Receiver Detect

The Arria GX transmitter buffer has a built-in receiver detection circuit for use in PCI Express (PIPE) mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires a tri-stated transmitter buffer (in electrical idle mode).

PCI Express (PIPE) Electric Idles (or Individual Transmitter Tri-State)

The Arria GX transmitter buffer supports PCI Express (PIPE) electrical idles. This feature is only active in PCI Express (PIPE) mode. The `tx_forceelecidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express (PIPE) power-down modes and has specific usage in each mode.

Receiver Path

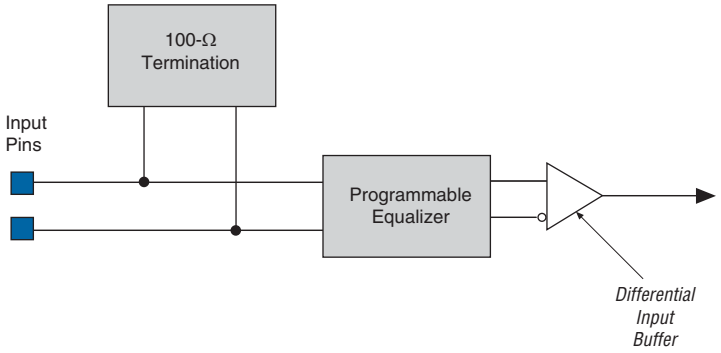
This section describes the data path through the Arria GX receiver. The sub-blocks are described in order from the receiver buffer to the PLD-receiver parallel interface.

Receiver Buffer

The Arria GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standards at rates up to 3.125 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and 1.2 V common mode voltage for DC-coupled LVDS links.

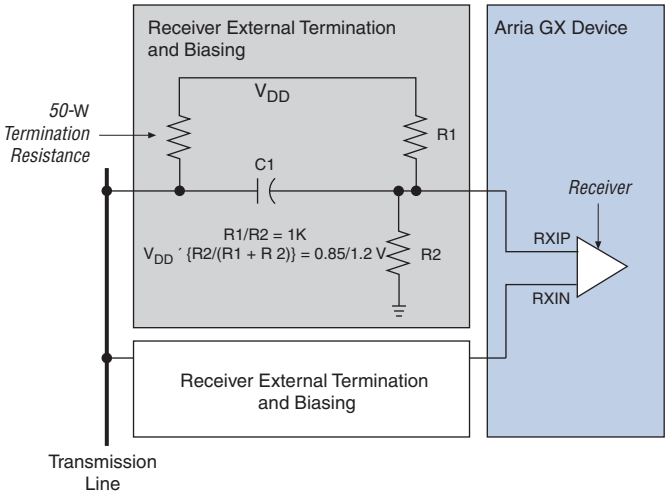
The receiver has 100-Ω on-chip differential termination (R_D OCT) for different protocols, as shown in Figure 2–11. You can disable the receiver's internal termination if external terminations and biasing are provided. The receiver and transmitter differential termination method can be set independently of each other.

Figure 2–11. Receiver Input Buffer



If a design uses external termination, the receiver must be externally terminated and biased to 0.85 V or 1.2 V. Figure 2–12 shows an example of an external termination and biasing circuit.

Figure 2–12. External Termination and Biasing Circuit



Programmable Equalizer

The Arria GX receivers provide a programmable receiver equalization feature to compensate for the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. Impedance mismatch boundaries can also cause signal degradation. Equalization in the receiver diminishes the lossy attenuation effects of the PCB at high frequencies.

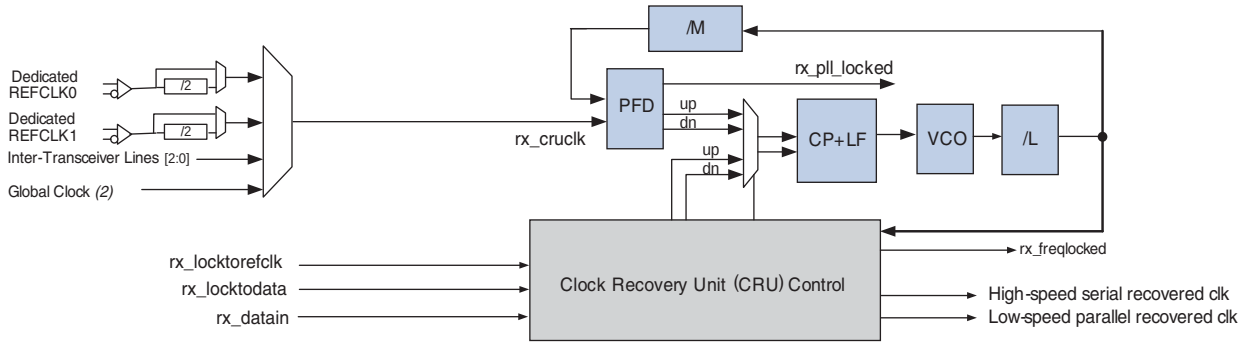
The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. The Quartus II software allows five equalization settings for Arria GX devices.

Receiver PLL and Clock Recovery Unit (CRU)

Each transceiver block has four receiver PLLs and CRU units, each of which is dedicated to a receiver channel. The receiver PLL is fed by an input reference clock. The receiver PLL, in conjunction with the CRU, generates two clocks: a high-speed serial recovered clock that clocks the deserializer and a low-speed parallel recovered clock that clocks the receiver's digital logic.

Figure 2–13 shows a block diagram of the receiver PLL and CRU circuits.

Figure 2–13. Receiver PLL and Clock Recovery Unit



Notes to Figure 2–13:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the ALTGXB MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers.

(2) The global clock line must be driven from an input pin only.

The reference clock input to the receiver PLL can be derived from:

- One of the two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

- Operates from 600 Mbps to 3.125 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to reference clock) and `rx_locktodata` (forces the receiver PLL to lock to data).

- The voltage-controlled oscillator (V_{CO}) operates at half rate.
- Programmable frequency multiplication W of 1, 4, 5, 8, 10, 16, 20, and 25. Not all settings are supported for any particular frequency.
- Two lock indication signals are provided. They are found in PFD mode (lock-to-reference clock), and PD (lock-to-data).

The CRU controls whether the receiver PLL locks to the input reference clock (lock-to-reference mode) or the incoming serial data (lock-to data mode). You can set the CRU to switch between lock-to-data and lock-to-reference modes automatically or manually. In automatic lock mode, the phase detector and dedicated parts per million (PPM) detector within each receiver channel control the switch between lock-to-data and lock-to-reference modes based on some pre-set conditions. In manual lock mode, you can control the switch manually using the `rx_locktorefclk` and `rx_locktodata` signals.

For more information, refer to the "Clock Recovery Unit" section in the *Arria GX Transceiver Protocol Support and Additional Features* chapter.

Table 2–4 lists the behavior of the CRU block with respect to the `rx_locktorefclk` and `rx_locktodata` signals.

Table 2–4. CRU Manual Lock Signals

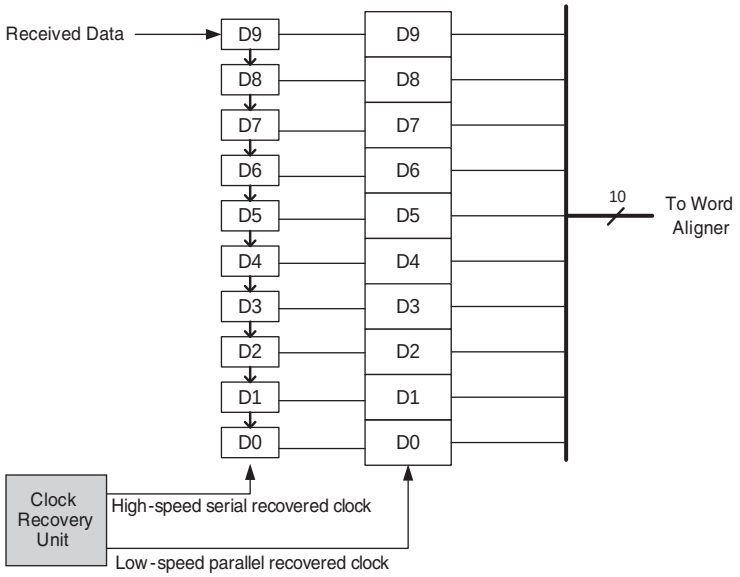
rx_locktorefclk	rx_locktodata	CRU Mode
1	0	Lock-to-reference clock
x	1	Lock-to-data
0	0	Automatic

If the `rx_locktorefclk` and `rx_locktodata` ports are not used, the default setting is automatic lock mode.

Deserializer

The deserializer block clocks in serial input data from the receiver buffer using the high-speed serial recovered clock and deserializes into 8- or 10-bit parallel data using the low-speed parallel recovered clock. The serial data is assumed to be received with LSB first, followed by MSB. It feeds the deserialized 8- or 10-bit data to the word aligner, as shown in Figure 2–14.

Figure 2–14. Deserializer *(Note 1)*



Note to Figure 2–14:

(1) This is a 10-bit deserializer. The deserializer can also convert 8 bits of data.

Word Aligner

The deserializer block creates 8- or 10-bit parallel data. The deserializer ignores protocol symbol boundaries when converting this data. Therefore, the boundaries of the transferred words are arbitrary. The word aligner aligns the incoming data based on specific byte or word boundaries. The word alignment module is clocked by the local receiver recovered clock during normal operation. All the data and programmed patterns are defined as "big-endian" (most significant word followed by least significant word). Most-significant-bit-first protocols should reverse the bit order of word align patterns programmed.

This module detects word boundaries for 8B/10B-based protocols. This module is also used to align to specific programmable patterns in PRBS7/23 test mode.

Pattern Detection

The programmable pattern detection logic can be programmed to align word boundaries using a single 7- or 10-bit pattern. The pattern detector can either do an exact match, or match the exact pattern and the complement of a given pattern. Once the programmed pattern is found, the data stream is aligned to have the pattern on the LSB portion of the data output bus.

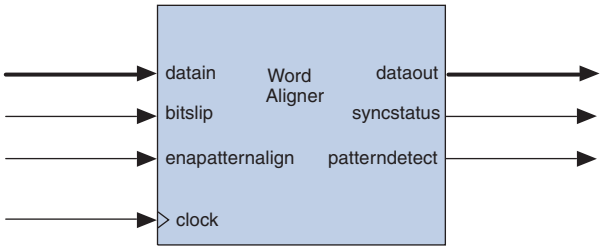
XAUI, GIGE, PCI Express (PIPE), and Serial RapidIO standards have embedded state machines for symbol boundary synchronization. These standards use K28.5 as their 10-bit programmed comma pattern. Each of these standards uses different algorithms before signaling symbol boundary acquisition to the FPGA.

Pattern detection logic searches from the LSB to the MSB. If multiple patterns are found within the search window, the pattern in the lower portion of the data stream (corresponding to the pattern received earlier) is aligned and the rest of the matching patterns are ignored.

Once a pattern is detected and the data bus is aligned, the word boundary is locked. The two detection status signals (rx_syncstatus and rx_patterndetect) indicate that an alignment is complete.

Figure 2–15 is a block diagram of the word aligner.

Figure 2–15. Word Aligner



Control and Status Signals

The rx_enapatternalign signal is the FPGA control signal that enables word alignment in non-automatic modes. The rx_enapatternalign signal is not used in automatic modes (PCI Express [PIPE], XAUI, GIGE, and Serial RapidIO).

In manual alignment mode, after the rx_enapatternalign signal is activated, the rx_syncstatus signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If rx_enapatternalign is deactivated, the rx_syncstatus signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the rx_syncstatus signal indicates the link status. If the rx_syncstatus signal is high, link synchronization is achieved. If the rx_syncstatus signal is low, link synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

For more information about manual alignment modes, refer to the *Arria GX Device Handbook*.

The rx_patterndetect signal pulses high during a new alignment and whenever the alignment pattern occurs on the current word boundary.

Programmable Run Length Violation

The word aligner supports a programmable run length violation counter. Whenever the number of the continuous '0' (or '1') exceeds a user programmable value, the rx_rlv signal goes high for a minimum pulse width of two recovered clock cycles. The maximum run values supported are 128 UI for 8-bit serialization or 160 UI for 10-bit serialization.

Running Disparity Check

The running disparity error rx_disperr and running disparity value rx_runningdisp are sent along with aligned data from the 8B/10B decoder to the FPGA. You can ignore or act on the reported running disparity value and running disparity error signals.

Bit-Slip Mode

The word aligner can operate in either pattern detection mode or in bit-slip mode.

The bit-slip mode provides the option to manually shift the word boundary through the FPGA. This feature is useful for:

- Longer synchronization patterns than the pattern detector can accommodate
- Scrambled data stream
- Input stream consisting of over-sampled data

The word aligner outputs a word boundary as it is received from the analog receiver after reset. You can examine the word and search its boundary in the FPGA. To do so, assert the `rx_bitslip` signal. The `rx_bitslip` signal should be toggled and held constant for at least two FPGA clock cycles.

For every rising edge of the `rx_bitslip` signal, the current word boundary is slipped by one bit. Every time a bit is slipped, the bit received earliest is lost. If bit slipping shifts a complete round of bus width, the word boundary is back to the original boundary.

The `rx_syncstatus` signal is not available in bit-slipping mode.

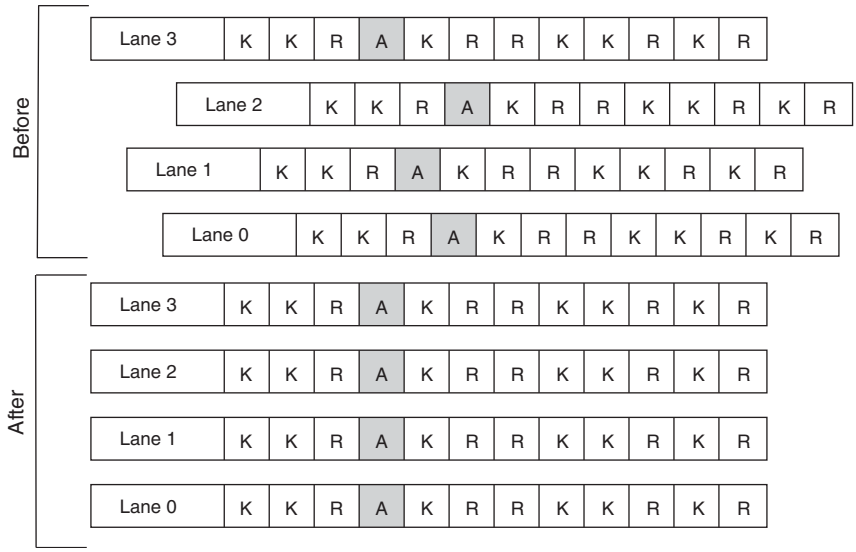
Channel Aligner

The channel aligner is available only in XAUI mode and aligns the signals of all four channels within a transceiver. The channel aligner follows the IEEE 802.3ae, clause 48 specification for channel bonding.

The channel aligner is a 16-word FIFO buffer with a state machine controlling the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel and aligns all the /A/ code groups in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the `rx_channelaligned` signal goes high, signifying that all the channels in the transceiver have been aligned. The reception of four consecutive misaligned /A/ code groups restarts the channel alignment sequence and sends the `rx_channelaligned` signal low.

Figure 2–16 shows misaligned channels before the channel aligner and the aligned channels after the channel aligner.

Figure 2–16. Before and After the Channel Aligner



Rate Matcher

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clock sources. Frequency differences in the order of a few hundred PPM can potentially corrupt the data at the receiver.

The rate matcher compensates for small clock frequency differences between the upstream transmitter and the local receiver clocks by inserting or removing skip characters from the inter packet gap (IPG) or idle streams. It inserts a skip character if the local receiver is running a faster clock than the upstream transmitter. It deletes a skip character if the local receiver is running a slower clock than the upstream transmitter. The Quartus II software automatically configures the appropriate skip character as specified in the IEEE 802.3 for GIGE mode and PCI-Express Base Specification for PCI Express (PIPE) mode. The rate matcher is bypassed in Serial RapidIO and must be implemented in the PLD logic array or external circuits depending on your system design.

Table 2–5 lists the maximum frequency difference that the rate matcher can tolerate in XAUI, PCI Express (PIPE), GIGE, and Basic functional modes.

Table 2–5. Rate Matcher PPM Tolerance

Function Mode	PPM
XAUI	± 100
PCI Express (PIPE)	± 300
GIGE	± 100
Basic	± 300

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express (PIPE) Mode Rate Matcher

In PCI Express (PIPE) mode, the rate matcher can compensate up to ± 300 PPM (600 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic looks for skip ordered sets (SOS), which contains a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher logic deletes or inserts /K28.0/ skip characters as necessary from/to the rate matcher FIFO.

The rate matcher in PCI Express (PIPE) mode has a FIFO buffer overflow and underflow protection. In the event of a FIFO buffer overflow, the rate matcher deletes any data after detecting the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO buffer is not empty. These measures ensure that the FIFO buffer can gracefully exit the overflow and underflow condition without requiring a FIFO reset. The rate matcher FIFO overflow and underflow condition is indicated on the `pipestatus` port.

You can bypass the rate matcher in PCI Express (PIPE) mode if you have a synchronous system where the upstream transmitter and local receiver derive their reference clocks from the same source.

GIGE Mode Rate Matcher

In GIGE mode, the rate matcher can compensate up to ± 100 PPM (200 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic inserts or deletes /I2/ idle ordered sets to/from the rate matcher FIFO during the inter-frame or inter-packet gap (IFG or IPG). /I2/ is selected as the rate matching ordered set because it maintains the running disparity, unlike /I1/ that alters the running disparity. Because the /I2/ ordered-set contains two 10-bit code groups (/K28.5/, /D16.2/), 20 bits are inserted or deleted at a time for rate matching.

The rate matcher logic has the capability to insert or delete /C1/ or /C2/ configuration ordered sets when 'GIGE Enhanced' mode is chosen as the sub-protocol in the MegaWizard Plug-In Manager.

If the frequency PPM difference between the upstream transmitter and the local receiver is high, or if the packet size is too large, the rate matcher FIFO buffer can face an overflow or underflow situation.

Basic Mode

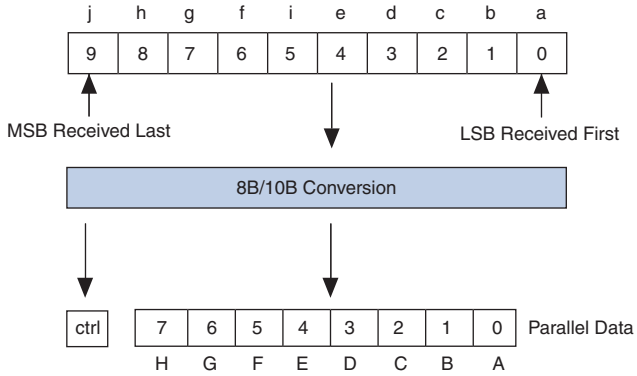
In basic mode, you can program the skip and control pattern for rate matching. There is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five.

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Byte Deserializer

Byte deserializer takes in one-byte wide data from the 8B/10B decoder and deserializes it into a two-byte wide data at half the speed. This allows clocking the PLD-receiver interface at half the speed as compared to the receiver PCS logic. The byte deserializer is bypassed in GIGE mode.

The byte ordering at the receiver output might be different than what was transmitted. This is a non-deterministic swap, because it depends on PLL lock times and link delay. If required, you must implement byte ordering logic in the PLD to correct this situation.

For more information about byte serializer, refer to the *Arria GX Transceiver Architecture* chapter.

Receiver Phase Compensation FIFO Buffer

A receiver phase compensation FIFO buffer is located at each receiver channel's logic array interface. It compensates for the phase difference between the receiver PCS clock and the local PLD receiver clock. The receiver phase compensation FIFO is used in all supported functional modes. The receiver phase compensation FIFO buffer is eight words deep in PCI Express (PIPE) mode and four words deep in all other modes.

For more information about architecture and clocking, refer to the *Arria GX Transceiver Architecture* chapter.

Loopback Modes

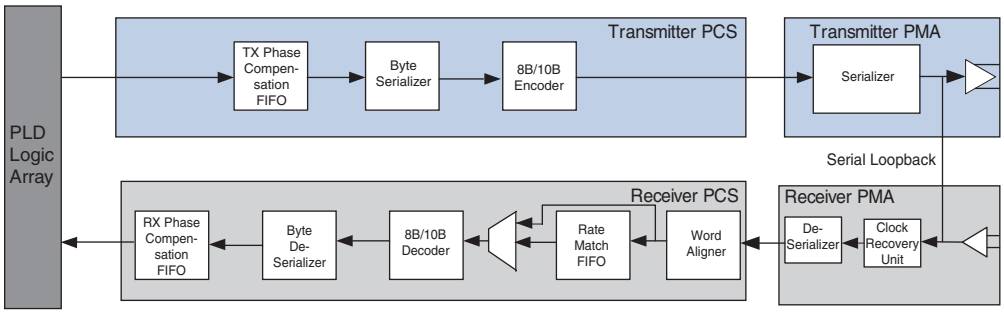
Arria GX transceivers support the following loopback configurations for diagnostic purposes:

- Serial loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express (PIPE) reverse parallel loopback (available only in [PIPE] mode)

Serial Loopback

Figure 2–18 shows the transceiver data path in serial loopback.

Figure 2–18. Transceiver Data Path in Serial Loopback



In GIGE and Serial RapidIO modes, you can dynamically put each transceiver channel individually in serial loopback by controlling the `rx_seriallpbken` port. A high on the `rx_seriallpbken` port puts the transceiver into serial loopback and a low takes the transceiver out of serial loopback.

As seen in Figure 2–18, the serial data output from the transmitter serializer is looped back to the receiver CRU in serial loopback. The transmitter data path from the PLD interface to the serializer in serial loopback is the same as in non-loopback mode. The receiver data path from the clock recovery unit to the PLD interface in serial loopback is the same as in non-loopback mode. Because the entire transceiver data path is available in serial loopback, this option is often used to diagnose the data path as a probable cause of link errors.

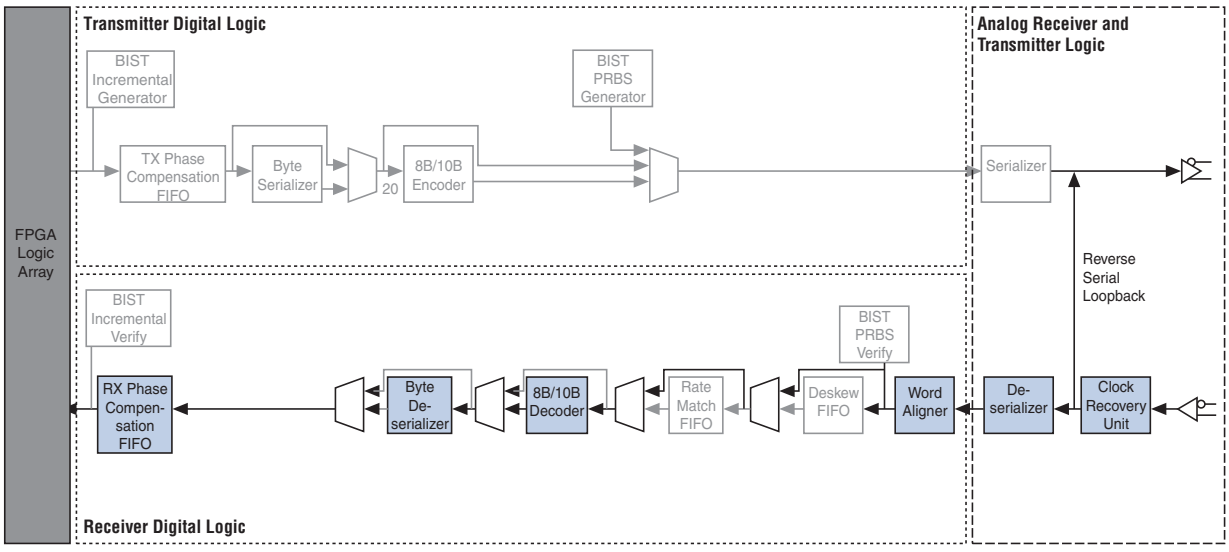
When serial loopback is enabled, the transmitter output buffer is still active and drives the serial data out on the `tx_dataout` port.

Reverse Serial Loopback

Reverse serial loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, passes through the CRU unit and the retimed serial data is looped back, and is transmitted though the high-speed differential transmitter output buffer.

Figure 2–19 shows the data path in reverse serial loopback mode.

Figure 2–19. Arria GX Block in Reverse Serial Loopback Mode

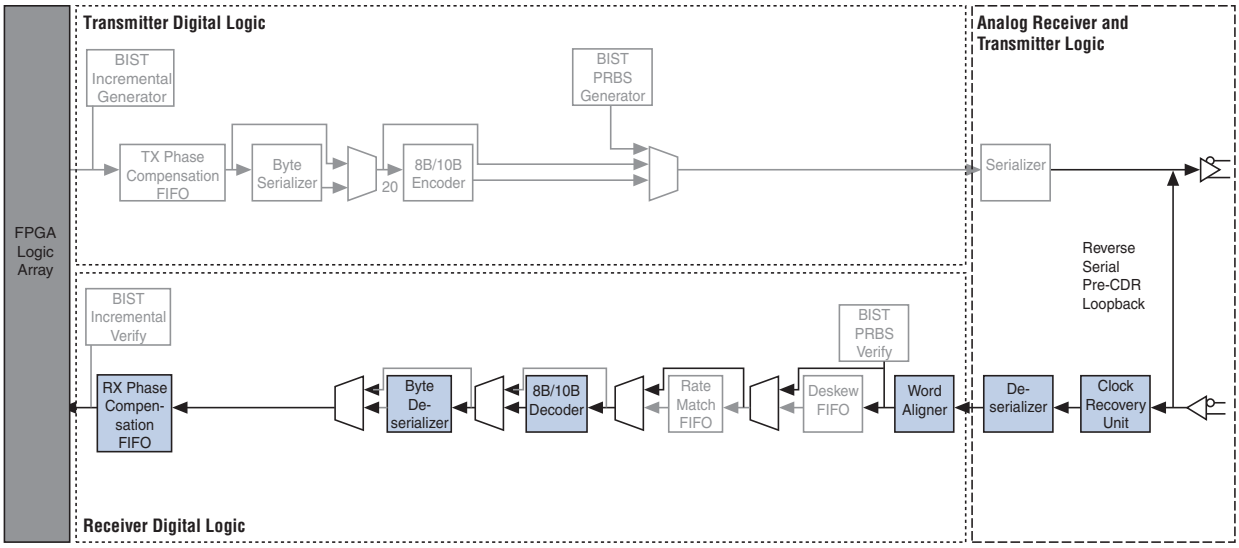


Reverse Serial Pre-CDR Loopback

Reverse serial pre-CDR loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, loops back before the CRU unit, and is transmitted though the high-speed differential transmitter output buffer. It is for test or verification use only to verify the signal being received after the gain and equalization improvements of the input buffer. The signal at the output is not exactly what is received because the signal goes through the output buffer and the V_{OD} is changed to the V_{OD} setting level. Pre-emphasis settings have no effect.

Figure 2–20 shows the Arria GX block in reverse serial pre-CDR loopback mode.

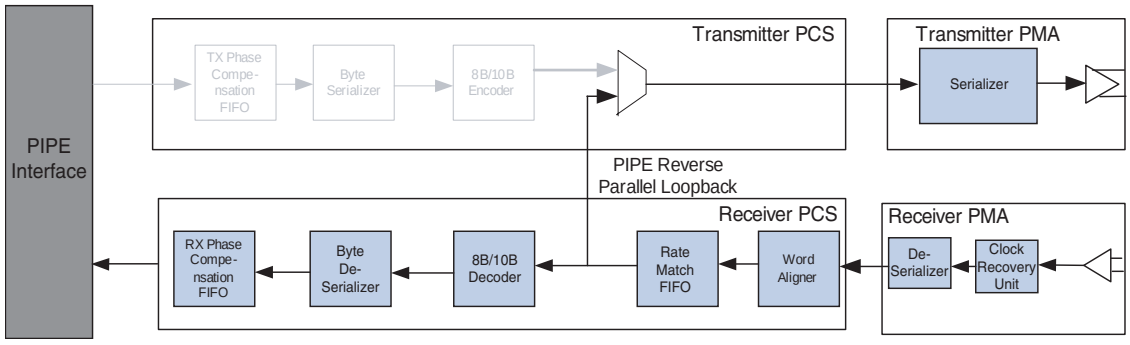
Figure 2–20. Arria GX Block in Reverse Serial Pre-CDR Loopback Mode



PCI Express (PIPE) Reverse Parallel Loopback

Figure 2–21 shows the data path for PCI Express (PIPE) reverse parallel loopback. The reverse parallel loopback configuration is compliant with the PCI Express (PIPE) specification and is available only on PCI Express (PIPE) mode.

Figure 2–21. PCI Express (PIPE) Reverse Parallel Loopback



You can dynamically put the PCI Express (PIPE) mode transceiver in reverse parallel loopback by controlling the `tx_detectrxloopback` port instantiated in the MegaWizard Plug-In Manager. A high on the `tx_detectrxloopback` port in P0 power state puts the transceiver in reverse parallel loopback. A high on the `tx_detectrxloopback` port in any other power state does not put the transceiver in reverse parallel loopback.

As seen in Figure 2–21, the serial data received on the `rx_datain` port in reverse parallel loopback goes through the CRU, deserializer, word aligner, and the rate matcher blocks. The parallel data at the output of the receiver rate matcher block is looped back to the input of the transmitter serializer block. The serializer converts the parallel data to serial data and feeds it to the transmitter output buffer that drives the data out on the `tx_dataout` port. The data at the output of the rate matcher also goes through the 8B/10B decoder, byte deserializer, and receiver phase compensation FIFO before being fed to the PLD on the `rx_dataout` port.

Reset and Powerdown

Arria GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed.

The following three reset signals are available per transceiver channel and can be used to individually reset the digital and analog portions within each channel:

- `tx_digitalreset`
- `rx_analogreset`
- `rx_digitalreset`

The following two powerdown signals are available per transceiver block and can be used to shut down an entire transceiver block that is not being used:

- `gxb_powerdown`
- `gxb_enable`

Table 2–6 lists the reset signals available in Arria GX devices and the transceiver circuitry affected by each signal.

Table 2–6. Reset Signal Map to Arria GX Blocks

Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset	—	—	—	—	—	—	—	—	✓	—	✓	✓	✓	—	✓	✓	—
rx_analogreset	—	—	—	—	—	—	—	✓	—	—	—	—	—	✓	—	—	✓
tx_digitalreset	✓	✓	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓

Calibration Block

Arria GX devices use the calibration block to calibrate OCT for the PLLs, and their associated output buffers, and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the OCT resistors on Arria GX devices. You can power down the calibration block. However, powering down the calibration block during operations can yield transmit and receive data errors.

Transceiver Clocking

This section describes the clock distribution in an Arria GX transceiver channel and the PLD clock resource utilization by the transceiver blocks.

Transceiver Channel Clock Distribution

Each transceiver block has one transmitter PLL and four receiver PLLs.

The transmitter PLL multiplies the input reference clock to generate a high-speed serial clock at a frequency that is half the data rate of the configured functional mode. This high-speed serial clock (or its divide-by-two version if the functional mode uses byte serializer) is fed to the CMU clock divider block. Depending on the configured functional mode, the CMU clock divider block divides the high-speed serial clock to generate the low-speed parallel clock that clocks the transceiver PCS logic in the associated channel. The low-speed parallel clock is also forwarded to the PLD logic array on the `tx_clkout` or `coreclkout` ports.

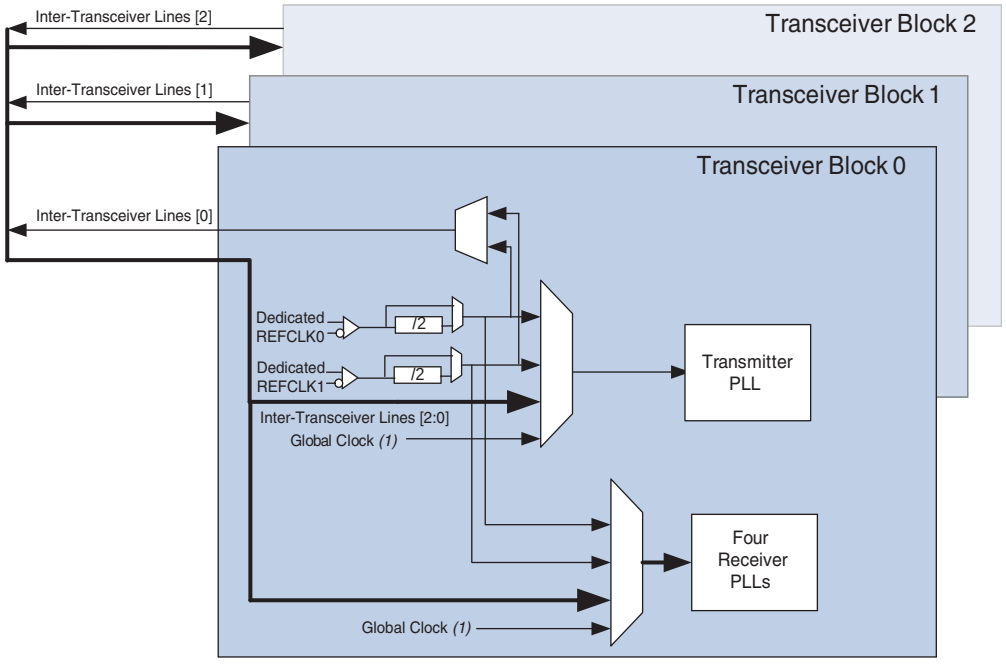
The receiver PLL in each channel is also fed by an input reference clock. The receiver PLL along with the clock recovery unit generates a high-speed serial recovered clock and a low-speed parallel recovered clock. The low-speed parallel recovered clock feeds the receiver PCS logic until the rate matcher. The CMU low-speed parallel clock clocks the rest of the logic from the rate matcher until the receiver phase compensation FIFO. In modes that do not use a rate matcher, the receiver PCS logic is clocked by the recovered clock until the receiver phase compensation FIFO.

The input reference clock to the transmitter and receiver PLLs can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Figure 2–22 shows the input reference clock sources for the transmitter and receiver PLL.

Figure 2–22. Input Reference Clock Sources



For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices

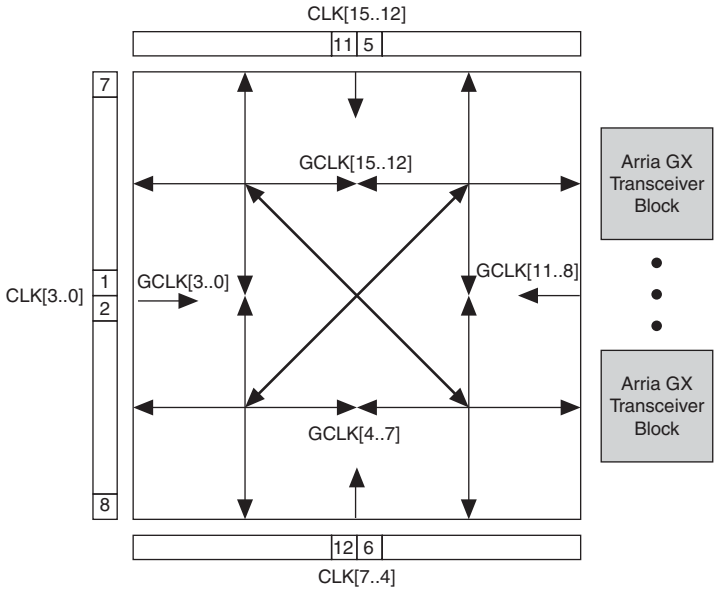
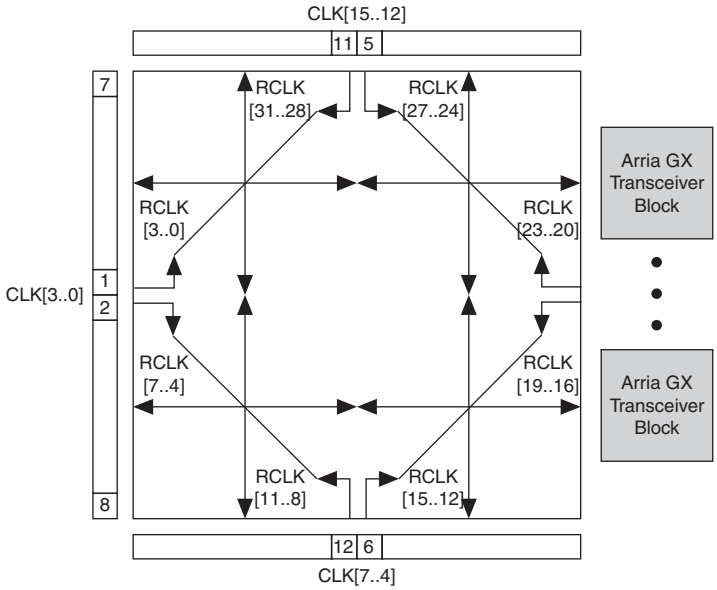


Figure 2–24. Regional Clock Resources in Arria GX Devices



For the RCLK or GCLK network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–7 and Table 2–8 list the number of LRIO resources available for Arria GX devices with different numbers of transceiver blocks.

Table 2–7. Available Clocking Connections for Transceivers in EP1AGX35D, EP1AGX50D, and EP1AGX60D

Source	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—
Region1 8 LRIO clock	✓	RCLK 12-19	—	✓

Table 2–8. Available Clocking Connections for Transceivers in EP1AGX60E and EP1AGX90E

Source	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O	Bank15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—	—
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	—
Region2 8 LRIO clock	✓	RCLK 12-19	—	✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19	—	—	✓

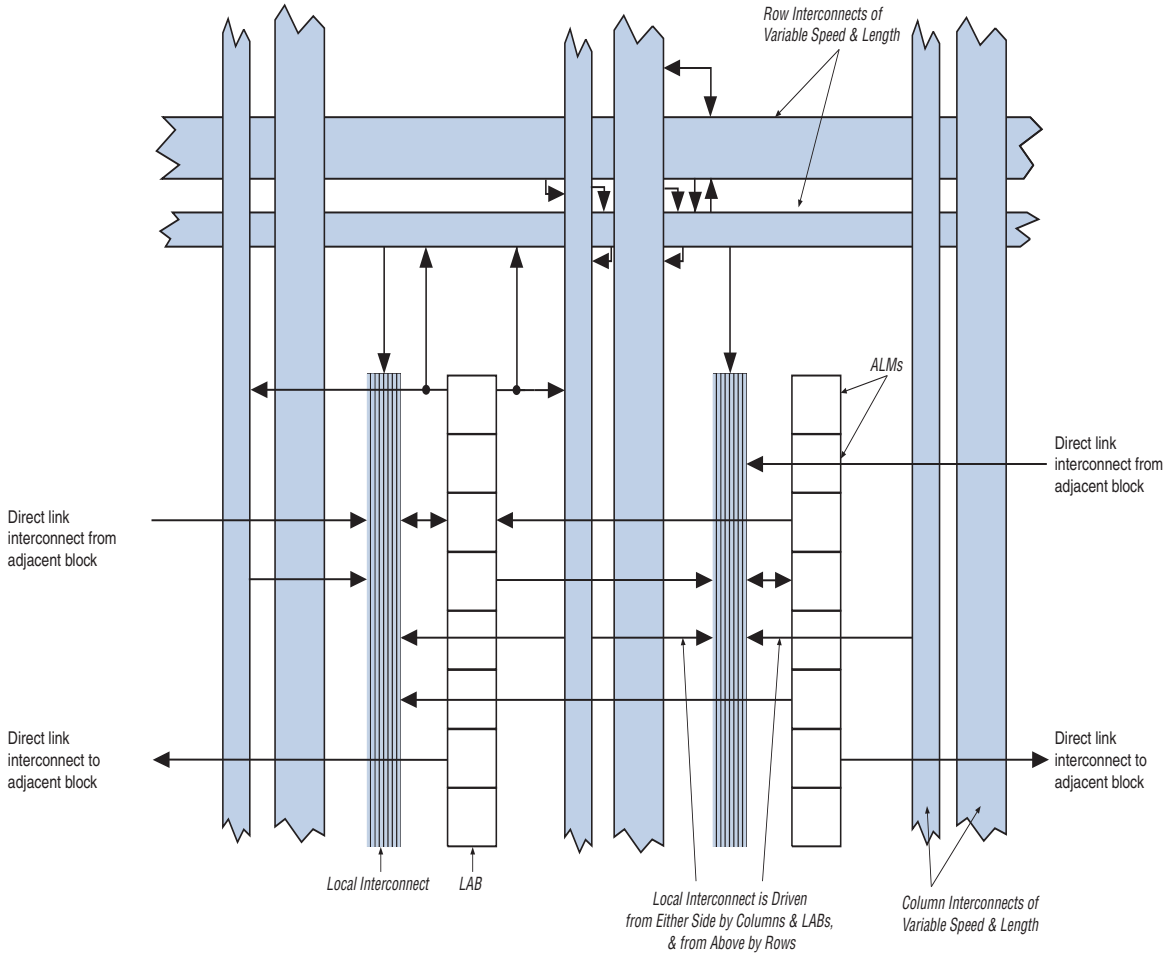
Logic Array Blocks

Each logic array block (LAB) consists of eight adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnects, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in a LAB. The Quartus II Compiler places associated logic in a LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Table 2–9 lists Arria GX device resources. Figure 2–25 shows the Arria GX LAB structure.

Table 2–9. Arria GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks
EP1AGX20	166	118	1	10
EP1AGX35	197	140	1	14
EP1AGX50	313	242	2	26
EP1AGX60	326	252	2	32
EP1AGX90	478	400	4	44

Figure 2–25. Arria GX LAB Structure

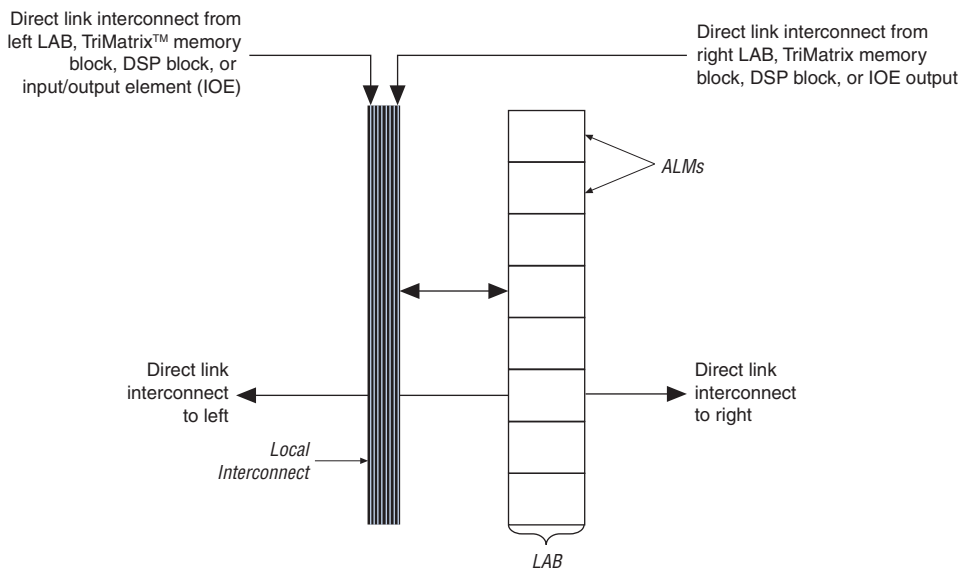


LAB Interconnects

The LAB local interconnect can drive all eight ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or digital signal processing (DSP) blocks from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects.

Figure 2–26 shows the direct link connection.

Figure 2–26. Direct Link Connection



LAB Control Signals

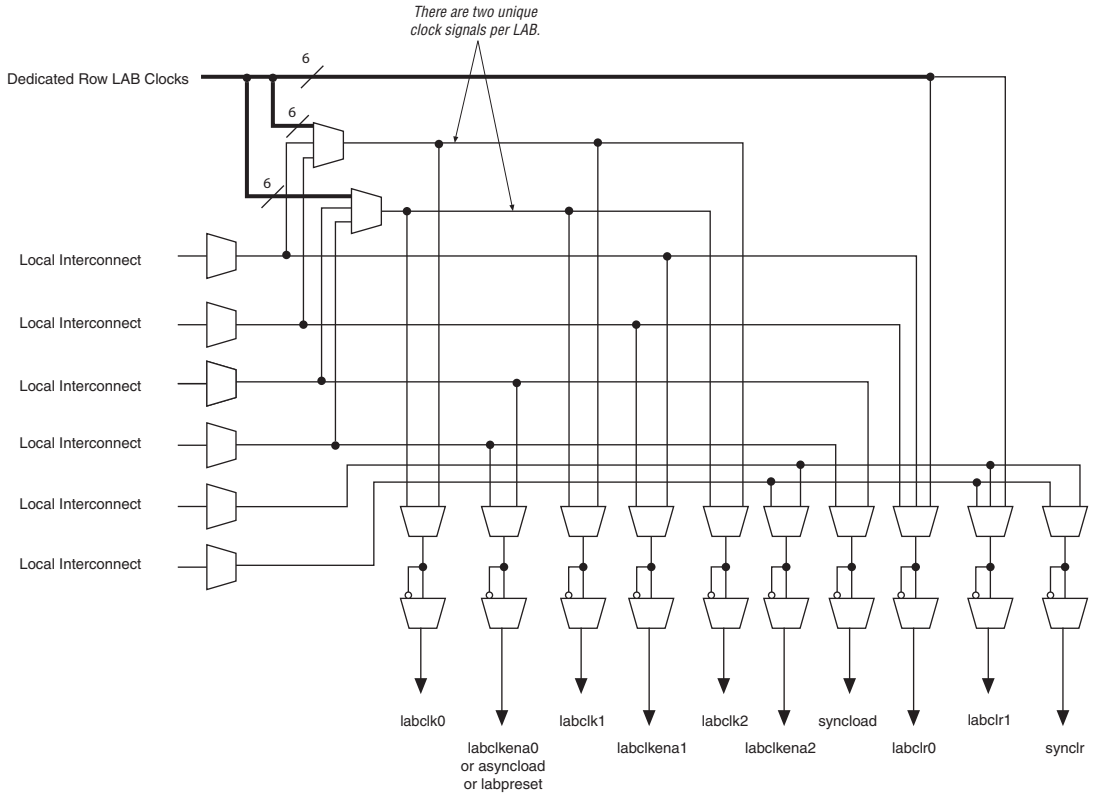
Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset or load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–27. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–27 shows the LAB control signal generation circuit.

Figure 2–27. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Arria GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–28 shows a high-level block diagram of the Arria GX ALM while Figure 2–29 shows a detailed view of all the connections in the ALM.

Figure 2–28. High-Level Block Diagram of the Arria GX ALM

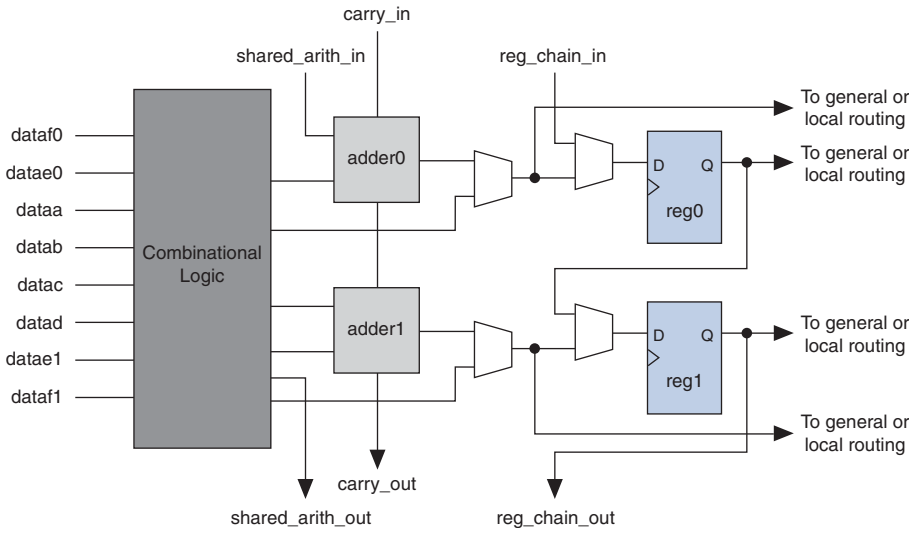
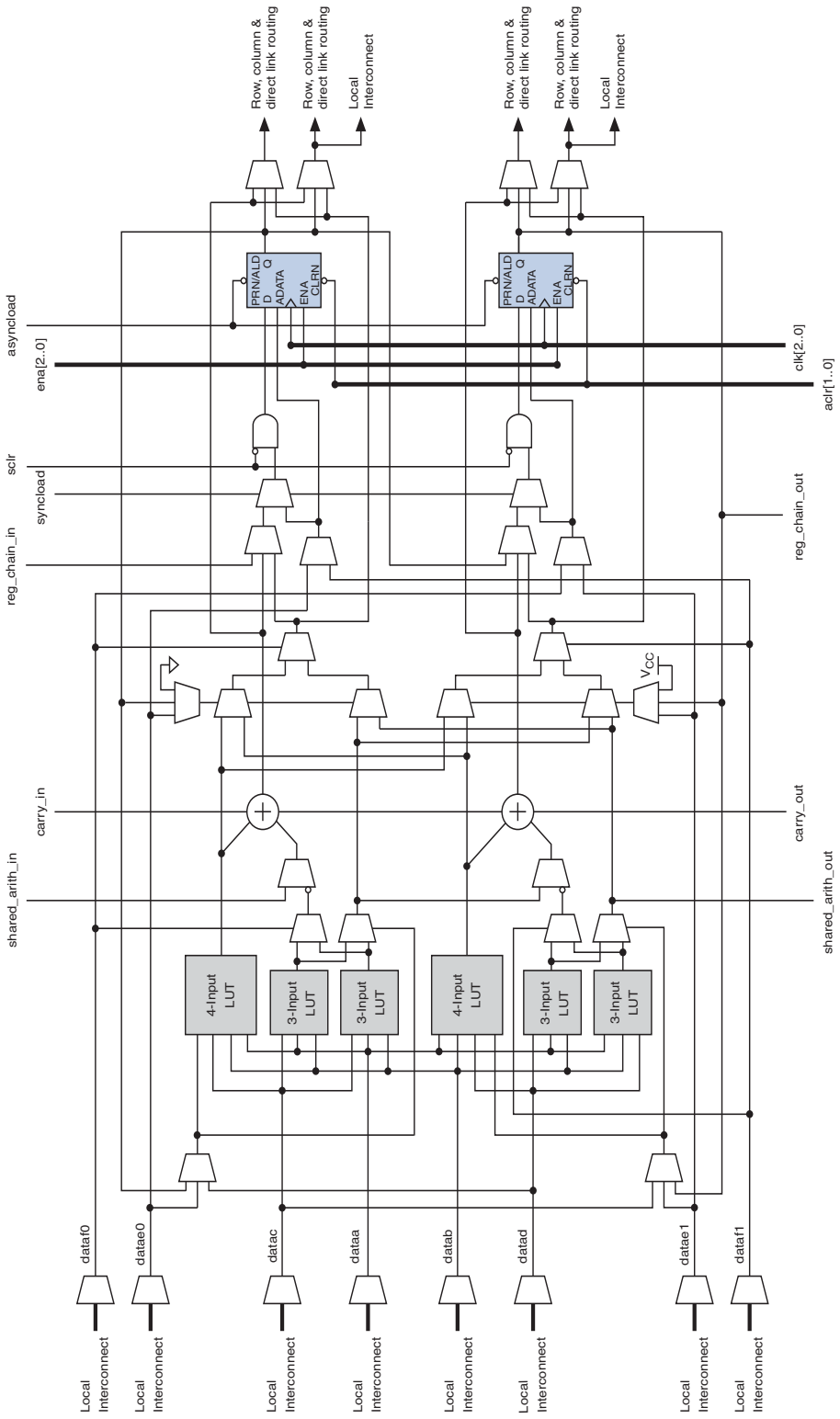


Figure 2–29. Arria GX ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs.

Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (refer to Figure 2–29). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections. One of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This feature provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

ALM Operating Modes

The Arria GX ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

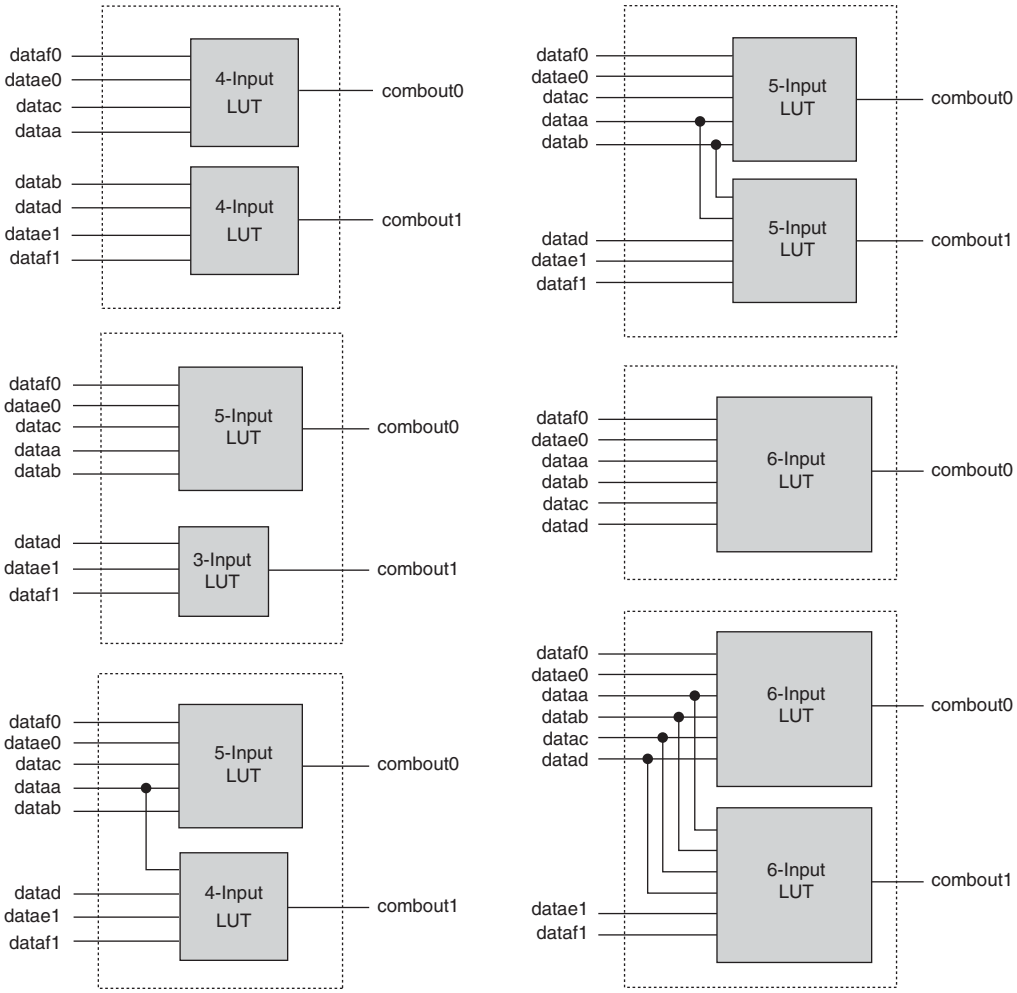
Each mode uses ALM resources differently. Each mode has 11 available inputs to the ALM (refer to Figure 2–28)—the eight data inputs from the LAB local interconnect; carry-in from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. For more information about LAB-wide control signals, refer to "LAB Control Signals" on page 2–30.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. Normal mode allows two functions to be implemented in one Arria GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–30 shows the supported LUT combinations in normal mode.

Figure 2–30. ALM in Normal Mode *(Note 1)*



Note to Figure 2–30:

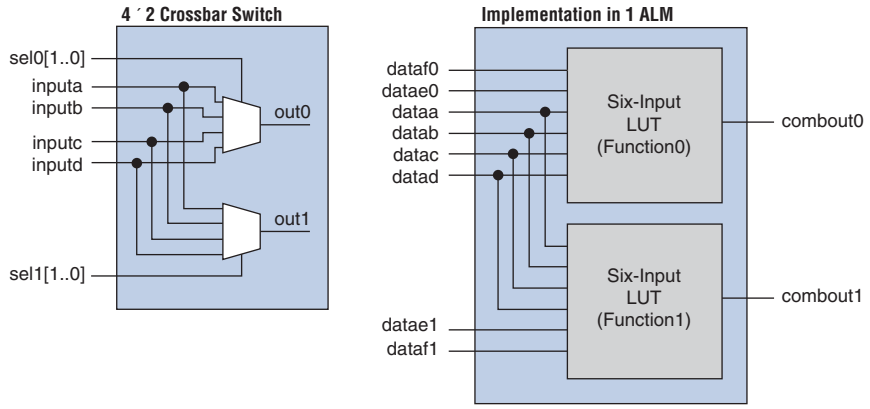
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, and so on.

Normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Arria GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

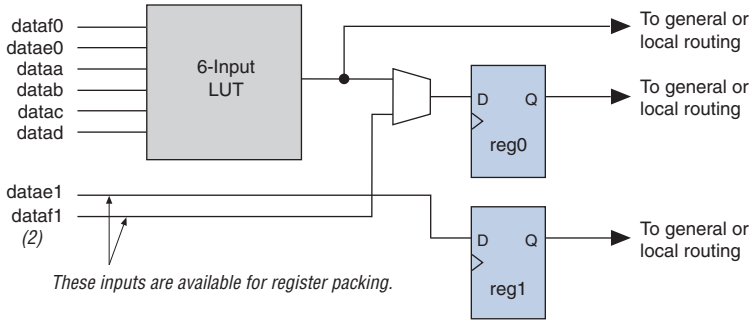
To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–31. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–31. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that can be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically uses the full potential of the Arria GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are used, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (refer to Figure 2–32). If datae1 and dataf1 are used, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

Figure 2–32. Six-Input Function in Normal Mode *Note (1), (2)*



Notes to Figure 2–32:

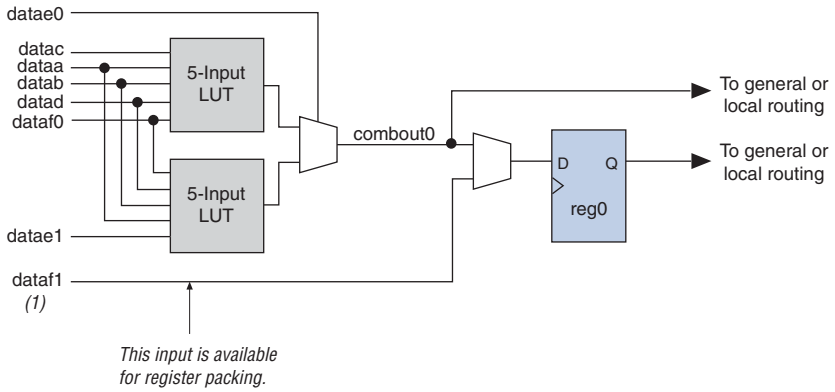
(1) If `datae1` and `dataf1` are used as inputs to the six-input function, `datae0` and `dataf0` are available for register packing.

(2) The `dataf1` input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

Extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–33 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing. Functions that fit into the template shown in Figure 2–33 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

Figure 2–33. Template for Supported Seven-Input Functions in Extended LUT Mode



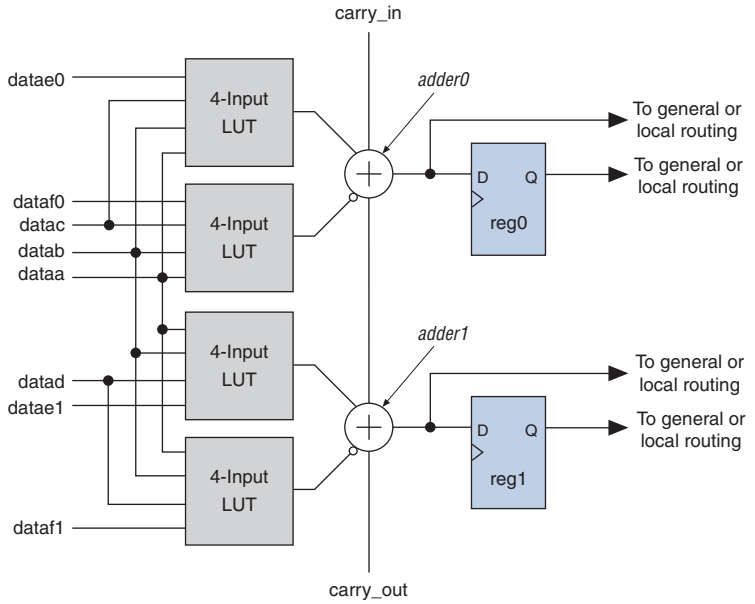
Note to Figure 2–33:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

Arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of 2 four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–34, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–34. ALM in Arithmetic Mode



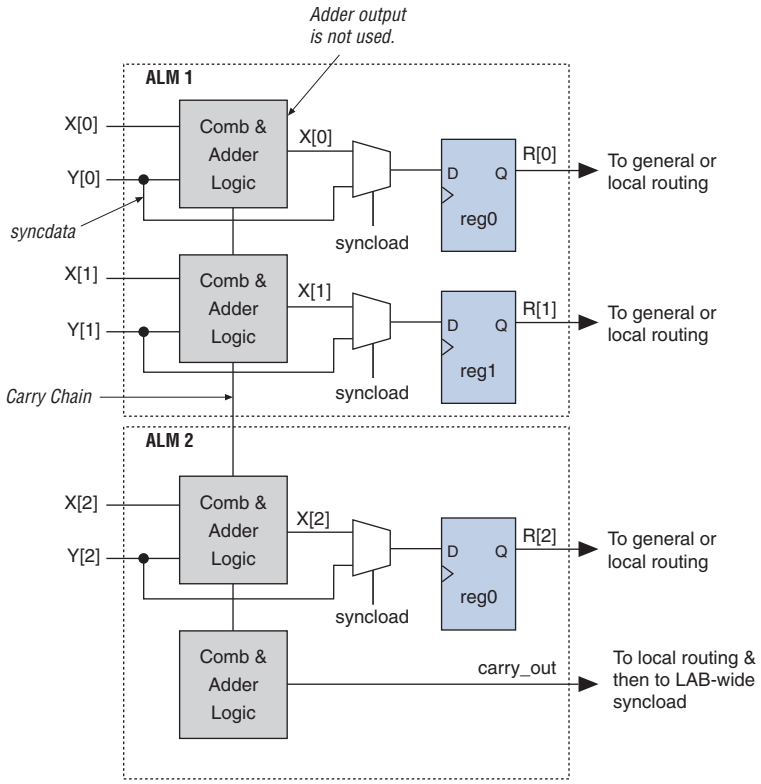
While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–35. The equation for this example is:

Equation 2–1.

$$R = (X < Y) ? Y : X$$

To implement this function, the adder is used to subtract 'Y' from 'X.' If 'X' is less than 'Y,' the `carry_out` signal is '1.' The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data 'Y' drives the `syncdata` inputs to the registers. If 'X' is greater than or equal to 'Y,' the `syncload` signal is deasserted and 'X' drives the data port of the registers.

Figure 2–35. Conditional Operation Example



Arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, and synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals can be used for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

Carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

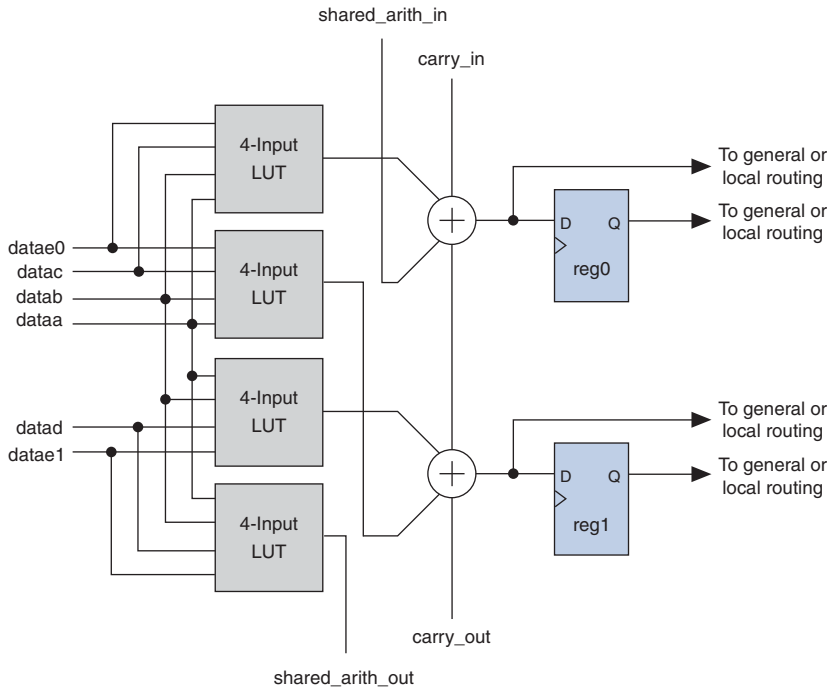
The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only use either the top half or bottom half of the LAB before connecting to the next LAB.

The other half of the ALMs in the LAB is available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carries into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carries into the bottom half of the ALMs in the next LAB within the column. Every other column of the LABs are top-half bypassable, while the other LAB columns are bottom-half bypassable. For more information about carry chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) using a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–36 shows the ALM in shared arithmetic mode.

Figure 2–36. ALM in Shared Arithmetic Mode

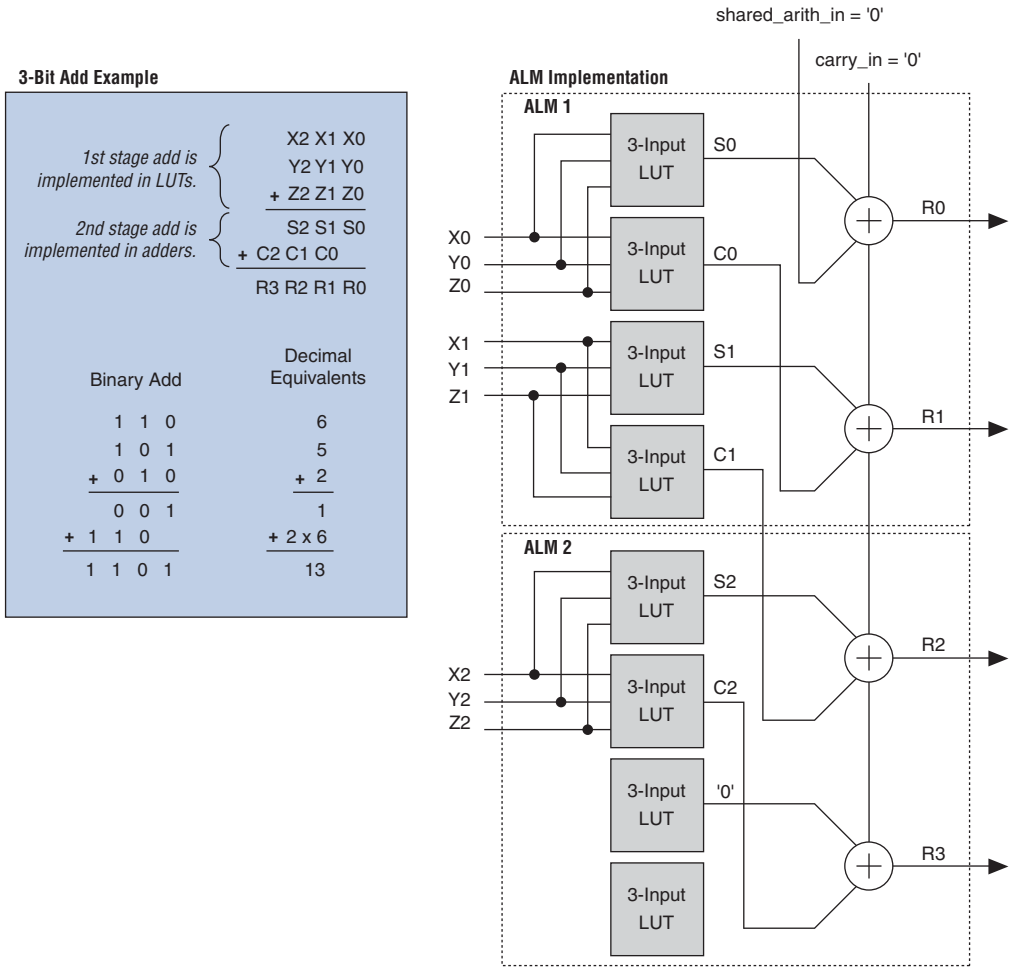


Note to Figure 2–36:

(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. For example, the summation of partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–37. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using LUTs, while the result (`R[2..0]`) is computed using dedicated adders.

Figure 2–37. Example of a 3-Bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

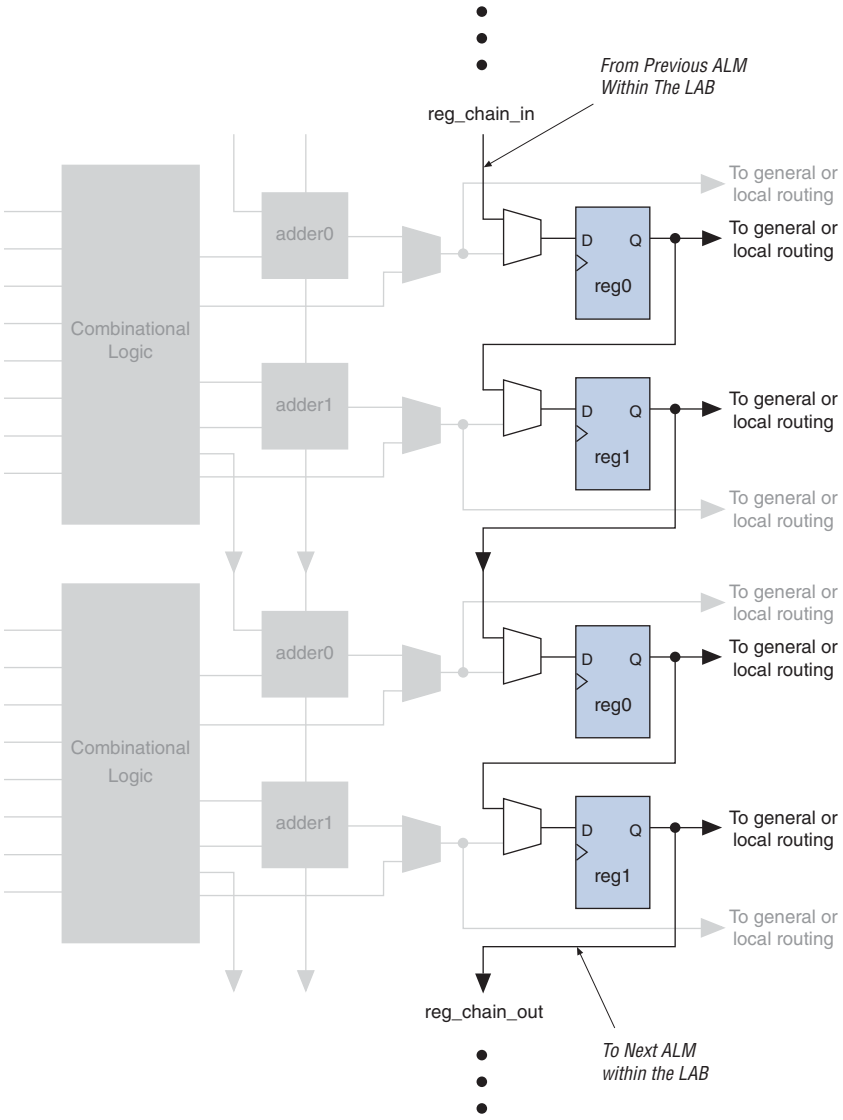
In addition to dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add, which significantly reduces the resources necessary to implement large adder trees or correlator functions. Shared arithmetic chains can begin in either the first or fifth ALM in a LAB. The Quartus II Compiler automatically links LABs to create shared arithmetic chains longer than 16 (eight ALMs in arithmetic or shared arithmetic mode). For enhanced fitting, a long shared arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column. Similar to carry chains, shared arithmetic

chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable. For more information about shared arithmetic chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

Register Chain

In addition to the general routing outputs, the ALMs in a LAB have register chain outputs. Register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (refer to Figure 2–38). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. For more information about register chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

Figure 2–38. Register Chain within a LAB *(Note 1)*



Note to Figure 2–38:

(1) The combinational or adder logic can be used to implement an unrelated, unregistered function.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Arria GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Arria GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In Arria GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

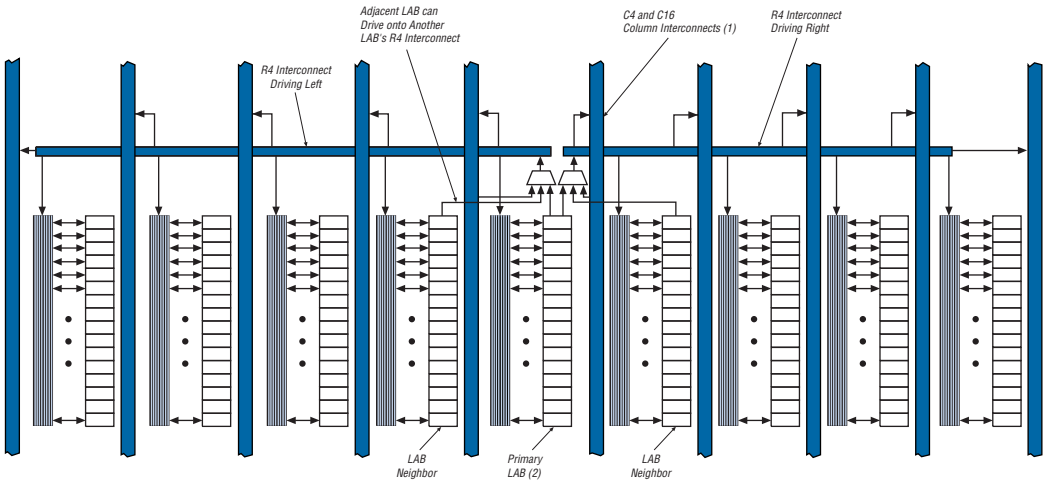
- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–39 shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–39. R4 Interconnect Connections *(Note 1)*, *(2)*, *(3)*



Notes to Figure 2–39:

(1) C4 and C16 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

(3) The LABs in Figure 2–39 show the 16 possible logical outputs per LAB.

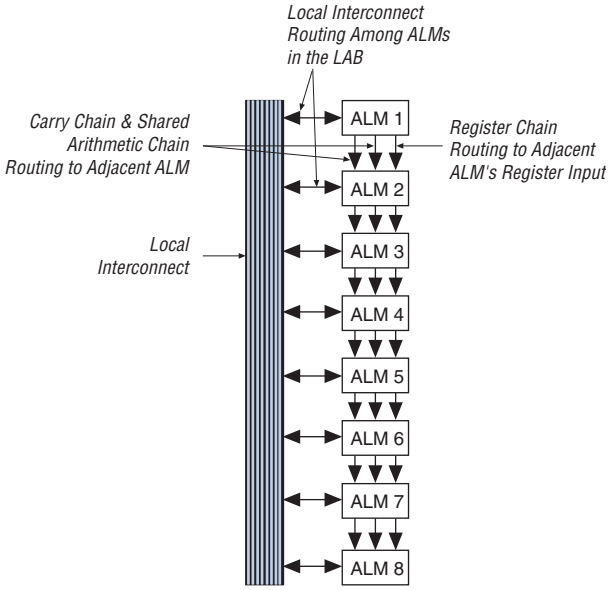
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

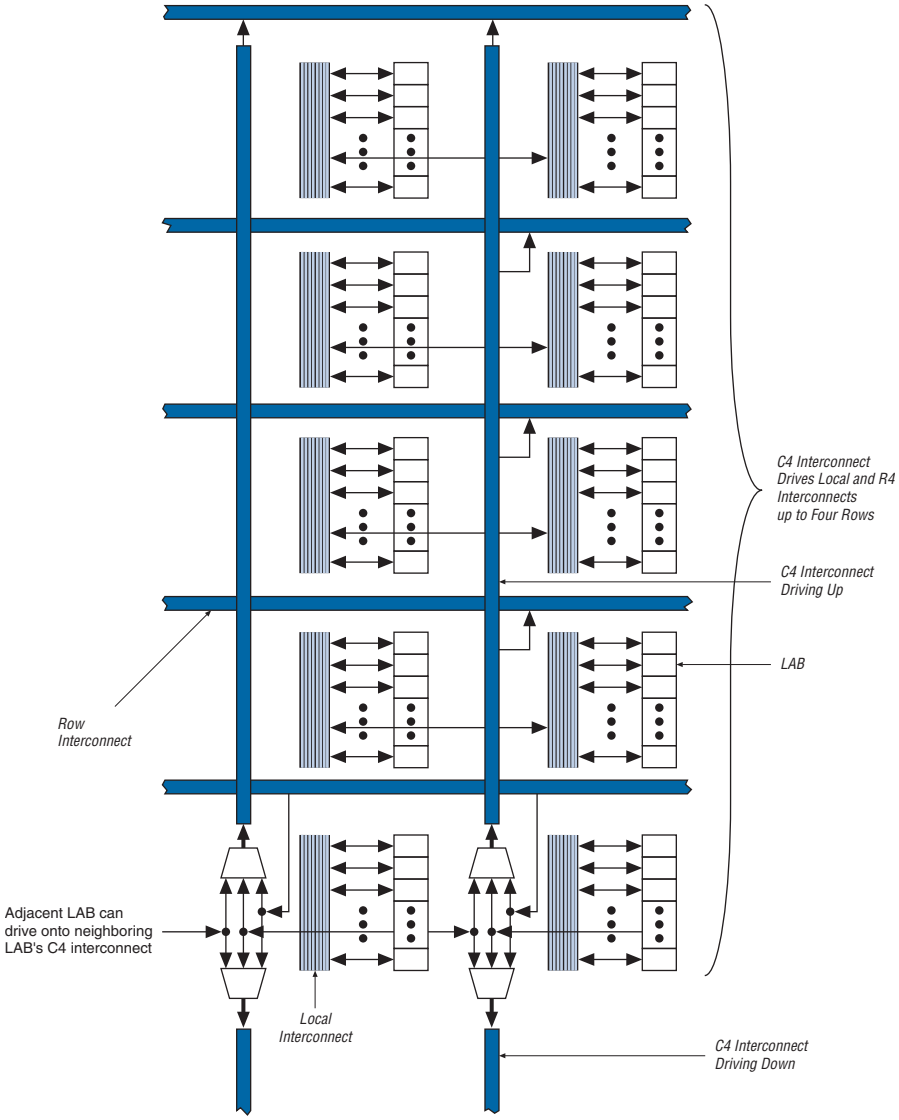
Arria GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–40 shows shared arithmetic chain, carry chain, and register chain interconnects.

Figure 2–40. Shared Arithmetic Chain, Carry Chain and Register Chain Interconnects



C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–41 shows the C4 interconnect connections from a LAB in a column. C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–41. C4 Interconnect Connections *(Note 1)*



Note to Figure 2–41:

(1) Each C4 interconnect can drive either up or down four rows.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–10 lists the routing scheme for Arria GX device.

Table 2–10. Arria GX Device Routing Scheme

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Carry chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Register chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Local interconnect	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
Direct link interconnect	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
R4 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
R24 interconnect	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—
C4 interconnect	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—
C16 interconnect	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—
ALM	✓	✓	✓	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M512 RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M4K RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M-RAM block	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
DSP blocks	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
Column IOE	—	—	—	—	✓	—	—	✓	✓	—	—	—	—	—	—	—
Row IOE	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–11 lists the size and features of the different RAM blocks.

Table 2–11. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	345 MHz	380 MHz	290 MHz
True dual-port memory	—	✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	—

Table 2–11. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
ROM	✓	✓	—
FIFO buffer	✓	✓	✓
Pack mode	—	✓	✓
Byte enable	✓	✓	✓
Address clock enable	—	✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization file (**.mif**)	✓	✓	—
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support	—	✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

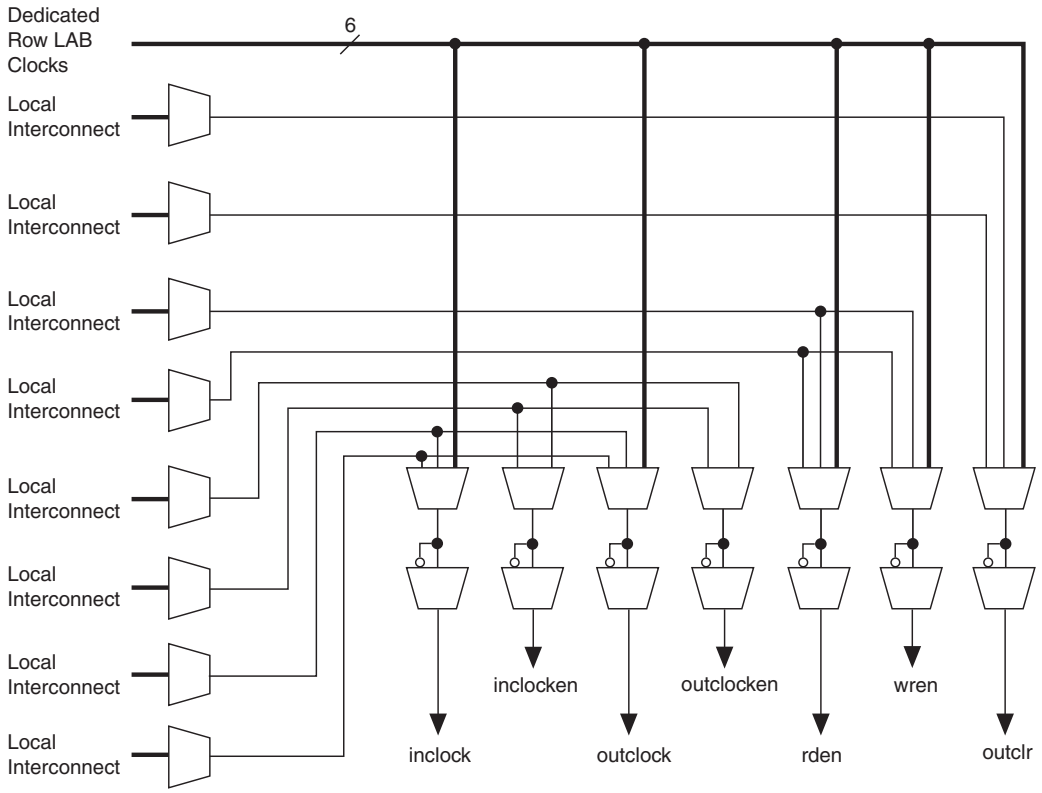
The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

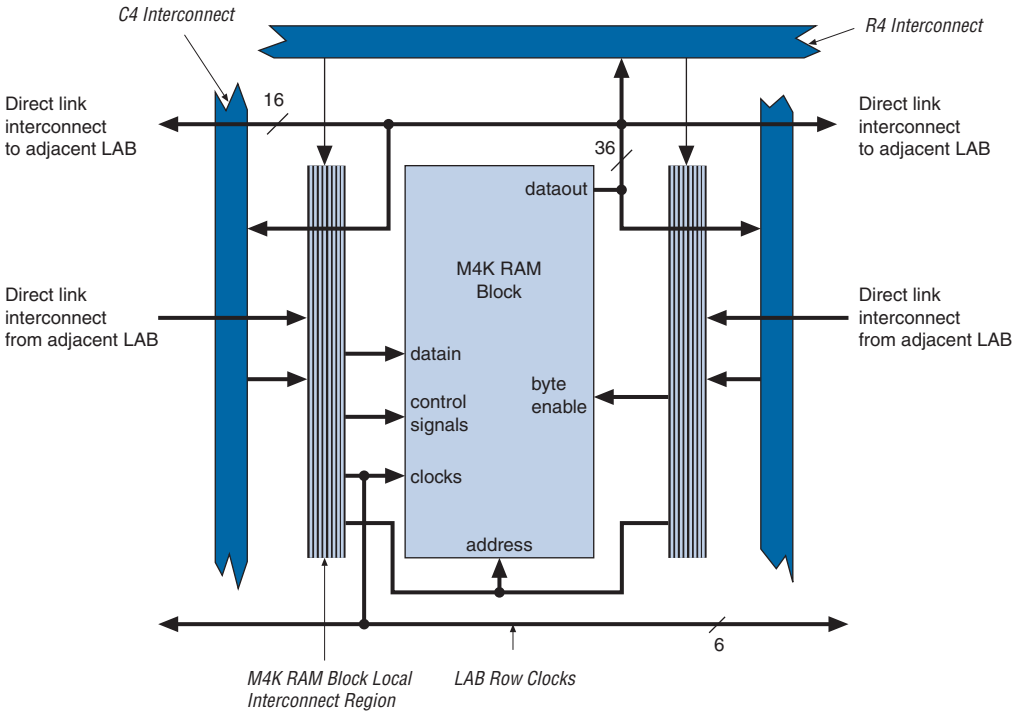
M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block, allowing the RAM block to operate in read and write or input and output clock modes. Only the output register can be bypassed. The six `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–42 shows the M512 RAM block control signal generation logic.

Figure 2–42. M512 RAM Block Control Signals



The RAM blocks in Arria GX devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–43 shows the M512 RAM block to logic array interface.

Figure 2–43. M512 RAM Block LAB Row Interface



M4K RAM Blocks

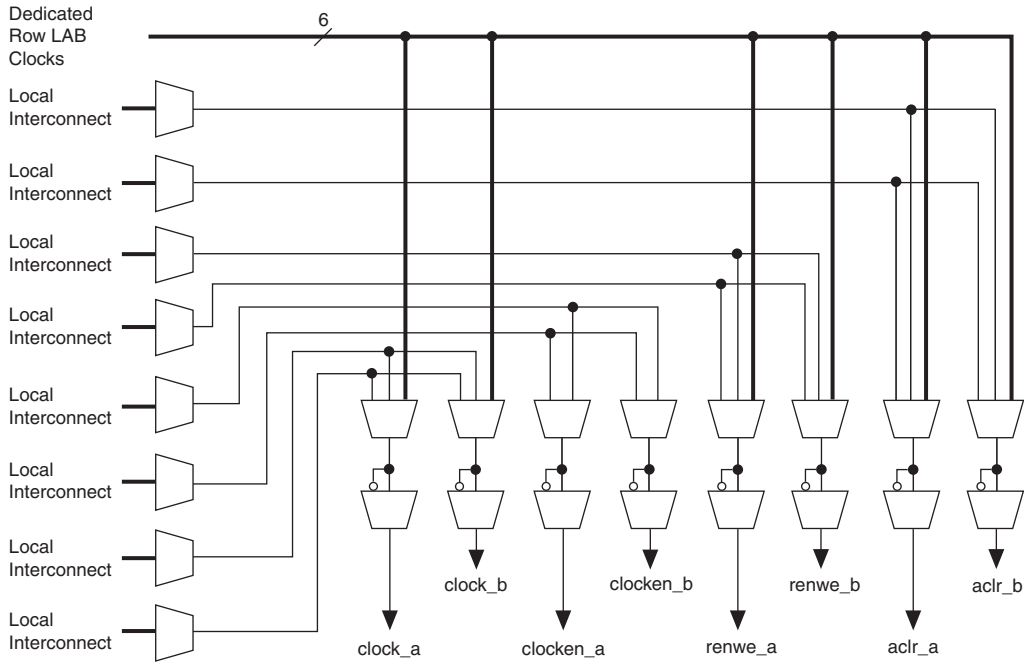
The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

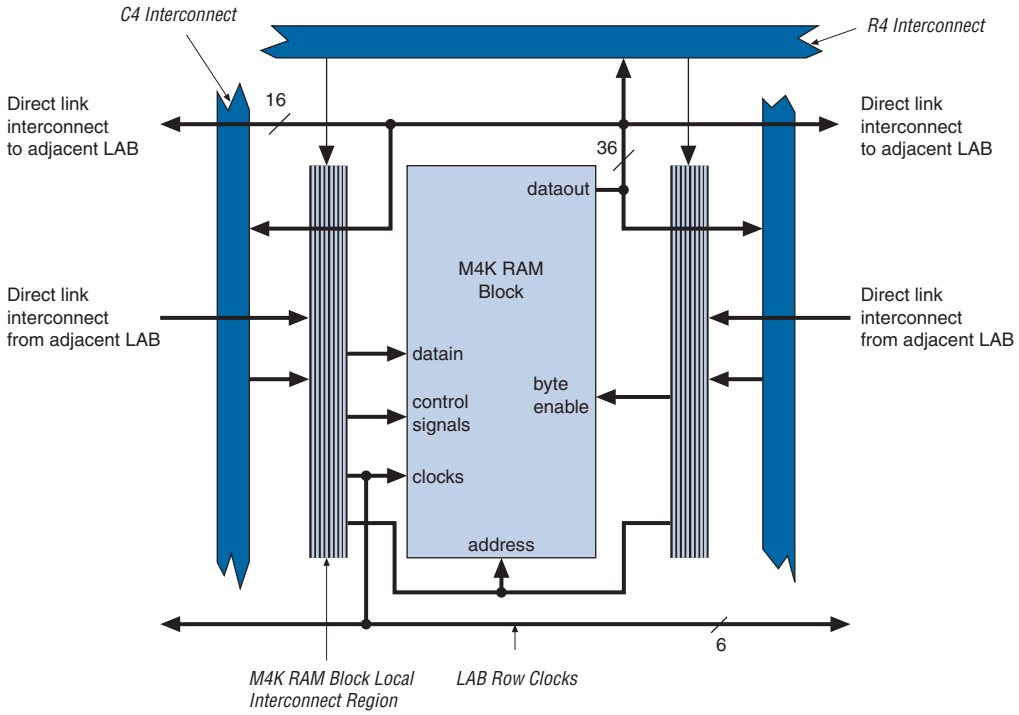
M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, `address`, `byte enable`, `datain`, and `output` registers). Only the `output` register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–44.

Figure 2–44. M4K RAM Block Control Signals



The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 are possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–45 shows the M4K RAM block to logic array interface.

Figure 2–45. M4K RAM Block LAB Row Interface



M-RAM Block

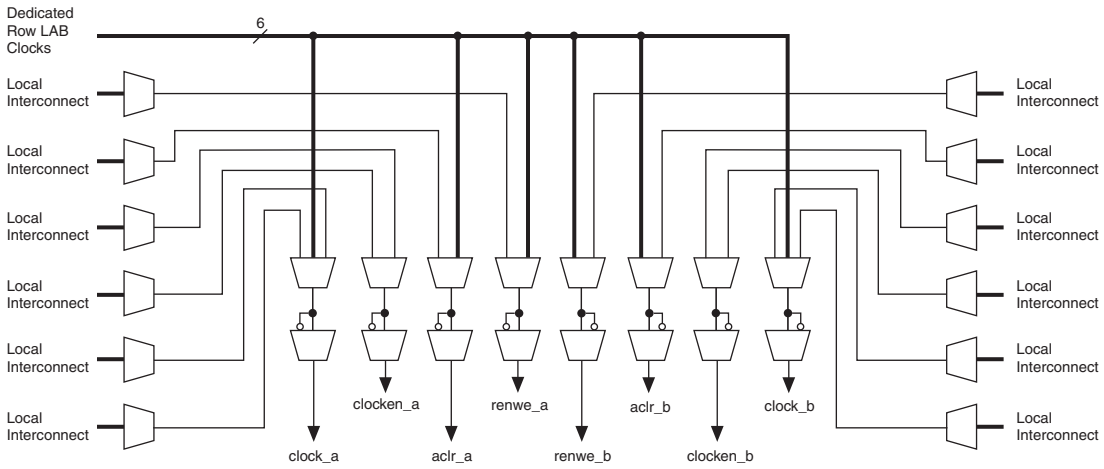
The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

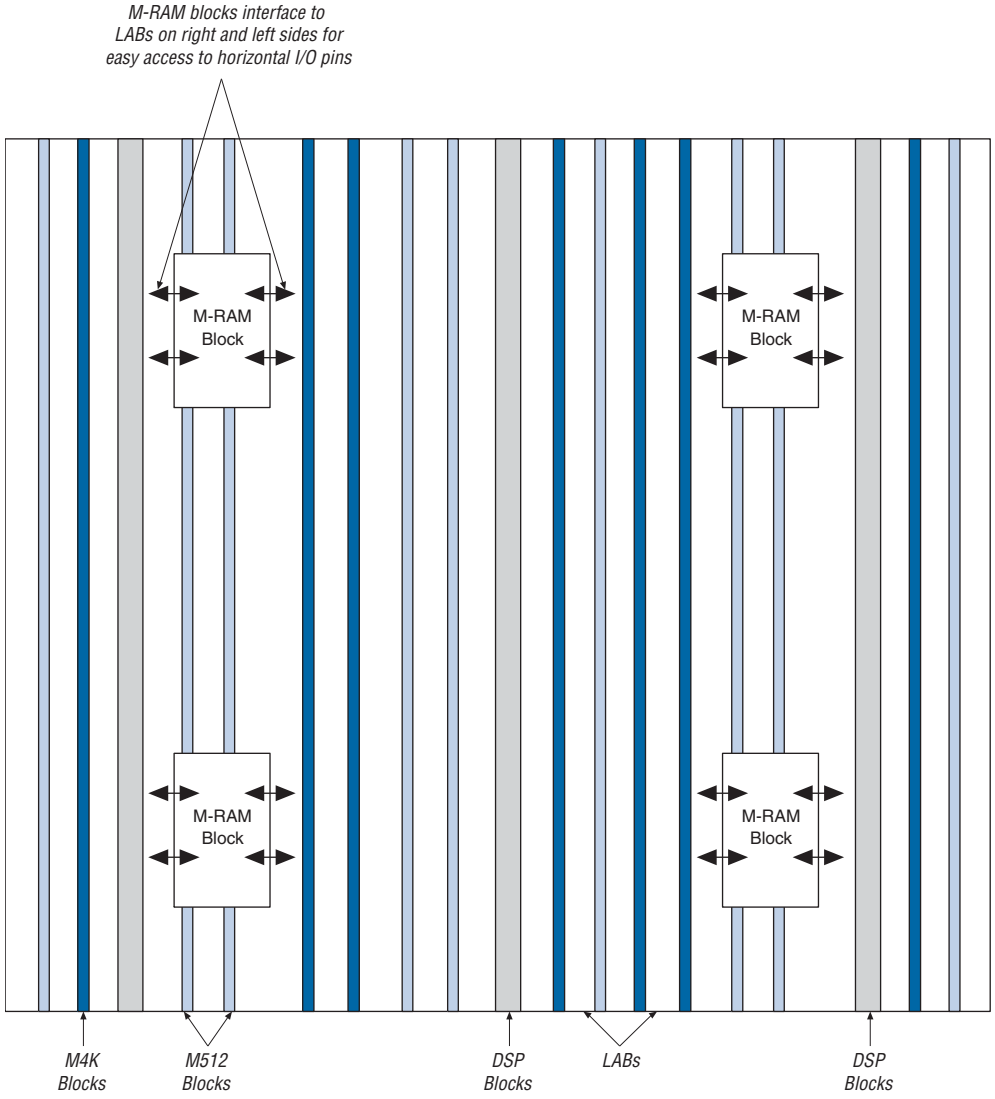
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (`renwe`, `address`, byte enable, `datain`, and output registers). You can bypass the output register. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–46.

Figure 2–46. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 are possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–47 shows an example floorplan for the EP1AGX90 device and the location of the M-RAM interfaces. Figure 2–48 and Figure 2–49 show the interface between the M-RAM block and the logic array.

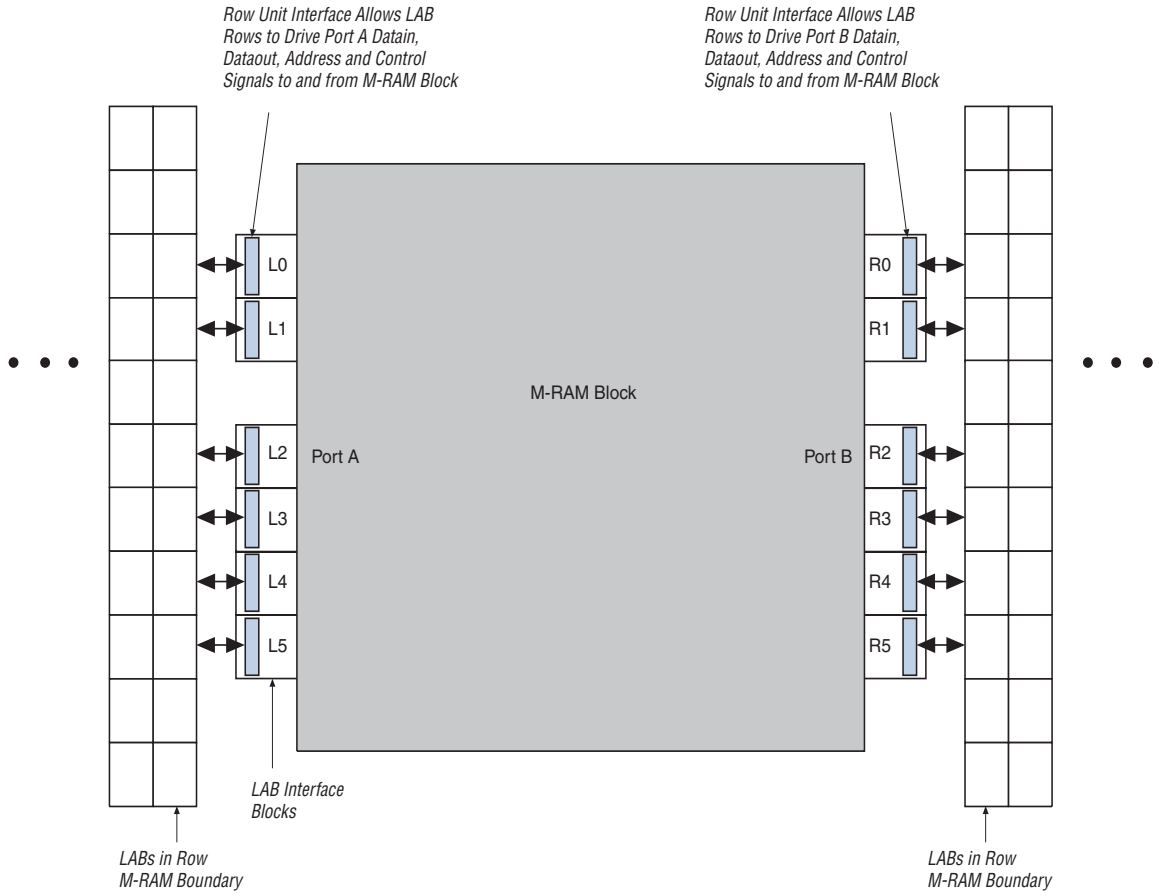
Figure 2–47. EP1AGX90 Device with M-RAM Interface Locations *(Note 1)*



Note to Figure 2–47:

(1) The device shown is an EP1AGX90 device. The number and position of M-RAM blocks vary in other devices.

Figure 2–48. M-RAM Block LAB Row Interface *(Note 1)*



Note to Figure 2–48:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

Figure 2–49. M-RAM Row Unit Interface to Interconnect

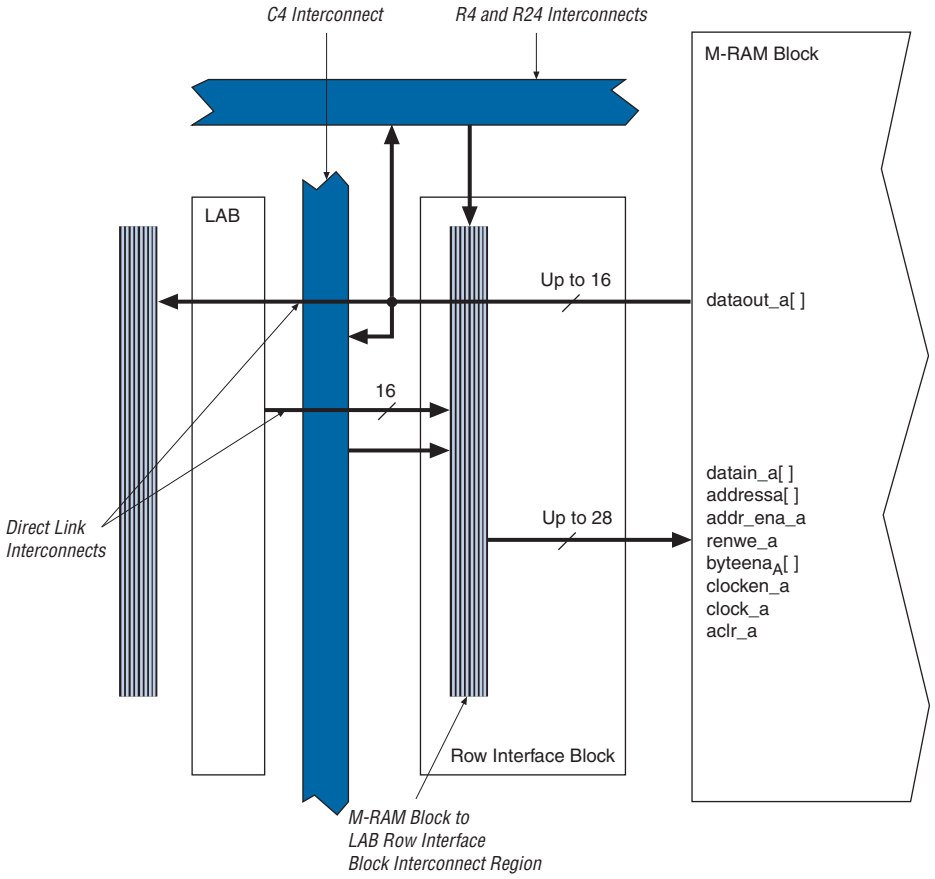


Table 2–12 lists the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

Table 2–12. M-RAM Row Interface Unit Signals (Part 1 of 2)

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]

Table 2–12. M-RAM Row Interface Unit Signals (Part 2 of 2)

Unit Interface Block	Input Signals	Output Signals
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

For more information about TriMatrix memory, refer to the *TriMatrix Embedded Memory Blocks in Arria GX Devices* chapter.

Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Arria GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Arria GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Arria GX DSP block can support one 36 × 36-bit multiplier in a single DSP block and is true for any combination of signed, unsigned, or mixed sign multiplications.

Figure 2–50 shows one of the columns with surrounding LAB rows.

Figure 2–50. DSP Blocks Arranged in Columns

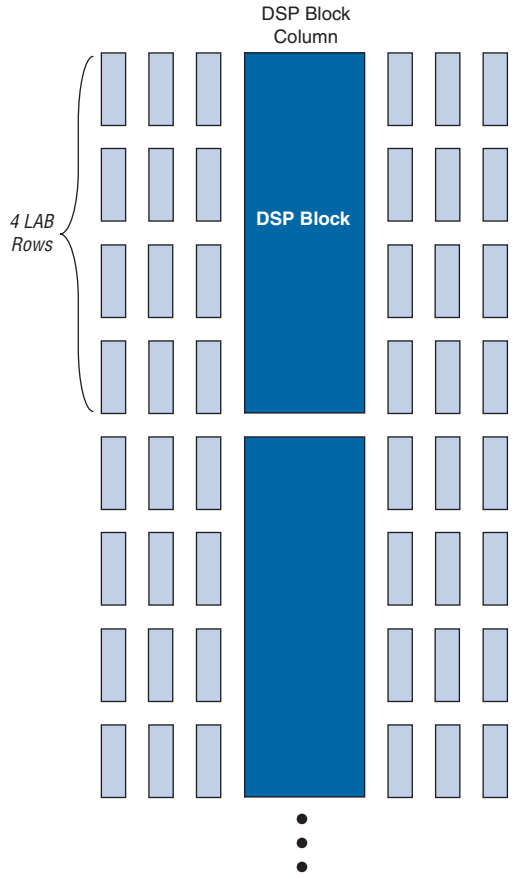


Table 2–13 lists the number of DSP blocks in each Arria GX device. DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on the configuration, which makes routing to ALMs easier, saves ALM routing resources, and increases performance because all connections and blocks are in the DSP block.

Table 2–13. DSP Blocks in Arria GX Devices *(Note 1)*

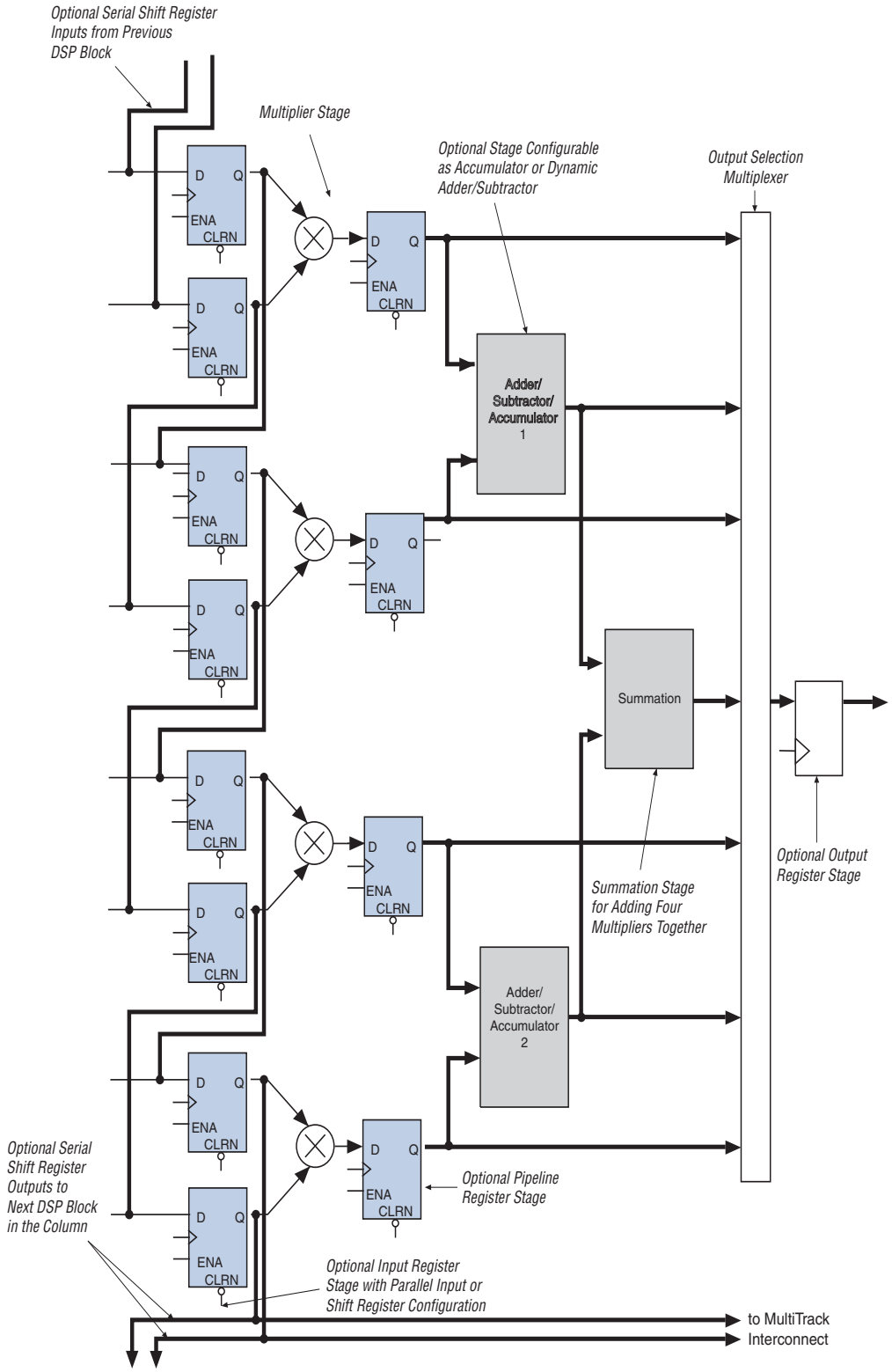
Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1AGX20	10	80	40	10
EP1AGX35	14	112	56	14
EP1AGX50	26	208	104	26
EP1AGX60	32	256	128	32
EP1AGX90	44	352	176	44

Note to Table 2–13:

(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, DSP block input registers can efficiently implement shift registers for FIR filter applications. DSP blocks support Q1.15 format rounding and saturation. Figure 2–51 shows a top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Figure 2–51. DSP Block Diagram for 18 × 18-Bit Configuration



Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–14 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, 2D FIR filters, equalizers, IIR, correlators, matrix multiplication, and many other functions. DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–14. Multiplier Size and Configurations per DSP Block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	—	Two 52-bit multiply-accumulate blocks	—
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	—
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	—

DSP Block Interface

The Arria GX device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between shift register inputs to cascade shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region.

The outputs also work similarly to LAB outputs. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and 18 can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing.

Figure 2–52 and Figure 2–53 show the DSP block interfaces to LAB rows.

Figure 2–52. DSP Block Interconnect Interface

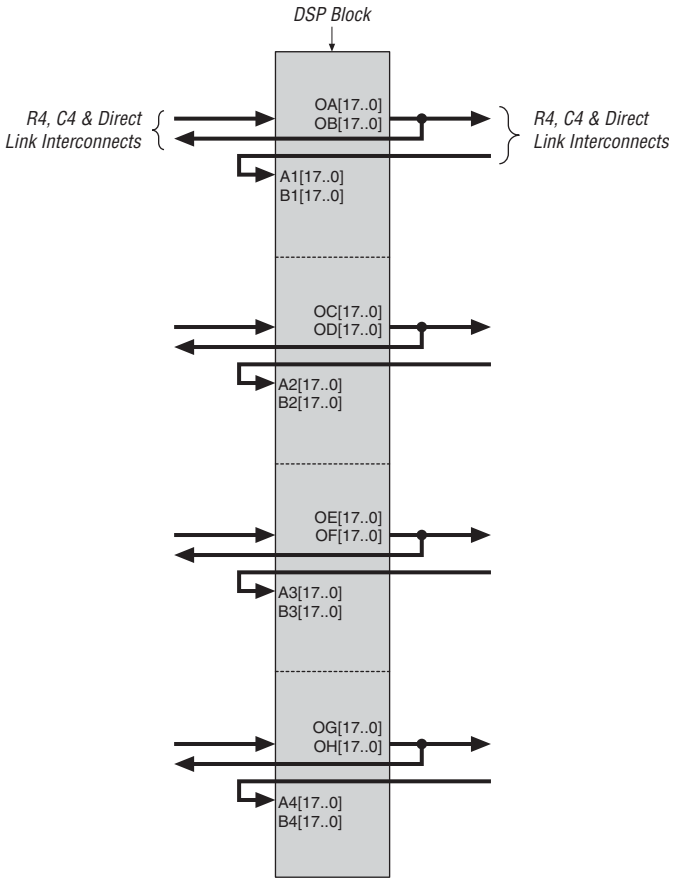
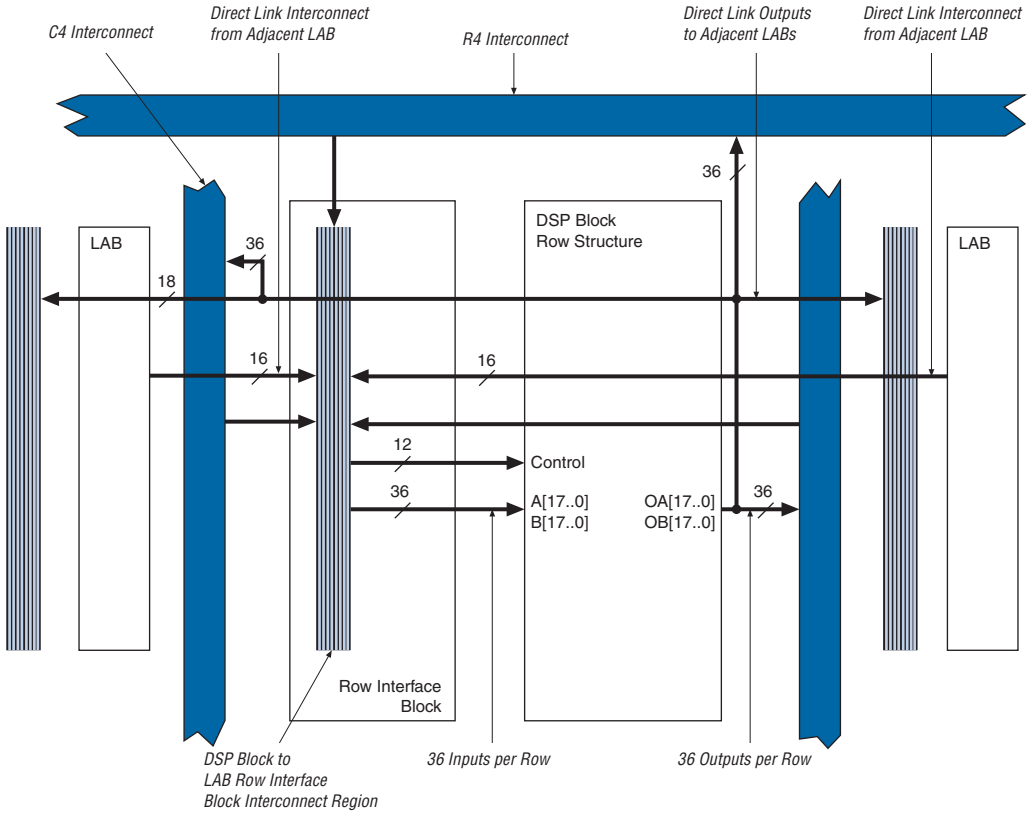


Figure 2–53. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–15.

For more information about DSP blocks, refer to the *DSP Blocks in Arria GX Devices* chapter.

Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

PLLs and Clock Networks

Arria GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global and Hierarchical Clocking

Arria GX devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Arria GX devices.

There are 12 dedicated clock pins (`CLK[15..12]` and `CLK[7..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device except the right side, as shown in Figure 2–54 and Figure 2–55. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. Table 2–16 lists the global and regional clock features.

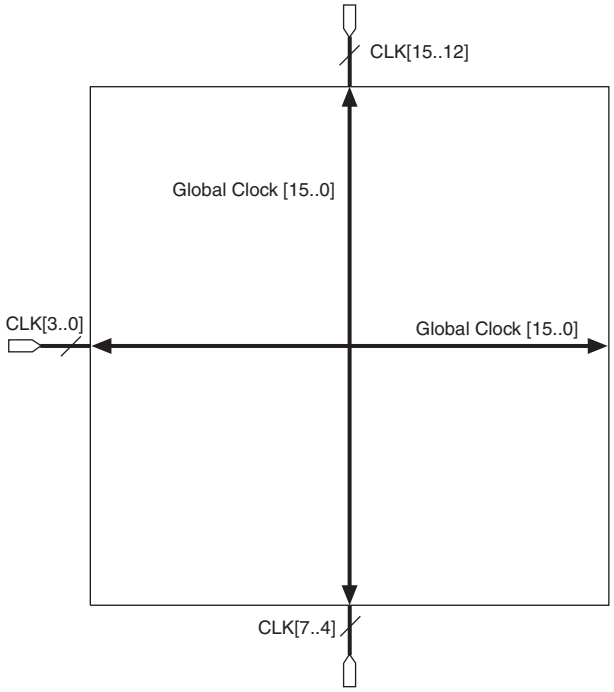
Table 2–16. Global and Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	Clock pins, PLL outputs, core routings, inter-transceiver clocks	Clock pins, PLL outputs, core routings, inter-transceiver clocks
Dynamic clock source selection	✓	—
Dynamic enable/disable	✓	✓

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. GCLK networks can be used as clock sources for all resources in the device IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–54 shows the 12 dedicated `CLK` pins driving global clock networks.

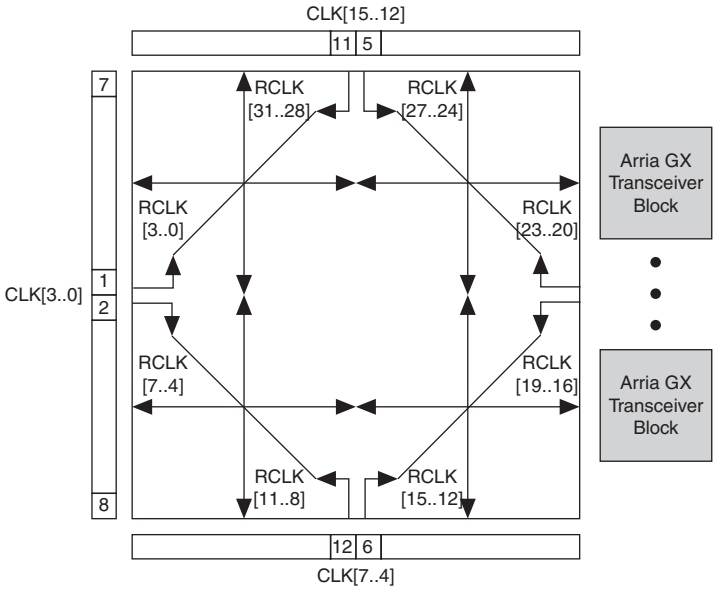
Figure 2–54. Global Clocking



Regional Clock Network

There are eight RCLK networks (RCLK[7..0]) in each quadrant of the Arria GX device that are driven by the dedicated CLK[15..12] and CLK[7..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–55.

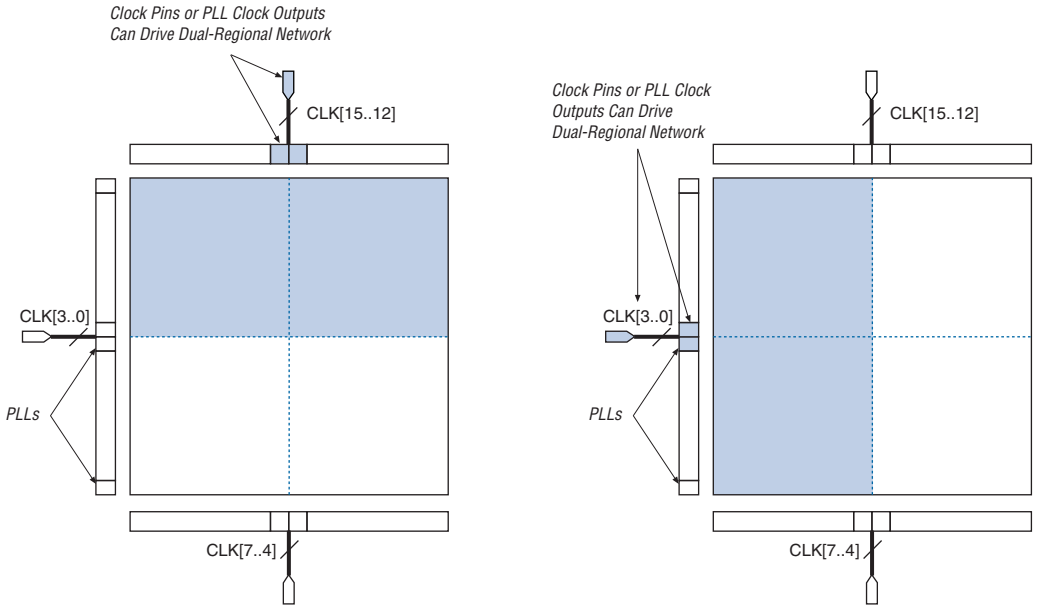
Figure 2–55. Regional Clocks



Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-RCLK by driving two RCLK network lines in adjacent quadrants (one from each quadrant), which allows logic that spans multiple quadrants to use the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–56. Corner PLLs cannot drive dual-regional clocks.

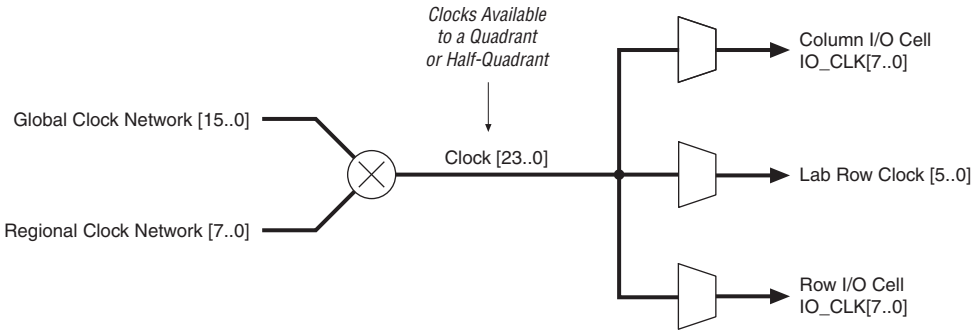
Figure 2–56. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and eight regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (refer to Figure 2–57).

Figure 2–57. Hierarchical Clock Networks Per Quadrant



You can use the Quartus II software to control whether a clock input pin drives either a GCLK, RCLK, or dual-RCLK network. The Quartus II software automatically selects the clocking resources if not specified.

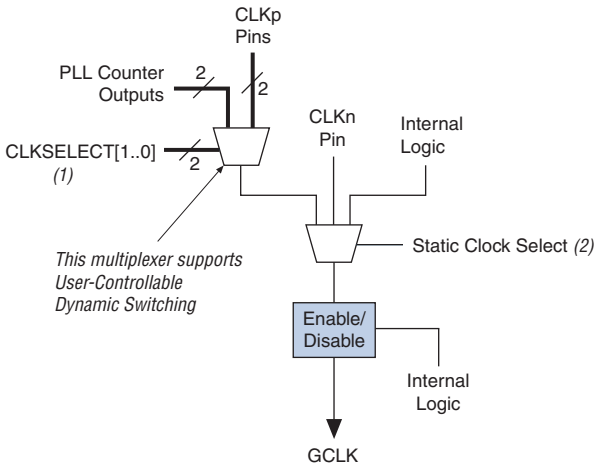
Clock Control Block

Each GCLK, RCLK, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

Figure 2–58 through Figure 2–60 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–58. Global Clock Control Blocks

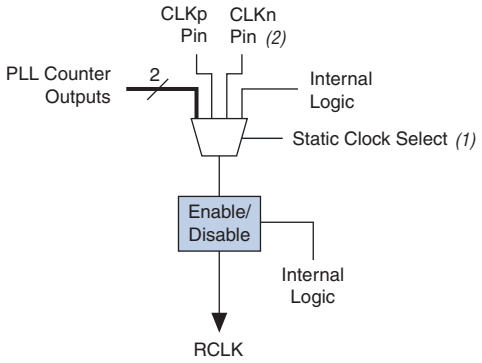


Notes to Figure 2–58:

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (SRAM Object File [**.sof**] or Programmer Object File [**.pof**]) and cannot be dynamically controlled during user mode operation.

Figure 2–59. Regional Clock Control Blocks

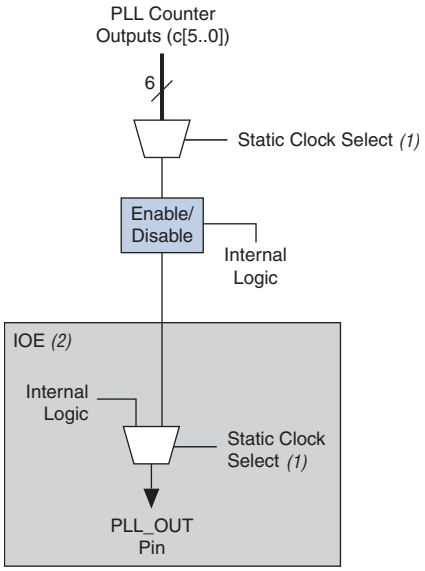


Notes to Figure 2–59:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) Only the `CLKn` pins on the top and bottom of the device feed to regional clock select.

Figure 2–60. External PLL Output Clock Control Blocks



Notes to Figure 2–60:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or controlling the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

Arria GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device. GCLK and RCLK networks can be powered down statically through a setting in the configuration file (**.sof** or **.pof**). Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software. The dynamic clock enable or disable feature allows the internal logic to control power up/down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figure 2–58 through Figure 2–60.

Enhanced and Fast PLLs

Arria GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Arria GX device's enhanced PLLs provide you with complete control of your clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Arria GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–17 lists the PLLs available for each Arria GX device and their type.

Table 2–17. Arria GX Device PLL Availability *(Note 1)*, *(2)*

Device	Fast PLLs								Enhanced PLLs			
	1	2	3 *(3)*	4 *(3)*	7	8	9 *(3)*	10 *(3)*	5	6	11	12
EP1AGX20	✓	✓	—	—	—	—	—	—	✓	✓	—	—
EP1AGX35	✓	✓	—	—	—	—	—	—	✓	✓	—	—
EP1AGX50 *(4)*	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓
EP1AGX60 *(5)*	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓
EP1AGX90	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓

Notes to Table 2–17:

(1) The global or regional clocks in a fast PLL's transceiver block can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) EP1AGX20C, EP1AGX35C/D, EP1AGX50C and EP1AGX60C/D devices only have two fast PLLs (PLLs 1 and 2), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown in this table.

(3) PLLs 3, 4, 9, and 10 are not available in Arria GX devices.

(4) 4 or 8 PLLs are available depending on C or D device and the package option.

(5) 4or 8 PLLs are available depending on C, D, or E device option.

Table 2–18 lists the enhanced PLL and fast PLL features in Arria GX devices.

Table 2–18. Arria GX PLL Features (Part 1 of 2)

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	—
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*

Table 2–18. Arria GX PLL Features (Part 2 of 2)

Feature	Enhanced PLL	Fast PLL
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	—

Notes to Table 2–18:

(1) For enhanced PLLs, *m*, *n* range from 1 to 256 and post-scale counters range from 1 to 512 with 50% duty cycle.

(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.

(3) The smallest phase shift is determined by the voltage controlled oscillator (V_{CO}) period divided by 8.

(4) For degree increments, Arria GX devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.

(5) Arria GX fast PLLs only support manual clock switchover.

(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.

(7) If the feedback input is used, you lose one (or two, if f_{BIN} is differential) external clock output pin.

(8) Every Arria GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–61 shows a top-level diagram of the Arria GX device and PLL floorplan.

Figure 2–61. PLL Locations

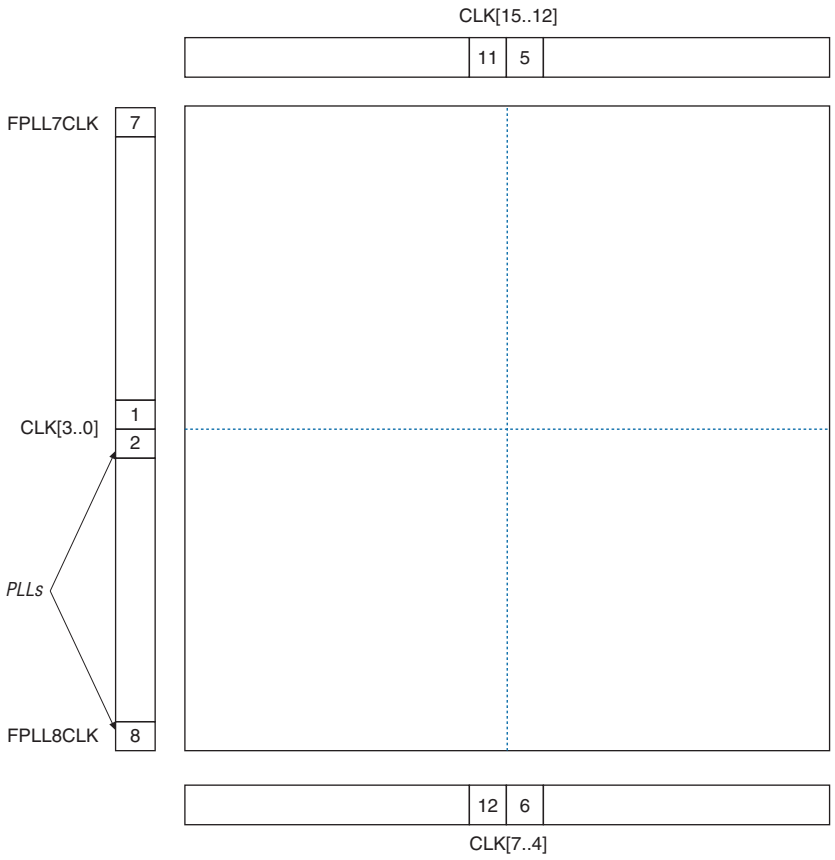
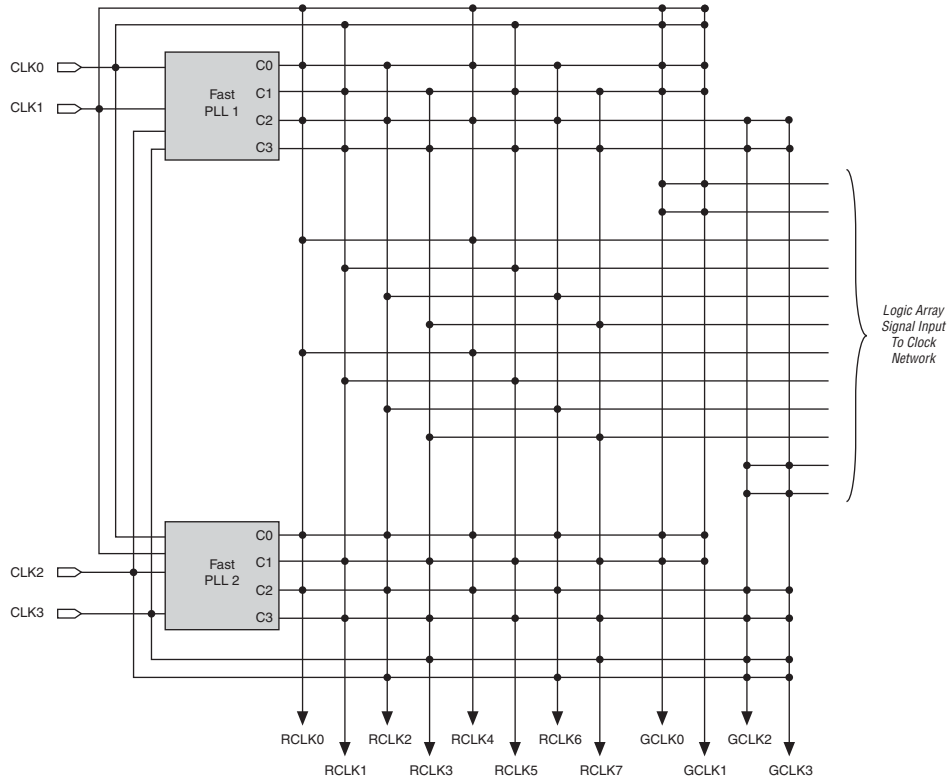


Figure 2–62 and Figure 2–63 shows global and regional clocking from the fast PLL outputs and side clock pins. The connections to the global and regional clocks from the fast PLL outputs, internal drivers, and `CLK` pins on the left side of the device are shown in Table 2–19.

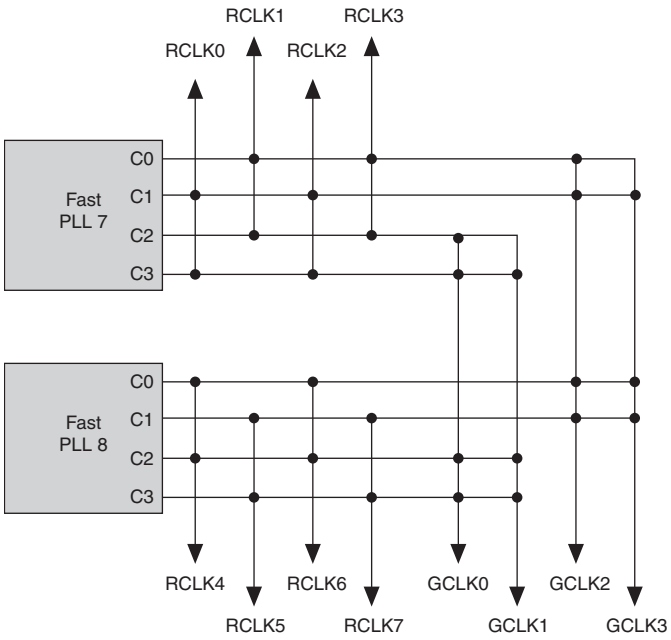
Figure 2–62. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–62:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Figure 2–63. Global and Regional Clock Connections from Corner Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–63:

(1) The GCLK or RCLK in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Table 2–19. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 1 of 2)

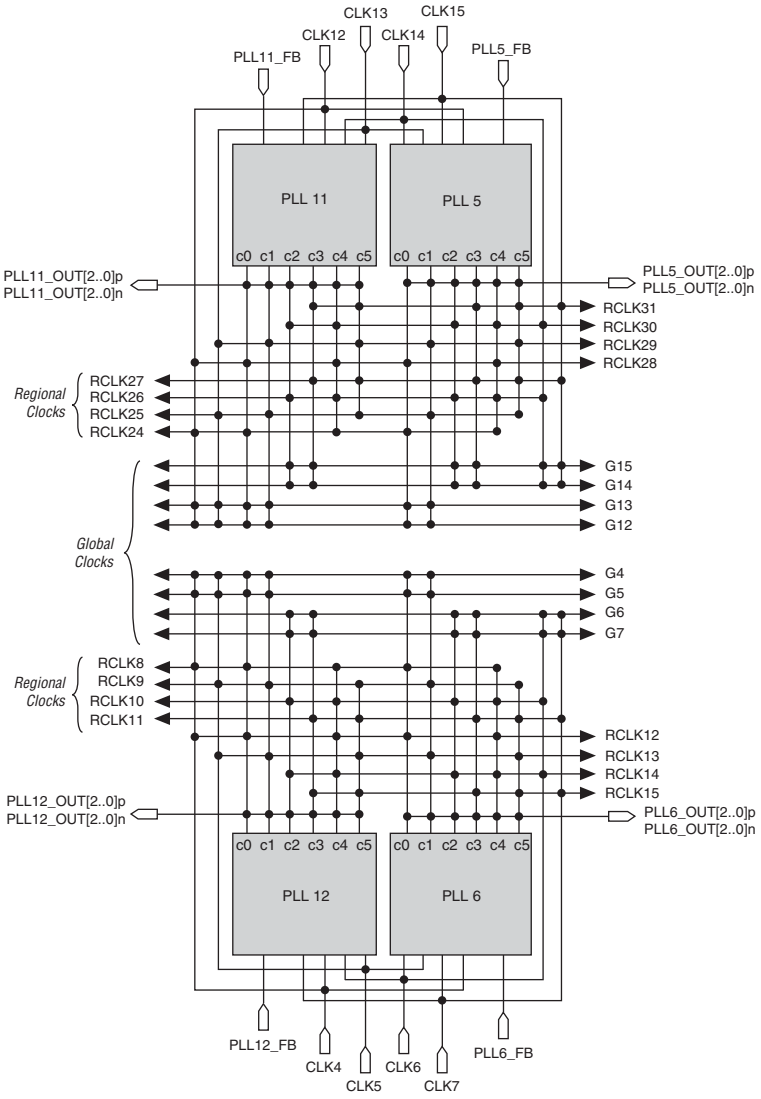
Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Clock Pins												
CLK0p	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK1p	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK2p	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK3p	—	—	✓	✓	—	—	—	✓	—	—	—	✓
Drivers from Internal Logic												
GCLKDRV0	✓	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	✓	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	✓	✓	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	✓	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	✓	—	—	—	✓	—

Table 2–19. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 2 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
RCLKDRV7	—	—	—	—	—	—	—	✓	—	—	—	✓
PLL 1 Outputs												
c0	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c1	✓	✓	—	—	—	✓	—	✓		✓	—	✓
c2	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
c3	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
PLL 2 Outputs												
c0	✓	✓	—	—	—	✓	—	✓	—	✓	—	✓
c1	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c2	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
c3	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
PLL 7 Outputs												
c0	—	—	✓	✓	—	✓	—	✓	—	—	—	—
c1	—	—	✓	✓	✓	—	✓	—	—	—	—	—
c2	✓	✓	—	—	—	✓	—	✓	—	—	—	—
c3	✓	✓	—	—	✓	—	✓	—	—	—	—	—
PLL 8 Outputs												
c0	—	—	✓	✓	—	—	—	—	✓	—	✓	—
c1	—	—	✓	✓	—	—	—	—	—	✓	—	✓
c2	✓	✓	—	—	—	—	—	—	✓	—	✓	—
c3	✓	✓	—	—	—	—	—	—	—	✓	—	✓

Figure 2–64 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–64. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs *(Note 1)*



Note to Figure 2–64:

(1) If the design uses the feedback input, you might lose one (or two if FBIN is differential) external clock output pin.

The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs are shown in Table 2–20. The connections to the clocks from the bottom clock pins are shown in Table 2–21.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

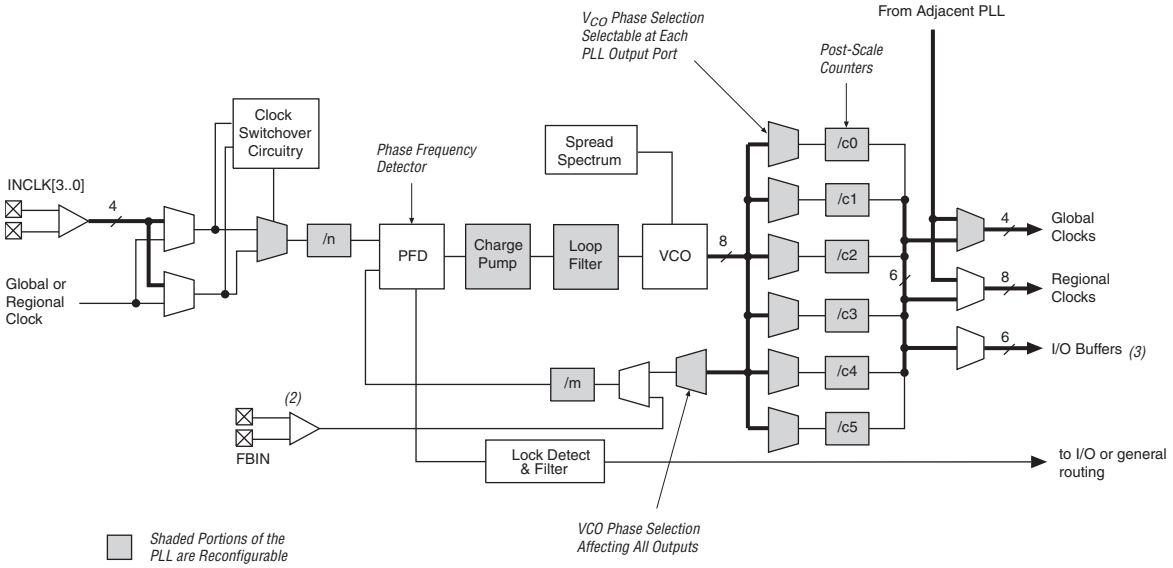
Table 2–21. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs

Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK5p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK6p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK7p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK4n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK5n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK6n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK7n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—		✓	
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 12 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Enhanced PLLs

Arria GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2–65 shows a diagram of the enhanced PLL.

Figure 2–65. Arria GX Enhanced PLL *(Note 1)*



Notes to Figure 2–65:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.

(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.

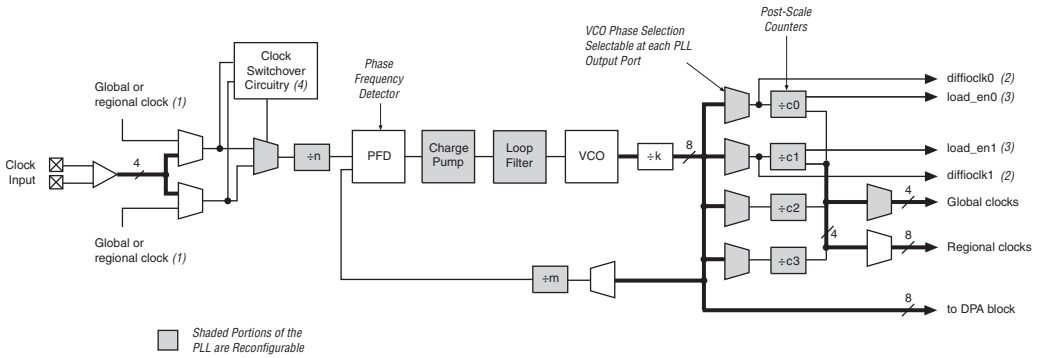
(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Fast PLLs

Arria GX devices contain up to four fast PLLs with high-speed serial interfacing ability. Fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2–66 shows a diagram of the fast PLL.

Figure 2–66. Arria GX Device Fast PLL



Notes to Figure 2–66:

(1) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the serializer/deserializer (SERDES) circuitry. Arria GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a differential I/O SERDES control signal.

(4) Arria GX fast PLLs only support manual clock switchover.

For more information about enhanced and fast PLLs, refer to the *PLLs in Arria GX Devices* chapter. For more information about high-speed differential I/O support, refer to "High-Speed Differential I/O with DPA Support" on page 2–99.

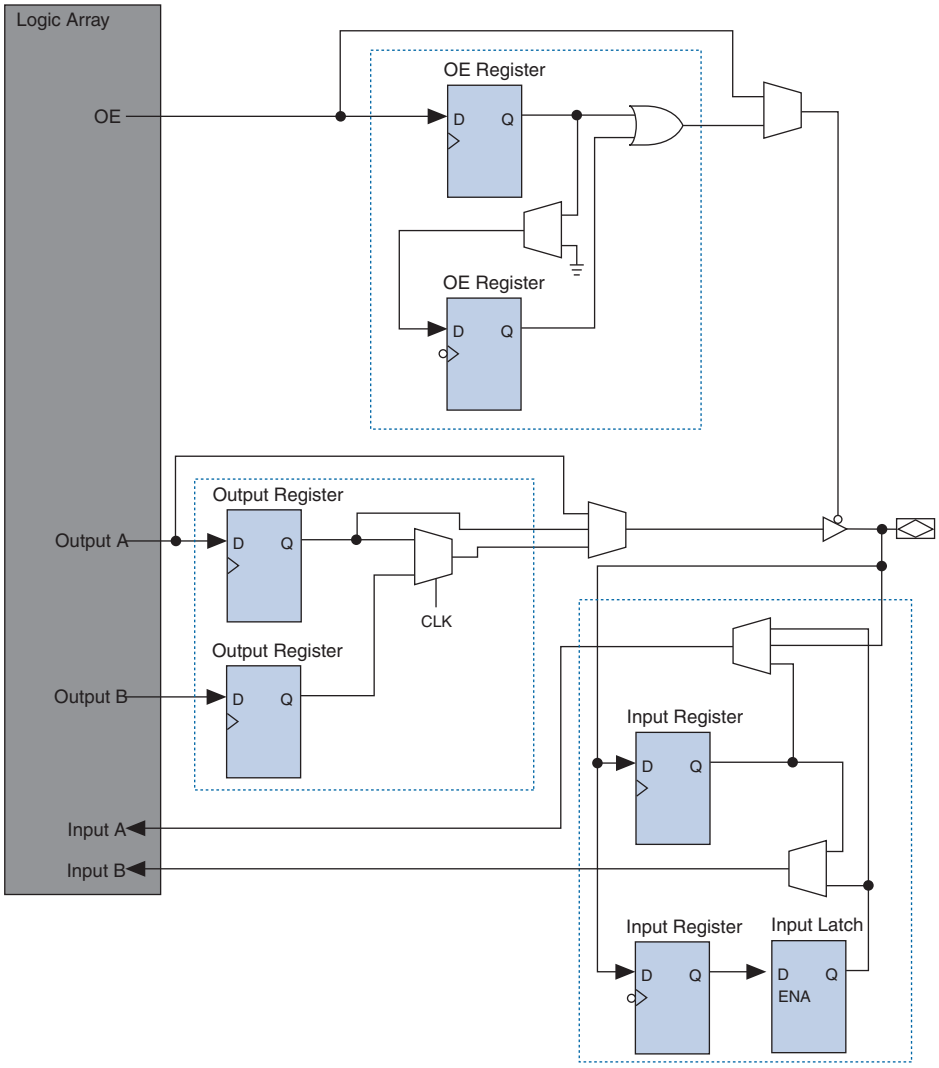
I/O Structure

Arria GX IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- JTAG boundary-scan test (BST) support
- On-chip driver series termination
- OCT for differential standards
- Programmable pull-up during configuration
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- DDR registers

The IOE in Arria GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–67 shows the Arria GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

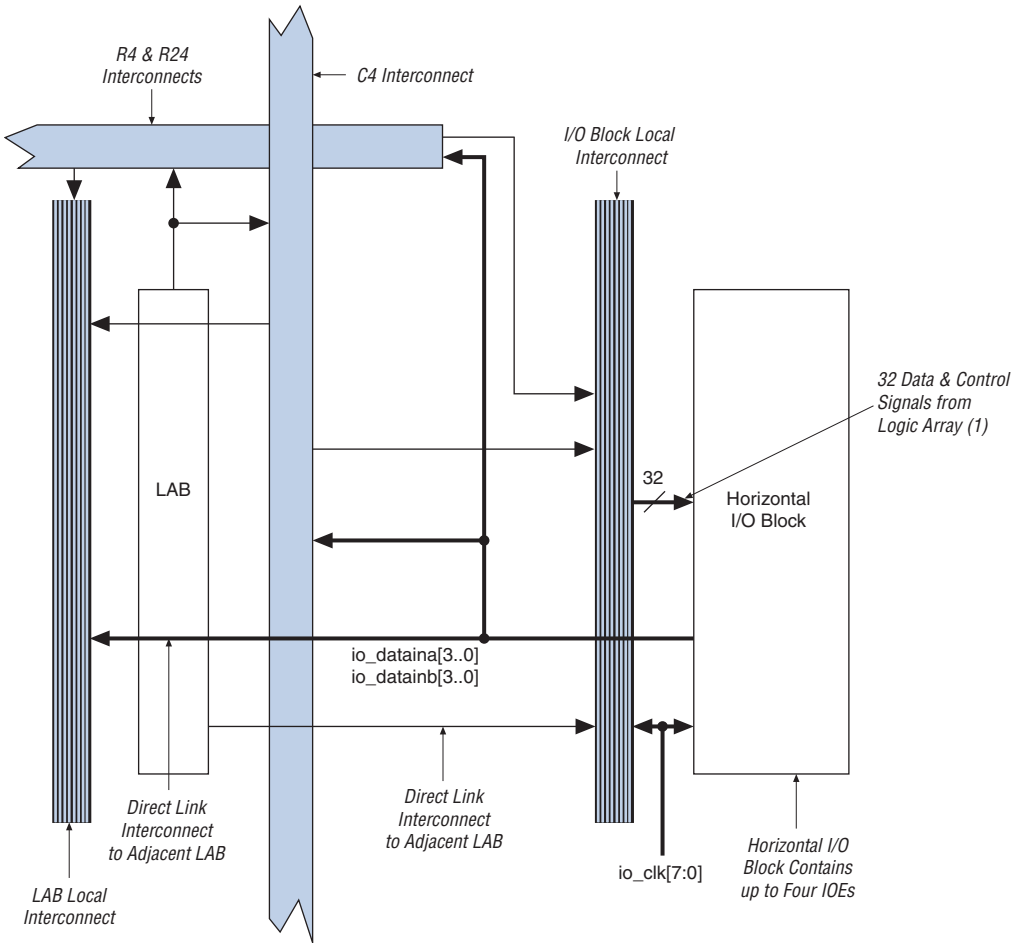
Figure 2–67. Arria GX IOE Structure



The IOEs are located in I/O blocks around the periphery of the Arria GX device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. Row I/O blocks drive row, column, or direct link interconnects. Column I/O blocks drive column interconnects.

Figure 2–68 shows how a row I/O block connects to the logic array.

Figure 2–68. Row I/O Block Connection to the Interconnect

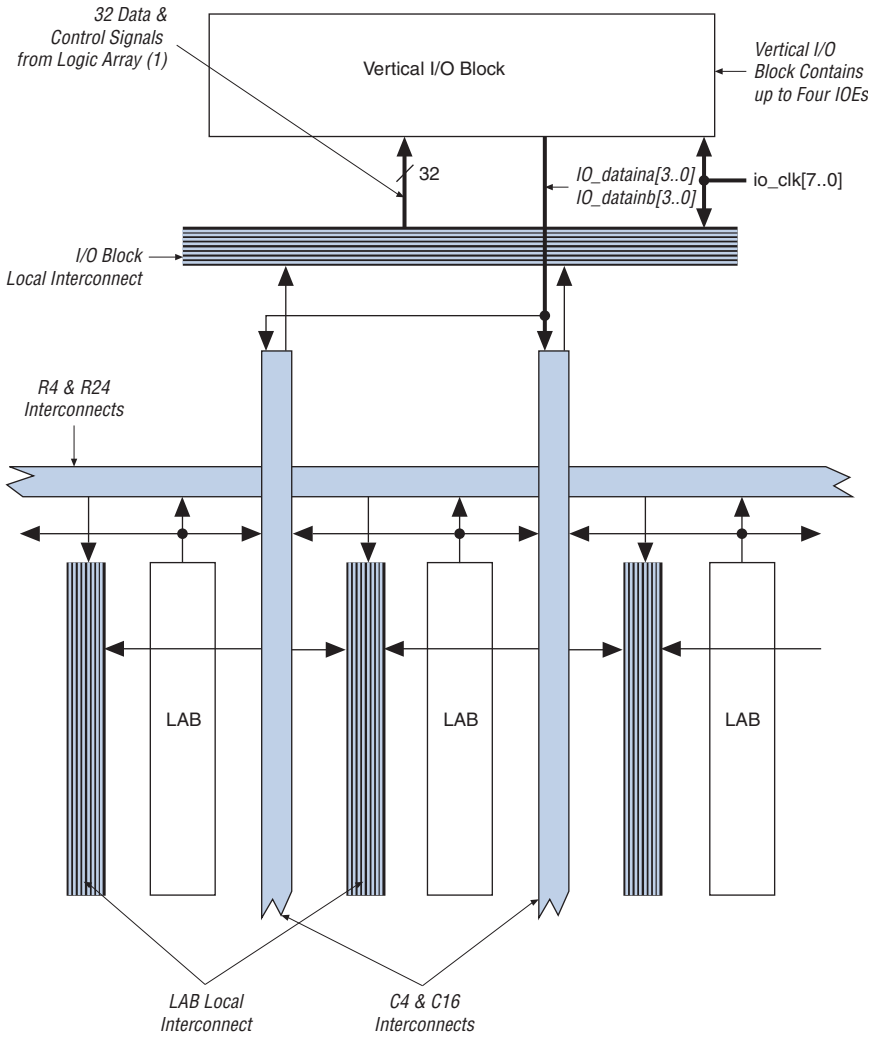


Note to Figure 2–68:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–69 shows how a column I/O block connects to the logic array.

Figure 2–69. Column I/O Block Connection to the Interconnect



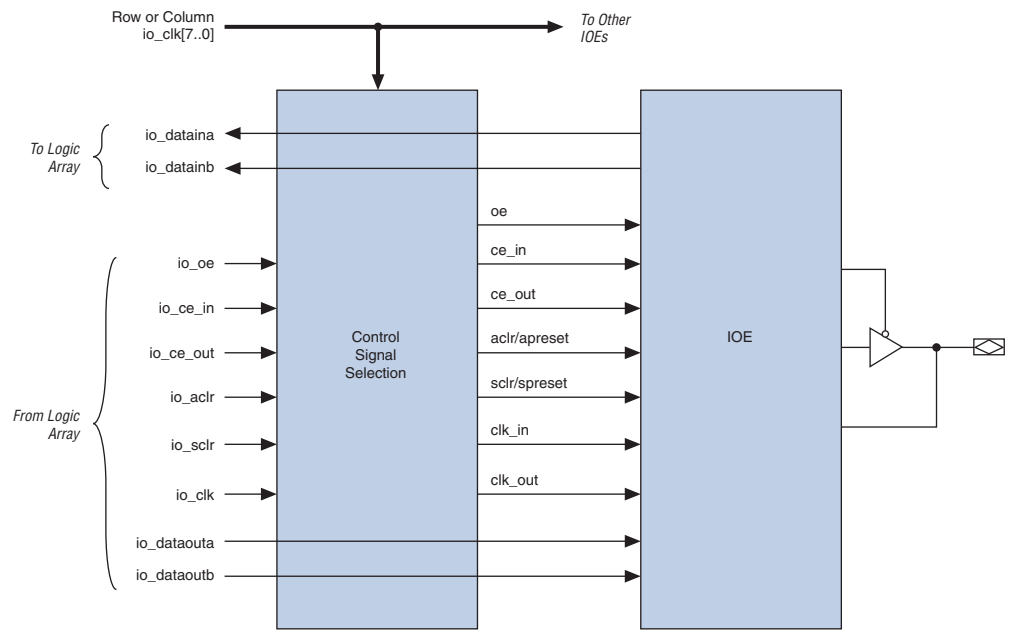
Note to Figure 2–69:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (refer to "PLLs and Clock Networks" on page 2–66).

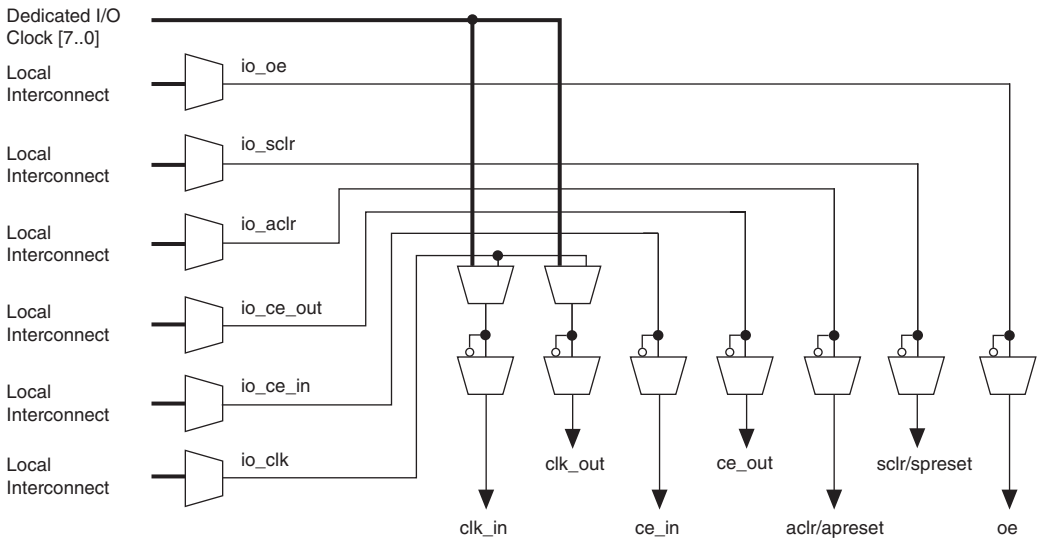
Figure 2–70 shows the signal paths through the I/O block.

Figure 2–70. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–71 shows the control signal selection.

Figure 2–71. Control Signal Selection per IOE *(Note 1)*

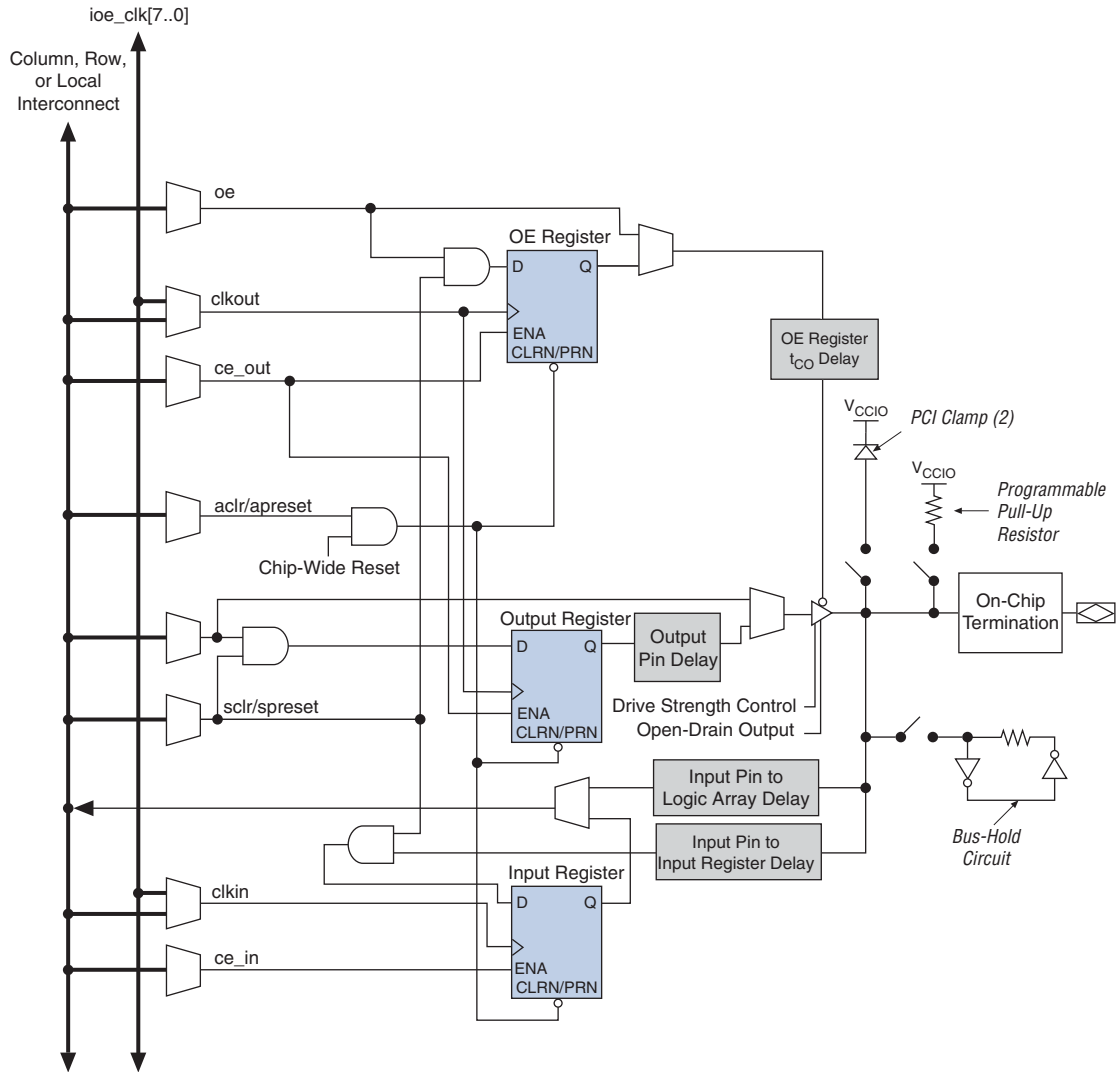


Notes to Figure 2–71:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from the local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–72 shows the IOE in bidirectional configuration.

Figure 2–72. Arria GX IOE in Bidirectional I/O Configuration *(Note 1)*



Notes to Figure 2–72:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The optional PCI clamp is only available on column I/O pins.

The Arria GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create zero hold time for these transfers. Table 2–22 shows the programmable delays for Arria GX devices.

Table 2–22. Arria GX Devices Programmable Delay Chain

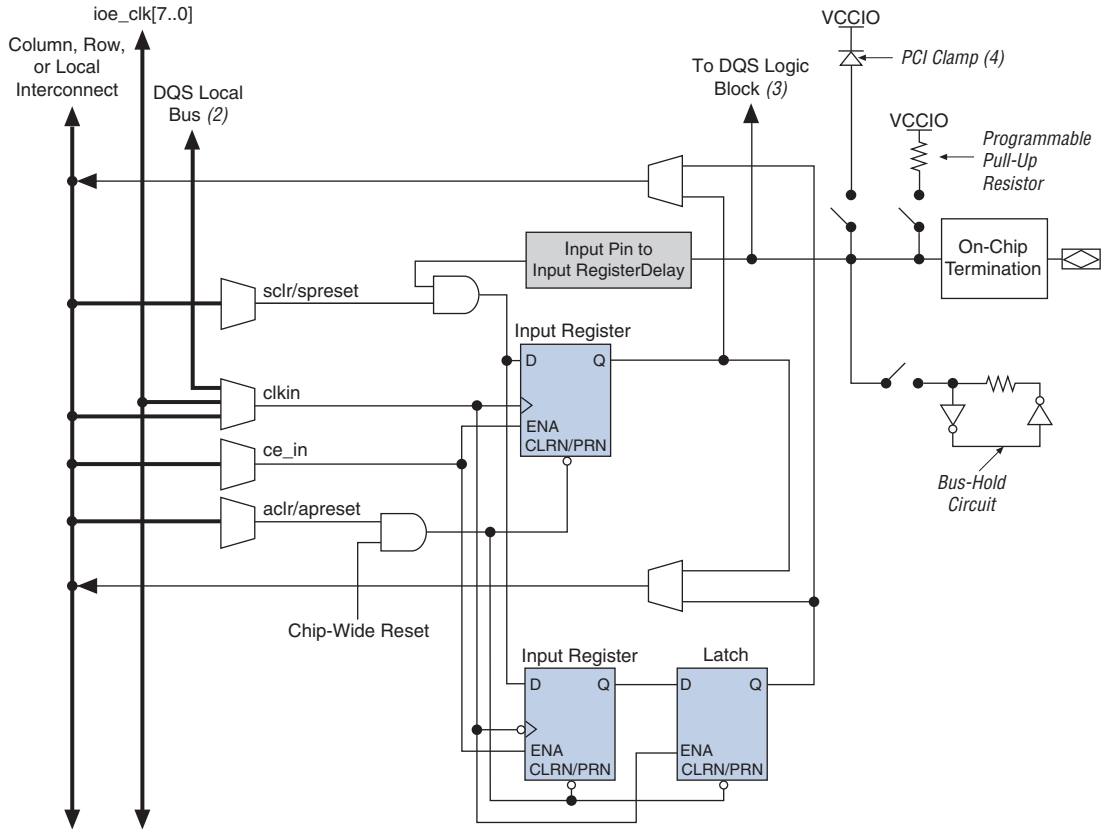
Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

IOE registers in Arria GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Arria GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Arria GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–73 shows an IOE configured for DDR input. Figure 2–74 shows the DDR input timing diagram.

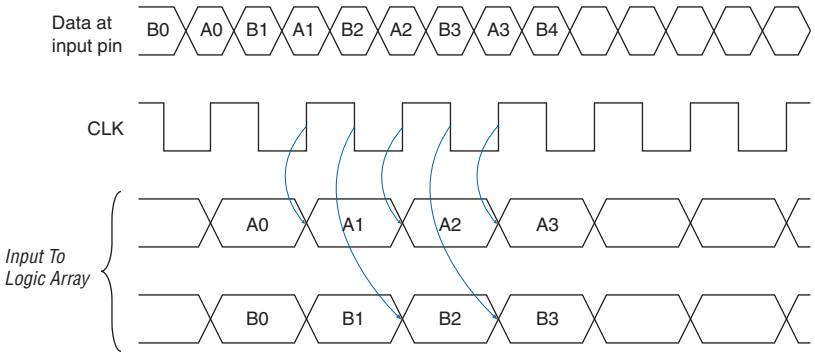
Figure 2–73. Arria GX IOE in DDR Input I/O Configuration *(Note 1)*



Notes to Figure 2–73:

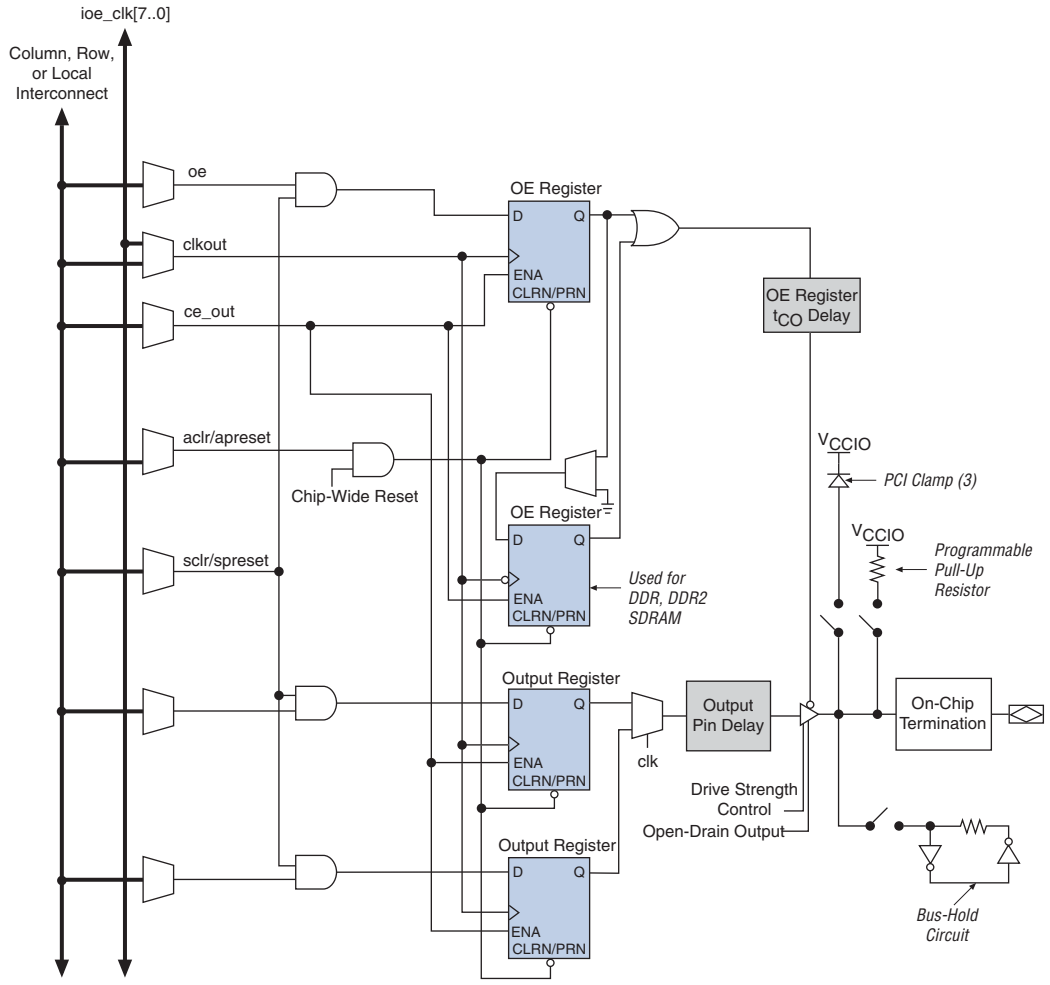
(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

Figure 2–74. Input Timing Diagram in DDR Mode



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from ALMs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–75 shows the IOE configured for DDR output. Figure 2–76 shows the DDR output timing diagram.

Figure 2–75. Arria GX IOE in DDR Output I/O Configuration *Notes (1), (2)*



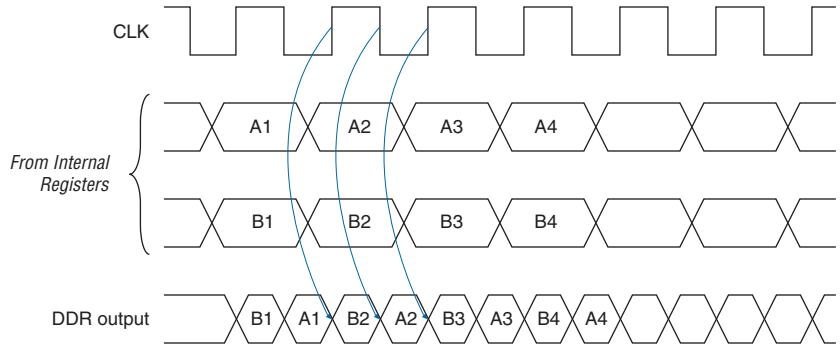
Notes to Figure 2–75:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port.

(3) The optional PCI clamp is only available on column I/O pins.

Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

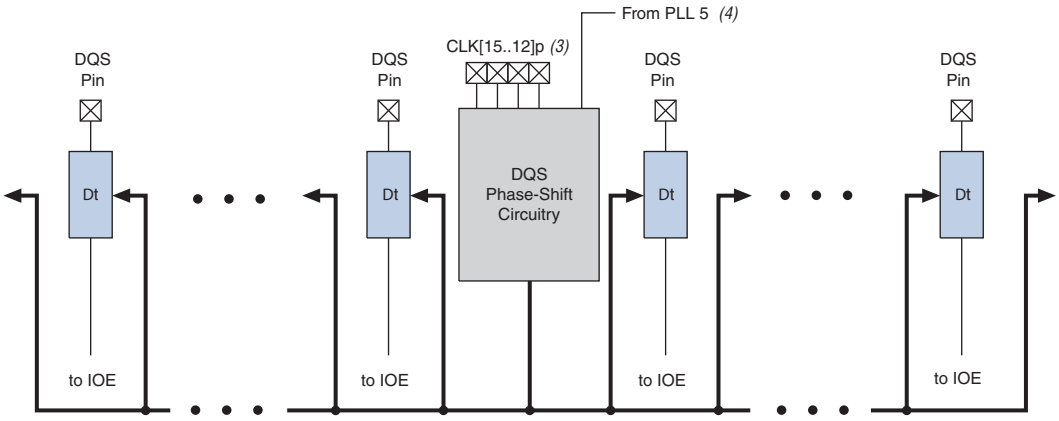
(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Arria GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–77 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–77. DQS Phase-Shift Circuitry *(Note 1)*, *(2)*



Notes to Figure 2–77:

(1) There are up to 18 pairs of DQS pins available on the top or bottom of the Arria GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to phase shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Arria GX Devices* chapter.

Programmable Drive Strength

The output buffer for each Arria GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–24 shows the possible settings for I/O standards with drive strength control.

Table 2–24. Programmable Drive Strength *(Note 1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 8	12, 8
SSTL-2 Class II	24, 20, 16	16
SSTL-18 Class I	12, 10, 8, 6, 4	10, 8, 6, 4
SSTL-18 Class II	20, 18, 16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	20, 18, 16	—
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	20, 18, 16	—

Note to Table 2–24:

(1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Arria GX devices provide an optional open-drain (equivalent to an open collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices.

Bus Hold

Each Arria GX device I/O pin provides an optional bus-hold feature. Bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

Bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 kΩ to pull the signal level to the last-driven state. This information is provided for each V_{CCIO} voltage level. Bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

For the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level, refer to the *DC & Switching Characteristics* chapter.

Programmable Pull-Up Resistor

Each Arria GX device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) holds the output to the V_{CCIO} level of the output pin's bank.

Advanced I/O Standard Support

Arria GX device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1
- LVDS
- LVPECL (on input and output clocks only)
- Differential 1.5-V HSTL class I and II
- Differential 1.8-V HSTL class I and II
- Differential SSTL-18 class I and II
- Differential SSTL-2 class I and II
- 1.2-V HSTL class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Table 2–25 describes the I/O standards supported by Arria GX devices.

Table 2–25. Arria GX Devices Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	—	3.3	—
LVCMOS	Single-ended	—	3.3	—
2.5 V	Single-ended	—	2.5	—
1.8 V	Single-ended	—	1.8	—
1.5-V LVCMOS	Single-ended	—	1.5	—
3.3-V PCI	Single-ended	—	3.3	—
3.3-V PCI-X mode 1	Single-ended	—	3.3	—
LVDS	Differential	—	2.5 *(3)*	—
LVPECL *(1)*	Differential	—	3.3	—
HyperTransport technology	Differential	—	2.5 *(3)*	—
Differential 1.5-V HSTL class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 class I and II *(2)*	Differential	1.25	2.5	1.25
1.2-V HSTL *(4)*	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25

Notes to Table 2–25:

(1) This I/O standard is only available on input and output column clock pins.

(2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9, 10, 11, and 12.

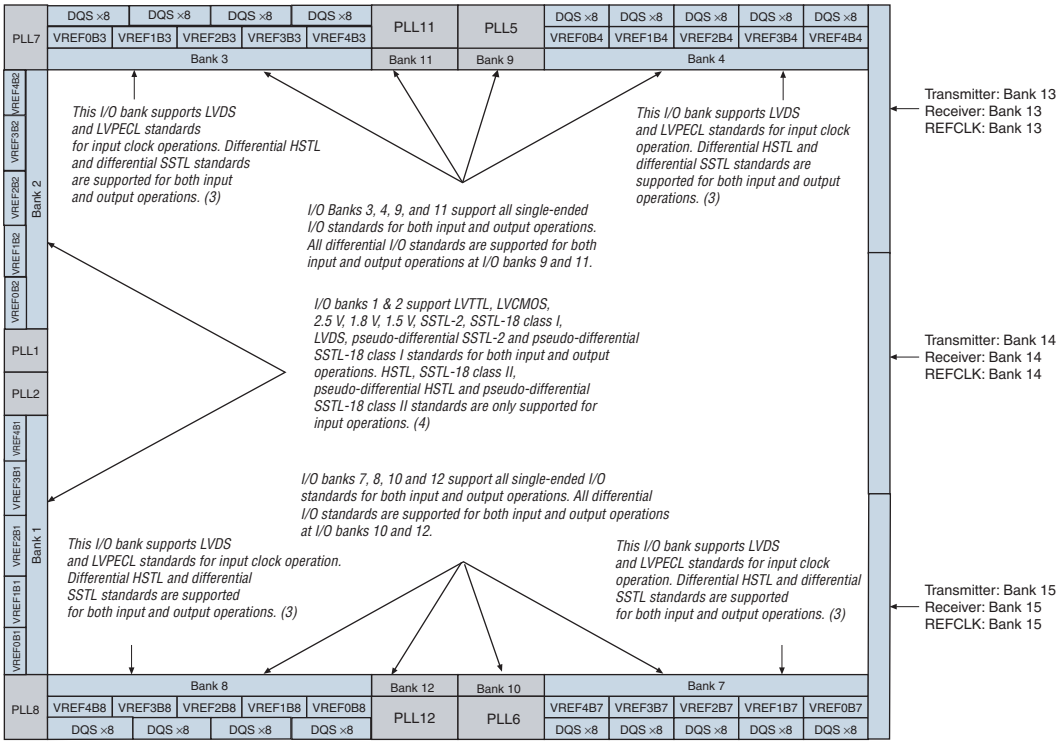
(3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 3, 4, 7, 8, 9, 10, 11, and 12).

(4) 1.2-V HSTL is only supported in I/O banks 4, 7, and 8.

For more information about the I/O standards supported by Arria GX I/O banks, refer to the *Selectable I/O Standards in Arria GX Devices* chapter.

Arria GX devices contain six I/O banks and four enhanced PLL external clock output banks, as shown in Figure 2–78. The two I/O banks on the left of the device contain circuitry to support source-synchronous, high-speed differential I/O for LVDS inputs and outputs. These banks support all Arria GX I/O standards except PCI or PCI-X I/O pins, and SSTL-18 class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Figure 2–78. Arria GX I/O Banks *(Note 1), (2)*



Notes to Figure 2–78:

(1) Figure 2–78 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. For the exact locations, refer to the pin list and the Quartus II software.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. For more information about differential I/O standards, refer to the *High-Speed Differential I/O Interfaces in Arria GX Devices* chapter.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Arria GX devices provide differential (for the LVDS technology I/O standard) and on-chip series termination to reduce reflections and maintain signal integrity. There is no calibration support for these on-chip termination resistors. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Arria GX devices provide two types of termination:

- On-chip differential termination (R_D OCT)
- On-chip series termination (R_S OCT)

Table 2–26 lists the Arria GX OCT support per I/O bank.

Table 2–26. On-Chip Termination Support by I/O Banks

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	✓
	1.5-V LVCMOS	✓	✓
	SSTL-2 class I and II	✓	✓
	SSTL-18 class I	✓	✓
	SSTL-18 class II	✓	—
	1.8-V HSTL class I	✓	✓
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	✓
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–26:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

On-Chip Differential Termination (R_D OCT)

Arria GX devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. R_D OCT is supported across the full range of supported differential data rates as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter.

For more information about R_D OCT, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

For more information about tolerance specifications for R_D OCT, refer to the *DC & Switching Characteristics* chapter.

On-Chip Series Termination (R_S OCT)

Arria GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Arria GX devices support R_S OCT for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–26 shows the list of output standards that support R_S OCT.

For more information about R_S OCT supported by Arria GX devices, refer to the *Selectable I/O Standards in Arria GX Devices* chapter.

For more information about tolerance specifications for OCT without calibration, refer to the *DC & Switching Characteristics* chapter.

MultiVolt I/O Interface

The Arria GX architecture supports the MultiVolt I/O interface feature that allows Arria GX devices in all packages to interface with systems of different supply voltages. Arria GX VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.2-, 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). Arria GX VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Table 2–27 lists Arria GX MultiVolt I/O support.

Table 2–27. Arria GX MultiVolt I/O Support *(Note 1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	*(4)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(4)*	—	—	—	—	—
1.5	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓	—	—	—	—
1.8	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓ *(3)*	✓	—	—	—
2.5	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 2–27:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Arria GX V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Arria GX device to drive out, a receiving device powered at a different level can still interface with the Arria GX device if it has inputs that tolerate the V_{CCIO} value.

(4) Arria GX devices support 1.2-V HSTL. They do not support 1.2-V LVTTL and 1.2-V LVCMOS.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside. TDO is in I/O bank 4 and nCEO is in I/O Bank 7. Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by V_{CCSEL} on slave devices. Master and slave devices can be in any position in the chain. The master device indicates that it is driving out TDO or nCEO to a slave device. For multi-device passive configuration schemes, the nCEO pin of the master device drives the nCE pin of the slave device. The VCCSEL pin on the slave device selects which input buffer is used for nCE. When V_{CCSEL} is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When V_{CCSEL} is logic low, it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the V_{CCSEL} settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application.

Table 2–28 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

Table 2–28. Board Design Recommendations for nCEO and nCE Input Buffer Power

nCE Input Buffer Power in I/O Bank 3	Arria GX nCEO V_{CCIO} Voltage Level in I/O Bank 7				
	V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
VCCSEL high (V_{CCIO} Bank 3 = 1.5 V)	✓ *(1), (2)*	✓ *(3), (4)*	✓ *(5)*	✓	✓
VCCSEL high (V_{CCIO} Bank 3 = 1.8 V)	✓ *(1), (2)*	✓ *(3), (4)*	✓	✓	Level shifter required
VCCSEL low (nCE powered by V_{CCPD} = 3.3 V)	✓	✓ *(4)*	✓ *(6)*	Level shifter required	Level shifter required

Notes to Table 2–28:

(1) Input buffer is 3.3-V tolerant.
(2) The nCEO output buffer meets V_{OH} (MIN) = 2.4 V.
(3) Input buffer is 2.5-V tolerant.
(4) The nCEO output buffer meets V_{OH} (MIN) = 2.0 V.
(5) Input buffer is 1.8-V tolerant.
(6) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.

For JTAG chains, the TDO pin of the first device drives the TDI pin of the second device in the chain. The V_{CCSEL} input on JTAG input I/O cells (TCK, TMS, TDI, and TRST) is internally hardwired to GND selecting the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the TDO bank from the first device to match the V_{CCSEL} settings for TDI on the second device, but that may not be possible depending on the application. Table 2–29 contains board design recommendations to ensure proper JTAG chain operation.

Table 2–29. Supported TDO/TDI Voltage Combinations

Device	TDI Input Buffer Power	Arria GX TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Arria GX	Always V_{CCPD} (3.3 V)	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
Non-Arria GX	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–29:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Arria GX devices contain dedicated circuitry for supporting differential standards at speeds up to 840 Mbps. LVDS differential I/O standards are supported in the Arria GX device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO standard

There are two dedicated high-speed PLLs (PLL1 and PLL2) in the EP1AGX20 and EP1AGX35 devices and up to four dedicated high-speed PLLs (PLL1, PLL2, PLL7, and PLL8) in the EP1AGX50, EP1AGX60, and EP1AGX90 devices to multiply reference clocks and drive high-speed differential SERDES channels in I/O banks 1 and 2.

Table 2–30 through Table 2–34 list the number of channels that each fast PLL can clock in each of the Arria GX devices. In Table 2–30 through Table 2–34 the first row for each transmitter or receiver provides the maximum number of channels that each fast PLL can drive in its adjacent I/O bank (I/O Bank 1 **or** I/O Bank 2). The second row shows the maximum number of channels that each fast PLL can drive in both I/O banks (I/O Bank 1 **and** I/O Bank 2). For example, in the 780-pin FineLine BGA EP1AGX20

device, PLL 1 can drive a maximum of 16 transmitter channels in I/O Bank 2 or a maximum of 29 transmitter channels in I/O Banks 1 and 2. The Quartus II software can also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

For more information, refer to the "Differential Pin Placement Guidelines" section in the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

Table 2–30. EP1AGX20 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine GBA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

Note to Table 2–30:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–31. EP1AGX35 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

Note to Table 2–31:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–32. EP1AGX50 Device Differential Channels *(Note 1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
484-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
780-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
			21	21	—	—
	Receiver	42	21	21	21	21
			21	21	—	—

Note to Table 2–32:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–33. EP1AGX60 Device Differential Channels *(Note 1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
484-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
780-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
			21	21	—	—
	Receiver	42	21	21	21	21
			21	21	—	—

Note to Table 2–33:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–34. EP1AGX90 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs
			PLL1	PLL2	PLL7
1,152-pin FineLine BGA	Transmitter	45	23	22	23
			22	23	—
	Receiver	47	23	24	23
			24	23	—

Note to Table 2–34:

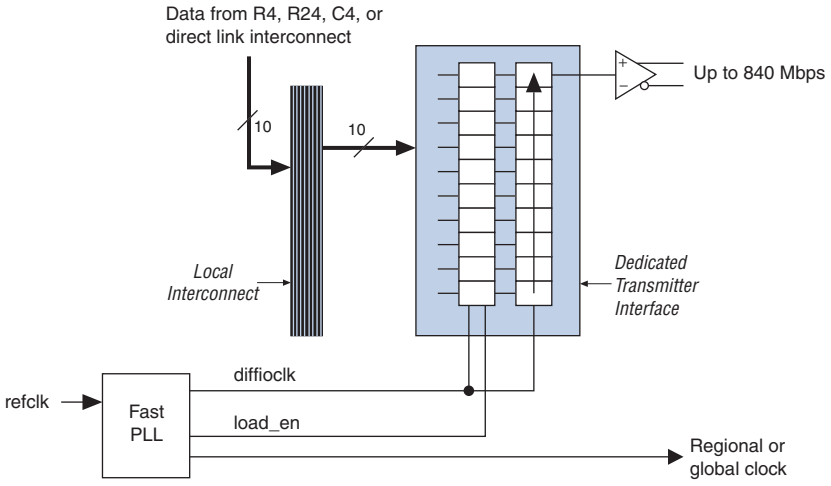
(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Dedicated Circuitry with DPA Support

Arria GX devices support source-synchronous interfacing with LVDS signaling at up to 840 Mbps. Arria GX devices can transmit or receive serial channels along with a low-speed or high-speed clock.

The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these J factor values. For a J factor of 1, the Arria GX device bypasses the SERDES block. For a J factor of 2, the Arria GX device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–79 shows the block diagram of the Arria GX transmitter channel.

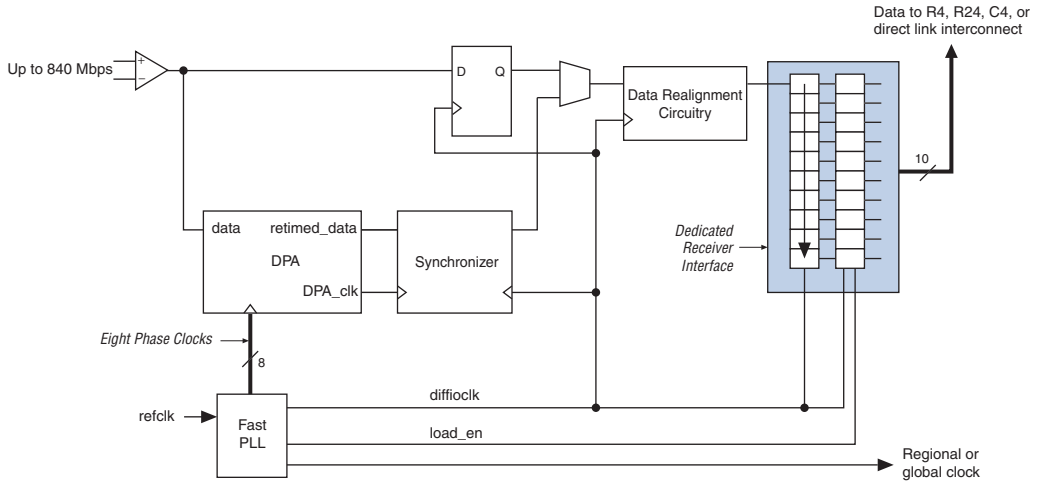
Figure 2–79. Arria GX Transmitter Channel



Each Arria GX receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array.

Figure 2–80 shows the block diagram of the Arria GX receiver channel.

Figure 2–80. GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the V_{CO} can feed to the DPA circuitry.

For more information about fast PLL, refer to the *PLLs in Arria GX Devices* chapter.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

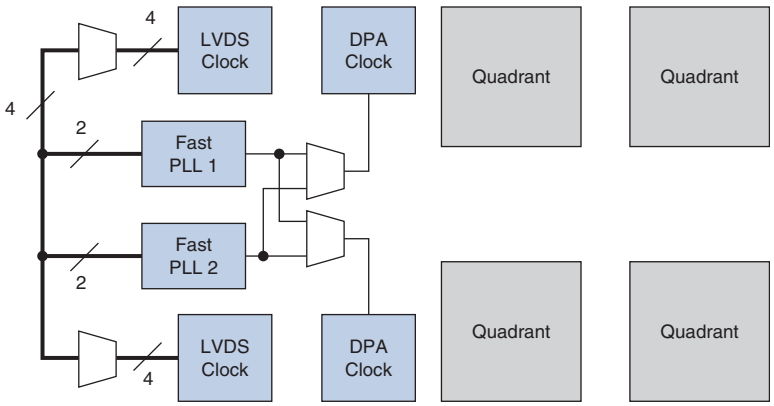
The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Because every channel using the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

For high-speed source-synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary as the clock is one half the data rate, not one eighth. The Arria GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved as such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–81 shows the fast PLL and channel layout in the EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D and EP1AGX60C/D devices. Figure 2–82 shows the fast PLL and channel layout in EP1AGX60E and EP1AGX90E devices.

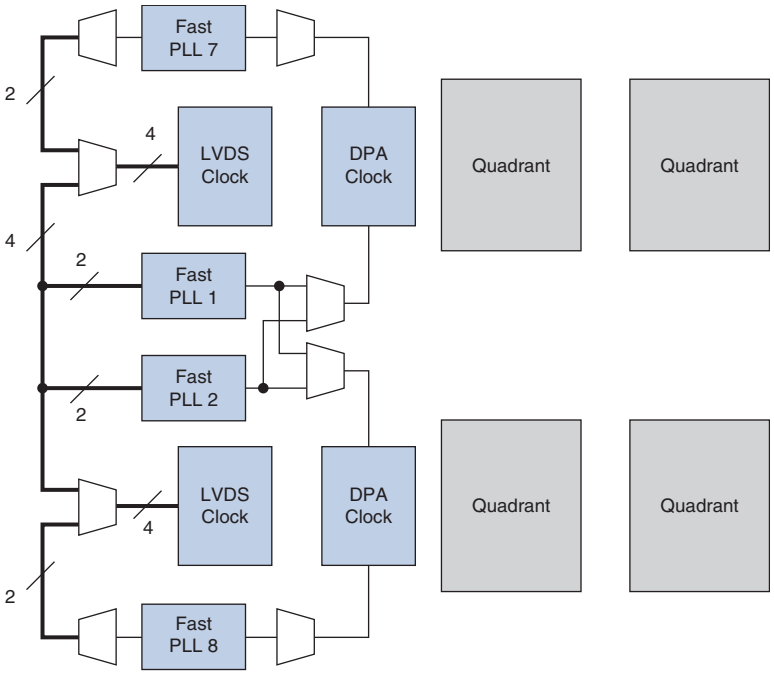
Figure 2–81. Fast PLL and Channel Layout in EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D, EP1AGX60C/D Devices *(Note 1)*



Note to Figure 2–81:

(1) For the number of channels each device supports, refer to Table 2–30.

Figure 2–82. Fast PLL and Channel Layout in EP1AGX60E and EP1AGX90E Devices *(Note 1)*



Note to Figure 2–82:

(1) For the number of channels each device supports, refer to Table 2–30 through Table 2–34.

Document Revision History

Table 2–35 shows the revision history for this chapter.

Table 2–35. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
May 2008, v1.3	Added "Reverse Serial Pre-CDR Loopback" and "Calibration Block" sub-sections to "Transmitter Path" section.	—
August 2007, v1.2	Added "Referenced Documents" section.	—
June 2007, v1.1	Added GIGE information.	—
May 2007 v1.0	Initial release.	—

3. Configuration and Testing

AGX51003-2.0

Introduction

All Arria® GX devices provide JTAG boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. You can perform JTAG boundary-scan testing either before or after, but not during configuration. Arria GX devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either jam files (**.jam**) or jam byte-code files (**.jbc**).

This chapter contains the following sections:

- "IEEE Std. 1149.1 JTAG Boundary-Scan Support"
- "SignalTap II Embedded Logic Analyzer" on page 3–3
- "Configuration" on page 3–3
- "Automated Single Event Upset (SEU) Detection" on page 3–8

IEEE Std. 1149.1 JTAG Boundary-Scan Support

Arria GX devices support I/O element (IOE) standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user-mode through the `CONFIG_IO` instruction. You can use this capability for JTAG testing before configuration when some of the Arria GX pins drive or receive from other devices on the board using voltage-referenced standards. Because the Arria GX device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming these I/O standards via JTAG allows you to fully test the I/O connections to other devices.

A device operating in JTAG mode uses four required pins, `TDI`, `TDO`, `TMS`, and `TCK`, and one optional pin, `TRST`. The `TCK` pin has an internal weak pull-down resistor, while the `TDI`, `TMS`, and `TRST` pins have weak internal pull-up resistors. The JTAG input pins are powered by the 3.3-V V_{CCPD} pins. The `TDO` output pin is powered by the V_{CCIO} power supply in I/O bank 4.

Arria GX devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Arria GX devices support the JTAG instructions shown in Table 3–1.

Arria GX, Cyclone® II, Cyclone, Stratix®, Stratix II, Stratix GX , and Stratix II GX devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix, Arria GX, Cyclone, and Cyclone II devices are in the 18th or further position, they will fail configuration. This does not affect the functionality of the SignalTap® II embedded logic analyzer.

Table 3–1. Arria GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring an Arria GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, EthernetBlaster™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner™.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information about using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices* White Paper.

The Arria GX device instruction register length is 10 bits and the USERCODE register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device IDCODE information for Arria GX devices.

Table 3–2. Arria GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1AGX20	1320
EP1AGX35	1320
EP1AGX50	1668
EP1AGX60	1668
EP1AGX90	2016

Table 3–3. 2-Bit Arria GX Device IDCODE

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit)
EP1AGX20	0000	0010 0001 0010 0001	000 0110 1110	1
EP1AGX35	0000	0010 0001 0010 0001	000 0110 1110	1
EP1AGX50	0000	0010 0001 0010 0010	000 0110 1110	1
EP1AGX60	0000	0010 0001 0010 0010	000 0110 1110	1
EP1AGX90	0000	0010 0001 0010 0011	000 0110 1110	1

SignalTap II Embedded Logic Analyzer

Arria GX devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA (FBGA) packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Arria GX architecture are configured with CMOS SRAM elements. Altera® FPGAs are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Arria GX devices are configured at system power up with data stored in an Altera configuration device or provided by an external controller (for example, a MAX® II device or microprocessor). You can configure Arria GX devices using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. Each Arria GX device has an optimized interface that allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Arria GX devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Arria GX devices also offer decompression and remote system upgrade features. The decompression feature allows Arria GX FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of Arria GX designs. For more information, refer to "Configuration Schemes" on page 3–5.

Operating Modes

The Arria GX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow you to reconfigure Arria GX devices in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, re-initializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select power-on reset (POR) delay times of 12 ms or 100 ms during power up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO_PULLUP pin is a dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-up resistors, while a logic low turns them on.

Arria GX devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_PULLUP, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The V_{CCSEL} pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO} voltage, you do not have to take the VIL and VIH levels driven to the configuration inputs into consideration. The configuration input pins, nCONFIG, DCLK (when used as an input), nIO_PULLUP, RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR, have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The V_{CCSEL} input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD}, while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}.

V_{CCSEL} is sampled during power up. Therefore, the V_{CCSEL} setting cannot change on-the-fly or during a reconfiguration. The V_{CCSEL} input buffer is powered by V_{CCINT} and must be hard-wired to V_{CCPD} or ground. A logic high V_{CCSEL} connection selects the 1.8-V/1.5-V input buffer, and a logic low selects the 3.3-V/2.5-V input buffer. V_{CCSEL} should be set to comply with the logic levels driven out of the configuration device or MAX II microprocessor.

If the design must support configuration input voltages of 3.3 V/2.5 V, set V_{CCSEL} to a logic low. You can set the V_{CCIO} voltage of the I/O bank that contains the configuration inputs to any supported voltage. If the design must support configuration input voltages of 1.8 V/1.5 V, set V_{CCSEL} to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information about multi-volt support, including information about using TDO and nCEO in multi-volt systems, refer to the *Arria GX Architecture* chapter.

Configuration Schemes

You can load the configuration data for an Arria GX device with one of five configuration schemes (refer to Table 3–4), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure an Arria GX device. A configuration device can automatically configure an Arria GX device at system power up.

You can configure multiple Arria GX devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Arria GX FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Remote system upgrades for remotely updating Arria GX designs

Table 3–4 lists which configuration features can be used in each configuration scheme.

For more information about configuration schemes in Arria GX devices, refer to the *Configuring Arria GX Devices* chapter.

Table 3–4. Arria GX Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ *(1)*	✓
	Enhanced configuration device	✓ *(2)*	✓
AS	Serial configuration device	✓	✓ *(3)*
PS	MAX II device or microprocessor and flash device	✓	✓
	Enhanced configuration device	✓	✓
	Download cable *(4)*	✓	—
PPA	MAX II device or microprocessor and flash device	—	✓

Table 3–4. Arria GX Configuration Features (Part 2 of 2)

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade
JTAG	Download cable *(4)*	—	—
	MAX II device or microprocessor and flash device	—	—

Notes for Table 3–4:

(1) In these modes, the host system must send a DCLK that is 4× the data rate.

(2) The enhanced configuration device decompression feature is available, while the Arria GX decompression feature is not available.

(3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.

(4) The supported download cables include the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, ByteBlasterMV parallel port download cable, and the EthernetBlaster download cable.

Device Configuration Data Decompression

Arria GX FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Arria GX FPGAs. During configuration, the Arria GX FPGA decompresses the bitstream in real time and programs its SRAM cells. Arria GX FPGAs support decompression in the FPP (when using a MAX II device or microprocessor and flash memory), AS, and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

Remote System Upgrades

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by system designers. Arria GX devices can help effectively deal with these challenges with their inherent re programmability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reduce time to market, and extend product life.

Arria GX FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios® processor or user logic) implemented in the Arria GX device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

Remote system configuration is supported in the following Arria GX configuration schemes: FPP, AS, PS, and PPA. You can also implement remote system configuration in conjunction with Arria GX features such as real-time decompression of configuration data for efficient field upgrades.

For more information about remote configuration in Arria GX devices, refer to the *Remote System Upgrades with Arria GX Devices* chapter.

Configuring Arria GX FPGAs with JRunner

The JRunner software driver configures Altera FPGAs, including Arria GX FPGAs, through the ByteBlaster™ II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information about the JRunner software driver, refer to the *AN414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website.

Programming Serial Configuration Devices with SRunner

You can program a serial configuration device in-system by an external microprocessor using SRunner™. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner software driver reads a raw programming data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner software driver is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Arria GX FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports a raw binary file (RBF) programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Arria GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

For more information about Arria GX PLLs, refer to the *PLLs in Arria GX Devices* chapter.

Automated Single Event Upset (SEU) Detection

Arria GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole requires periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device and Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Arria GX devices, eliminating the need for external logic. Arria GX devices compute CRC during configuration. The Arria GX device checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Arria GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

Beginning with version 7.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device and Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Arria GX FPGA.

For more information about CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGAs*.

Document Revision History

Table 3–5 lists the revision history for this chapter.

Table 3–5. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
May 2009 v1.4	■ Removed "Temperature Sensing Diode" section. ■ Updated Table 3–1 and Table 3–4.	—
May 2008 v1.3	Updated note in "Introduction" section.	
	Minor text edits.	—
August 2007 v1.2	Added the "Referenced Documents" section.	—
June 2007 v1.1	Deleted Signal Tap II information from Table 3–1.	—
May 2007 v1.0	Initial Release	—

AGX51004-2.0

Operating Conditions

Arria® GX devices are offered in both commercial and industrial grades. Both commercial and industrial devices are offered in –6 speed grade only.

This chapter contains the following sections:

- "Operating Conditions"
- "Power Consumption" on page 4–25
- "I/O Timing Model" on page 4–26
- "Typical Design Performance" on page 4–32
- "Block Performance" on page 4–84
- "IOE Programmable Delay" on page 4–86
- "Maximum Input and Output Clock Toggle Rate" on page 4–87
- "Duty Cycle Distortion" on page 4–95
- "High-Speed I/O Specifications" on page 4–100
- "PLL Timing Specifications" on page 4–103
- "External Memory Interface Specifications" on page 4–105
- "JTAG Timing Specifications" on page 4–106

Table 4–1 through Table 4–42 on page 4–25 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Arria GX devices.

Absolute Maximum Ratings

Table 4–1 contains the absolute maximum ratings for the Arria GX device family.

Table 4–1. Arria GX Device Absolute Maximum Ratings *(Note 1)*, *(2)*, *(3)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage *(4)*	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	C

Table 4–1. Arria GX Device Absolute Maximum Ratings *(Note 1)*, *(2)*, *(3)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction temperature	BGA packages under bias	–55	125	C

Notes to Table 4–1:

(1) For more information about operating requirements for Altera® devices, refer to the *Arria GX Device Family Data Sheet* chapter.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–2. Maximum Duty Cycles in Voltage Transitions *(Note 1)*

Symbol	Parameter	Condition	Maximum Duty Cycles (%)
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100
		V_I = 4.1 V	90
		V_I = 4.2 V	50
		V_I = 4.3 V	30
		V_I = 4.4 V	17
		V_I = 4.5 V	10

Note to Table 4–2:

(1) During transition, the inputs may overshoot to the voltages shown based on the input duty cycle. The DC case is equivalent to 100% duty cycle.

Recommended Operating Conditions

Table 4–3 lists the recommended operating conditions for the Arria GX device family.

Table 4–3. Arria GX Device Recommended Operating Conditions (Part 1 of 2) *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Rise time ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	Rise time ≤ 100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	Rise time ≤ 100 ms *(3)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	Rise time ≤ 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	Rise time ≤ 100 ms *(3)*	1.425	1.575	V
	Supply voltage for output buffers, 1.2-V operation	Rise time ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤ rise time ≤ 100 ms *(4)*	3.135	3.465	V
V_I	Input voltage (refer to Table 4–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V

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Table 4–3. Arria GX Device Recommended Operating Conditions (Part 2 of 2) *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Operating junction temperature	For commercial use	0	85	C
		For industrial use	–40	100	C

Notes to Table 4–3:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(2) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.

(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 µs to 100 ms. If V_{CCPD} is not ramped up within this specified time, the Arria GX device will not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, hold `nCONFIG` low until all power supplies are reliable.

(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, can be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.

(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

Transceiver Block Characteristics

Table 4–4 through Table 4–6 on page 4–4 contain transceiver block specifications.

Table 4–4. Arria GX Transceiver Block Absolute Maximum Ratings *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCR}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCL_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V

Note to Table 4–4:

(1) The device can tolerate prolonged operation at this absolute maximum, as long as the maximum specification is not violated.

Table 4–5. Arria GX Transceiver Block Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	3.135	3.3	3.465	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCR}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCL_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
			1.425	1.5	1.575	V
R_{REFB} *(1)*	Reference resistor	Commercial and industrial	2K - 1%	2K	2K +1%	Ω

Note to Table 4–5:

(1) The DC signal on this pin must be as clean as possible. Ensure that no noise is coupled to this pin.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 1 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Reference clock					
Input reference clock frequency	—	50	—	622.08	MHz
Absolute V_{MAX} for a REFCLK Pin	—	—	—	3.3	V
Absolute V_{MIN} for a REFCLK Pin	—	–0.3	—	—	V
Rise/Fall time	—	—	0.2	—	UI
Duty cycle	—	45	—	55	%
Peak to peak differential input voltage V_{ID} (diff p-p)	—	200	—	2000	mV
Spread spectrum clocking *(1)*	0 to –0.5%	30	—	33	kHz
On-chip termination resistors	—		115 ± 20%		Ω
V_{ICM} (AC coupled)	—		1200 ± 5%		mV
V_{ICM} (DC coupled) *(2)*	PCI Express (PIPE) mode	0.25	—	0.55	V
RREFB	—		2000 +/-1%		Ω
Transceiver Clocks					
Calibration block clock frequency	—	10	—	125	MHz
Calibration block minimum power-down pulse width	—	30	—	—	ns
fixedclk clock frequency *(3)*	—		125 ±10%		MHz
reconfig clock frequency	SDI mode	2.5	—	50	MHz
Transceiver block minimum power-down pulse width	—	100	—	—	ns
Receiver					
Data rate	—	600	—	3125	Mbps
Absolute V_{MAX} for a receiver pin *(4)*	—	—	—	2.0	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	Vicm = 0.85 V	—	—	3.3	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	DC Gain = 3 dB	160	—	—	mV
On-chip termination resistors	—		100±15%		Ω
V_{ICM} *(15)*	Vicm = 0.85 V setting	850 ± 10%	850 ± 10%	850 ± 10%	mV
	Vicm = 1.2 V setting	1200 ± 10%	1200 ± 10%	1200 ± 10%	mV
Bandwidth at 3.125 Gbps	BW = Low	—	30	—	MHz
	BW = Med	—	40	—	
	BW = High	—	50	—	

Table 4–6. Arria GX Transceiver Block AC Specification (Part 2 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Bandwidth at 2.5 Gbps	BW = Low	—	35	—	MHz
	BW = Med	—	50	—	
	BW = High	—	60	—	
Return loss differential mode	50 MHz to 1.25 GHz (PCI Express)	–10			dB
	100 MHz to 2.5 GHz (XAUI)				
Return loss common mode	50 MHz to 1.25 GHz (PCI Express)	–6			dB
	100 MHz to 2.5 GHz (XAUI)				
Programmable PPM detector *(5)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000			PPM
Run length *(6)*	—	80			UI
Programmable equalization	—	—	—	5	dB
Signal detect/loss threshold *(7)*	—	65	—	175	mV
CDR LTR TIme *(8)*, *(9)*	—	—	—	75	us
CDR Minimum T1b *(9)*, *(10)*	—	15	—	—	us
LTD lock time *(9)*, *(11)*	—	0	100	4000	ns
Data lock time from `rx_freqlocked` *(9)*, *(12)*	—	—	—	4	us
Programmable DC gain	—	0, 3, 6			dB
Transmitter Buffer					
Output Common Mode voltage (V_{ocm})	—	580 ± 10%			mV
On-chip termination resistors	—	108±10%			Ω
Return loss differential mode	50 MHz to 1.25 GHz (PCI Express)	–10			dB
	312 MHz to 625 MHz (XAUI)				
	625 MHz to 3.125GHz (XAUI)	–10			$\frac{dB}{decade\ slope}$
Return loss common mode	50 MHz to 1.25 GHz (PCI Express)	–6			dB
Rise time	—	35	—	65	ps
Fall time	—	35	—	65	ps
Intra differential pair skew	V_{OD} = 800 mV	—	—	15	ps
Intra-transceiver block skew (×4) *(13)*	—	—	—	100	ps

Table 4–6. Arria GX Transceiver Block AC Specification (Part 3 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Transmitter PLL					
VCO frequency range	—	500	—	1562.5	MHz
Bandwidth at 3.125 Gbps	BW = Low	—	3	—	MHz
	BW = Med	—	5	—	
	BW = High	—	9	—	
Bandwidth at 2.5 Gbps	BW = Low	—	1	—	MHz
	BW = Med	—	2	—	
	BW = High	—	4	—	
TX PLL lock time from `gxb_powerdown` de-assertion *(9)*, *(14)*	—	—	—	100	us
PCS					
Interface speed per mode	—	25	—	156.25	MHz
Digital Reset Pulse Width	—	Minimum is 2 parallel clock cycles			—

Notes to Table 4–6:

(1) Spread spectrum clocking is allowed only in PCI Express (PIPE) mode if the upstream transmitter and the receiver share the same clock source.
(2) The reference clock DC coupling option is only available in PCI Express (PIPE) mode for the HCSL I/O standard.
(3) The `fixedclk` is used in PIPE mode receiver detect circuitry.
(4) The device cannot tolerate prolonged operation at this absolute maximum.
(5) The rate matcher supports only up to ± 300 PPM for PIPE mode and ± 100 PPM for GIGE mode.
(6) This parameter is measured by embedding the run length data in a PRBS sequence.
(7) Signal detect threshold detector circuitry is available only in PCI Express (PIPE mode).
(8) Time taken for `rx_pll_locked` to go high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(9) For lock times specific to the protocols, refer to protocol characterization documents.
(10) Time for which the CDR needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(11) Time taken to recover valid data from GXB after the `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(12) Time taken to recover valid data from GXB after the `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–2.
(13) This is applicable only to PCI Express (PIPE) ×4 and XAUI ×4 mode.
(14) Time taken to lock `TX PLL` from `gxb_powerdown` deassertion.
(15) The 1.2 V RX VICM settings is intended for DC-coupled LVDS links.

Figure 4–1 shows the lock time parameters in manual mode. Figure 4–2 shows the lock time parameters in automatic mode.

LTD = Lock to data
LTR = Lock to reference clock

Figure 4–1. Lock Time Parameters for Manual Mode

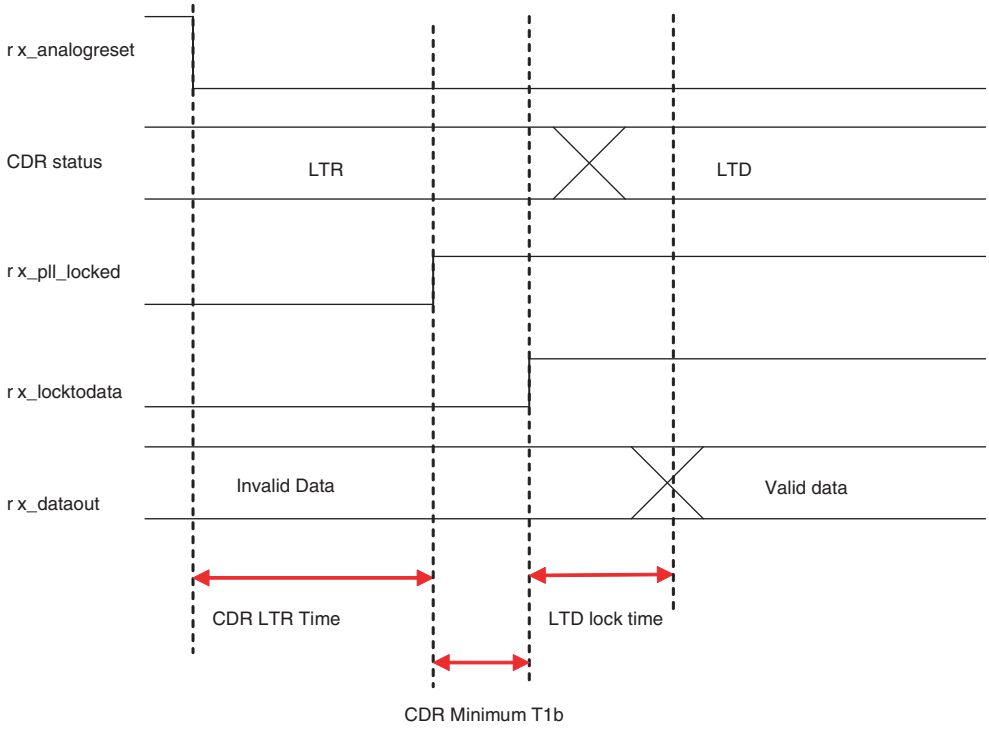


Figure 4–2. Lock Time Parameters for Automatic Mode

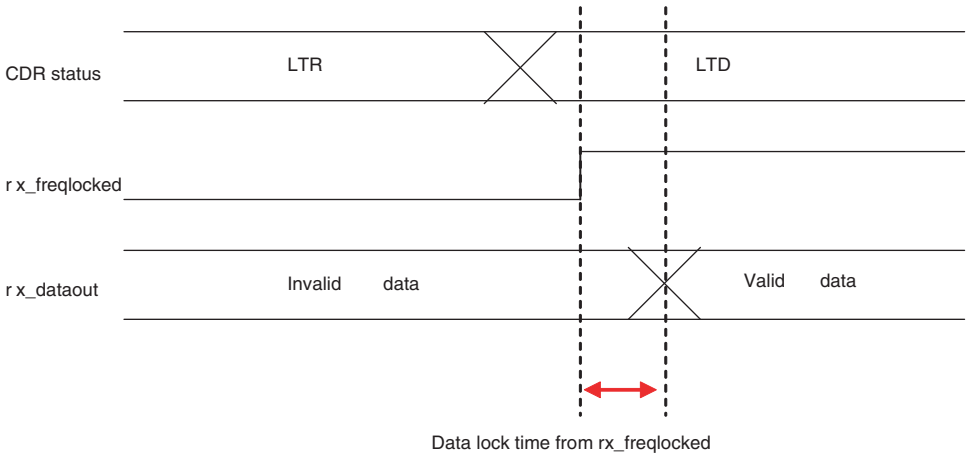


Figure 4–3 and Figure 4–4 show differential receiver input and transmitter output waveforms, respectively.

Figure 4–3. Receiver Input Waveform

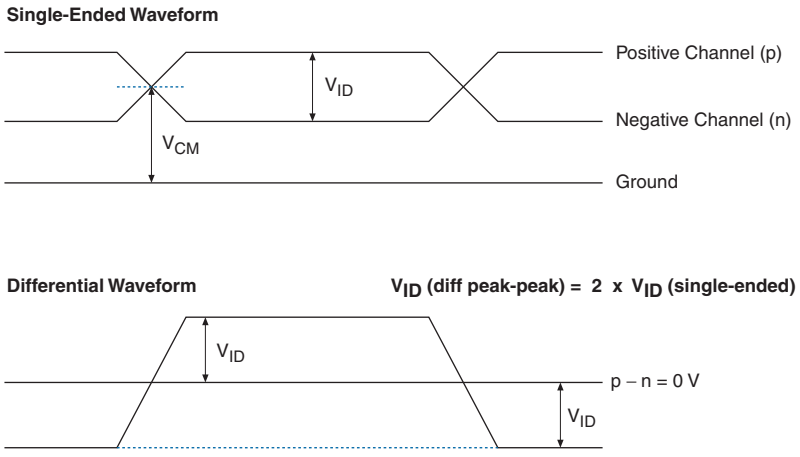


Figure 4–4. Transmitter Output Waveform

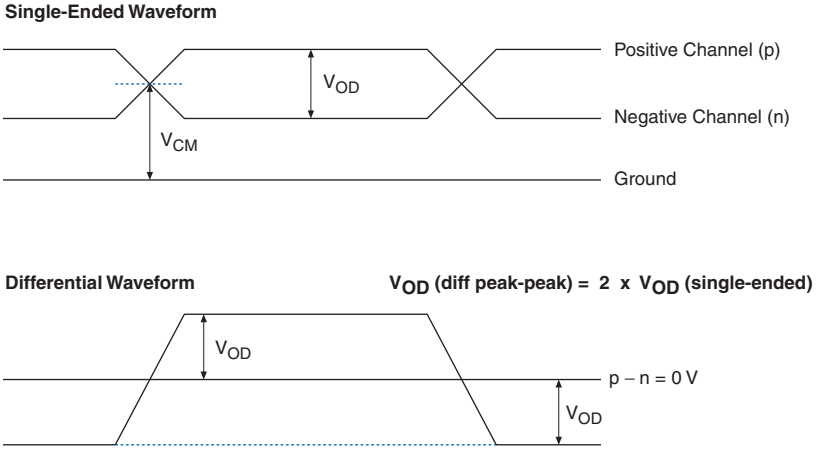


Table 4–7 lists the Arria GX transceiver block AC specification.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1)*, *(2)*, *(3)* (Part 1 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
XAUI Transmit Jitter Generation *(4)*			
Total jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.3	UI

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1)*, *(2)*, *(3)* (Part 2 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*			
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65	UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1	UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1	UI
PCI Express (PIPE) Transmitter Jitter Generation *(5)*			
Total Transmitter Jitter Generation	Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 49%	< 0.25	UI p-p
PCI Express (PIPE) Receiver Jitter Tolerance *(5)*			
Total Receiver Jitter Tolerance	Compliance Pattern; DC Gain = 3 db	> 0.6	UI p-p
Gigabit Ethernet (GIGE) Transmitter Jitter Generation *(7)*			
Total Transmitter Jitter Generation (TJ)	CRPAT: V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.279	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CRPAT; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.14	UI p-p
Gigabit Ethernet (GIGE) Receiver Jitter Tolerance			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.66	UI p-p
Deterministic Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.4	UI p-p
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Transmitter Jitter Generation *(6)*			
Total Transmitter Jitter Generation (TJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.35	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.17	UI p-p

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1)*, *(2)*, *(3)* (Part 3 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Receiver Jitter Tolerance *(6)*			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.65	UI p-p
Combined Deterministic and Random Jitter Tolerance (J_{DR})	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.55	UI p-p
Deterministic Jitter Tolerance (J_D)	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.37	UI p-p
Sinusoidal Jitter Tolerance	Jitter Frequency = 22.1 KHz	> 8.5	UI p-p
	Jitter Frequency = 200 KHz	> 1.0	UI p-p
	Jitter Frequency = 1.875 MHz	> 0.1	UI p-p
	Jitter Frequency = 20 MHz	> 0.1	UI p-p
SDI Transmitter Jitter Generation *(8)*			
Alignment Jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.2	UIv
	Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.3	UI

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1)*, *(2)*, *(3)* (Part 4 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
SDI Receiver Jitter Tolerance *(8)*			
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB	> 2	UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB	> 0.3	UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB	> 0.3	UI
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB	> 1	UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB	> 0.2	UI

Notes to Table 4–7:

(1) Dedicated REFCLK pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) Refer to the protocol characterization documents for detailed information.
(4) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(5) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(6) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(7) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(8) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M specifications.

Table 4–8 and Table 4–9 list the transmitter and receiver PCS latency for each mode, respectively.

Table 4–8. PCS Latency *(Note 1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI	—	—	2–3	1	0.5	0.5	4–5
PIPE	×1, ×4, ×8 8-bit channel width	1	3–4	1	—	1	6–7
	×1, ×4, ×8 16-bit channel width	1	3–4	1	—	0.5	6–7
GIGE	—	—	2–3	1	—	1	4–5
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	—	2–3	1	—	0.5	4–5
SDI	HD10-bit channel width	—	2–3	1	—	1	4–5
	HD, 3G 20-bit channel width	—	2–3	1	—	0.5	4–5
BASIC Single Width	8-bit/10-bit channel width	—	2–3	1	—	1	4–5
	16-bit/20-bit channel width	—	2–3	1	—	0.5	4–5

Notes to Table 4–8:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

Table 4–9. PCS Latency (Part 1 of 2) (Part 1 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
XAUI	—	2–2.5	2–2.5	5.5–6.5	0.5	1	1	1	1–2	—	14–17
PIPE	×1, ×4 8-bit channel width	4–5	—	11–13	1	—	1	1	2–3	1	21–25
	×1, ×4 16-bit channel width	2–2.5	—	5.5–6.5	0.5	—	1	1	2–3	1	13–16
GIGE	—	4–5	—	11–13	1	—	1	1	1–2	—	19–23
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7
SDI	HD 10-bit channel width	5	—	—	1	—	1	1	1–2	—	9–10
	HD, 3G 20-bit channel width	2.5	—	—	0.5	—	1	1	1–2	—	6–7

Table 4–9. PCS Latency (Part 2 of 2) (Part 2 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher (3)	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum (2)
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4–5	—	11–13	1	—	1	1	1–2	1	19–23
	8/10-bit channel width; without Rate Matcher	4–5	—	—	1	—	1	1	1–2	—	8–10
	16/20-bit channel width; with Rate Matcher	2–2.5	—	5.5–6.5	0.5	—	1	1	1–2	—	11–14
	16/20-bit channel width; without Rate Matcher	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7

Notes to Table 4–9:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.

Table 4–10 through Table 4–13 show the typical V_{OD} for data rates from 600 Mbps to 3.125 Gbps. The specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.5 V	V_{OD} Setting (mV)				
	400	600	800	1000	1200
V_{OD} Typical (mV)	430	625	830	1020	1200

Table 4–11. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.2 V	V_{OD} Setting (mV)				
	320	480	640	800	960
V_{OD} Typical (mV)	344	500	664	816	960

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
400	24%	62%	112%	184%	—
600	—	31%	56%	86%	122%
800	—	20%	35%	53%	73%

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
1000	—	—	23%	36%	49%
1200	—	—	17%	25%	35%

Note to Table 4–12:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.2 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
320	24%	61%	114%	—	—
480	—	31%	55%	86%	121%
640	—	20%	35%	54%	72%
800	—	—	23%	36%	49%
960	—	—	18%	25%	35%

Note to Table 4–13:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

DC Electrical Characteristics

Table 4–14 lists the Arria GX device family DC electrical characteristics.

Table 4–14. Arria GX Device DC Operating Conditions (Part 1 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	0.30	*(3)*	A
			EP1AGX50/60	—	0.50	*(3)*	A
			EP1AGX90	—	0.62	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP1AGX20/35	—	2.7	*(3)*	mA
			EP1AGX50/60	—	3.6	*(3)*	mA
			EP1AGX90	—	4.3	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	4.0	*(3)*	mA
			EP1AGX50/60	—	4.0	*(3)*	mA
			EP1AGX90	—	4.0	*(3)*	mA

Table 4–14. Arria GX Device DC Operating Conditions (Part 2 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	V_i = 0, V_{CCIO} = 3.3 V	—	10	25	50	kΩ
		V_i = 0, V_{CCIO} = 2.5 V	—	15	35	70	kΩ
		V_i = 0, V_{CCIO} = 1.8 V	—	30	50	100	kΩ
		V_i = 0, V_{CCIO} = 1.5 V	—	40	75	150	kΩ
		V_i = 0, V_{CCIO} = 1.2 V	—	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	—	1	2	kΩ

Notes to Table 4–14:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) Maximum values depend on the actual TJ and design utilization. For maximum values, refer to the Excel-based PowerPlay Early Power Estimator (available at PowerPlay Early Power Estimators (EPE) and Power Analyzer) or the Quartus® II PowerPlay Power Analyzer feature for maximum values. For more information, refer to "Power Consumption" on page 4–25.

(4) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 4–15 through Table 4–38 show the Arria GX device family I/O standard specifications.

Table 4–15. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4	—	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*	—	0.45	V

Notes to Table 4–15:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard.

Table 4–16. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*	—	0.2	V

Notes to Table 4–16:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard.

Table 4–17. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1 mA *(2)*	2.0	—	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*	—	0.4	V

Notes to Table 4–17:

(1) The Arria GX device V_{CCIO} voltage level support of 2.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard.

Table 4–18. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.45	V

Notes to Table 4–18:

(1) The Arria GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in *Arria GX Architecture* chapter.

Table 4–19. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.25 V_{CCIO}	V

Notes to Table 4–19:

(1) The Arria GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Figure 4–5 and Figure 4–6 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4–5. Receiver Input Waveforms for Differential I/O Standards

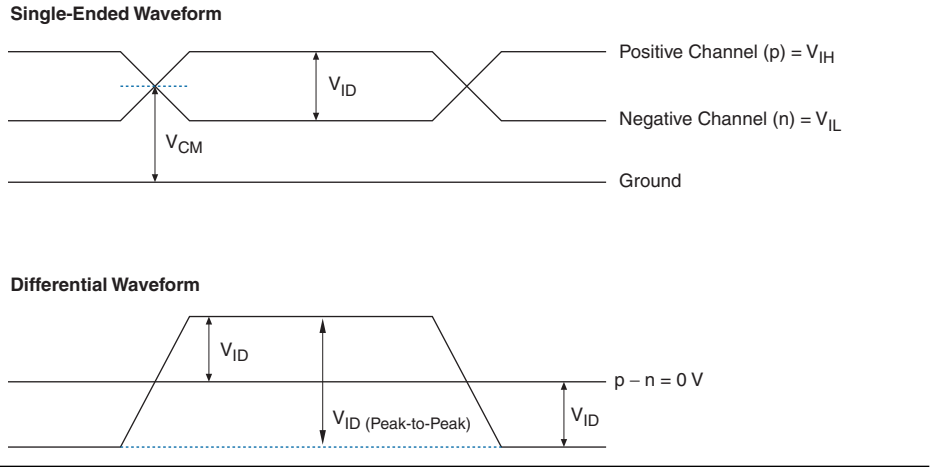


Figure 4–6. Transmitter Output Waveforms for Differential I/O Standards

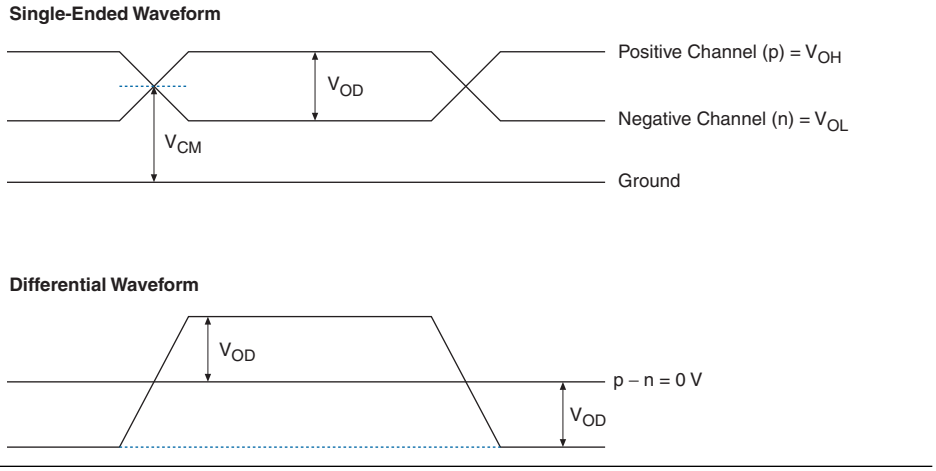


Table 4–20. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)	—	2.375	2.5	2.625	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125	—	1.375	V
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Table 4–21. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840	—	1,570	mV
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Note to Table 4–21:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–22. 3.3-V PCML Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	300	—	600	mV
V_{ICM}	Input common mode voltage	1.5	—	3.465	V
V_{OD}	Output differential voltage (single-ended)	300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	50	mV
V_{OCM}	Output common mode voltage	2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low	—	—	50	mV
V_T	Output termination voltage	—	V_{CCIO}	—	V
R_1	Output external pull-up resistors	45	50	55	Ω
R_2	Output external pull-up resistors	45	50	55	Ω

Table 4–23. LVPECL Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units	Parameter
V_{CCIO} *(1)*	I/O supply voltage	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	300	600	1,000	mV
V_{ICM}	Input common mode voltage	—	1.0	—	2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	—	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650	—	2,250	mV
R_L	Receiver differential input resistor	—	90	100	110	Ω

Note to Table 4–23:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–24. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	—	0.3 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 V_{CCIO}	V

Table 4–25. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{IPU}	Input pull-up voltage	—	0.7 V_{CCIO}	—	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	0.1 V_{CCIO}	V

Table 4–26. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*	—	—	V_{TT} – 0.475	V

Note to Table 4–26:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*	—	—	0.28	V

Note to Table 4–27:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–28. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.71	1.8	1.89	V
V_{SWING} (DC)	DC differential input voltage	0.25	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.175	—	(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage	0.5	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential cross point voltage	(V_{CCIO}/2) – 0.125	—	(V_{CCIO}/2) + 0.125	V

Table 4–29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	3.0	V
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57	—		V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*	—	—	V_{TT} – 0.57	V

Note to Table 4–29:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–30. SSTL-2 Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V

Table 4–30. SSTL-2 Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*	—	—	V_{TT} – 0.76	V

Note to Table 4–30:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–31. SSTL-2 Class I & II Differential Specifications *(Note 1)*

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	2.375	2.5	2.625	V
V_{SWING} (DC)	DC differential input voltage	0.36	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V
V_{SWING} (AC)	AC differential input voltage	0.7	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential output cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V

Note to Table 4–31:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–32. 1.2-V HSTL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.14	1.2	1.26	V
V_{REF}	Reference voltage	0.48 V_{CCIO}	0.5 V_{CCIO}	0.52 V_{CCIO}	V
V_{IH} (DC)	High-level DC input voltage	V_{REF} + 0.08	—	V_{CCIO} + 0.15	V
V_{IL} (DC)	Low-level DC input voltage	–0.15	—	V_{REF} – 0.08	V
V_{IH} (AC)	High-level AC input voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.24	V
V_{IL} (AC)	Low-level AC input voltage	–0.24	—	V_{REF} – 0.15	V
V_{OH}	High-level output voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.15	V
V_{OL}	Low-level output voltage	–0.15	—	V_{REF} – 0.15	V

Table 4–33. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.425	1.5	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*	—	—	0.4	V

Note to Table 4–33:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–34. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.425	1.50	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*	—	—	0.4	V

Note to Table 4–34:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Table 4–35. 1.5-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage	0.2	—	—	V
V_{CM} (DC)	DC common mode input voltage	0.68	—	0.9	V
V_{DIF} (AC)	AC differential input voltage	0.4	—	—	V
V_{OX} (AC)	AC differential cross point voltage	0.68	—	0.9	V

Table 4–36. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.80	1.89	V
V_{REF}	Input reference voltage	—	0.85	0.90	0.95	V
V_{TT}	Termination voltage	—	0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*	—	—	0.4	V

Note to Table 4–36:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Table 4–37. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.80	1.89	V
V_{REF}	Input reference voltage	—	0.85	0.90	0.95	V
V_{TT}	Termination voltage	—	0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*	—	—	0.4	V

Note to Table 4–37:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter in volume 1 of the *Arria GX Device Handbook*.

Table 4–38. 1.8-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage	0.2	—	—	V
V_{CM} (DC)	DC common mode input voltage	0.78	—	1.12	V
V_{DIF} (AC)	AC differential input voltage	0.4	—	—	V
V_{OX} (AC)	AC differential cross point voltage	0.68	—	0.9	V

Bus Hold Specifications

Table 4–39 shows the Arria GX device family bus hold specifications.

Table 4–39. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Units
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V <$V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < $V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	—	0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Table 4–40 and Table 4–41 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–40. Series On-Chip Termination Specification for Top and Bottom I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Units
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	± 30	%
25-Ω R_S 1.8	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8V	±30	±30	%
50-Ω R_S 1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	±36	%
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2V	±50	±50	%

Table 4–41. Series On-Chip Termination Specification for Left I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Units
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	±30	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	±36	%
R_D	Internal differential termination for LVDS (100-Ω setting)	V_{CCIO} = 2.5V	±20	±25	%

Pin Capacitance

Table 4–42 shows the Arria GX device family pin capacitance.

Table 4–42. Arria GX Device Capacitance *(Note 1)*

Symbol	Parameter	Typical	Units
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.	5.0	pF
C_{IOL}	Input capacitance on I/O pins in I/O banks 1 and 2, including high-speed differential receiver and transmitter pins.	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.	6.0	pF
C_{CLKL}	Input capacitance on left clock inputs: `CLK0` and `CLK2`.	6.1	pF
C_{CLKL+}	Input capacitance on left clock inputs: `CLK1` and `CLK3`.	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 11 and 12.	6.7	pF

Note to Table 4–42:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay Early Power Estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

For more information about PowerPlay tools, refer to the *PowerPlay Early Power Estimator and PowerPlay Power Analyzer* page and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

For typical I_{CC} standby specifications, refer to Table 4–14 on page 4–14 .

I/O Timing Model

The DirectDrive technology and MultiTrack interconnect ensures predictable performance, accurate simulation, and accurate timing analysis across all Arria GX device densities and speed grades. This section describes and specifies the performance of I/Os.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.1.

Preliminary, Correlated, and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during design compilation if the timing models are preliminary. Table 4–43 lists the status of the Arria GX device timing models.

- **Preliminary** status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.
- **Correlated** numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.
- **Final timing** numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Arria GX family devices have been completely characterized and no further changes to the timing model are expected.

Table 4–43. Arria GX Device Timing Model Status

Device	Preliminary	Correlated	Final
EP1AGX20	—	—	✓
EP1AGX35	—	—	✓
EP1AGX50	—	—	✓
EP1AGX60	—	—	✓
EP1AGX90	—	—	✓

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–44.

Use the following equations to calculate clock pin to output pin timing for Arria GX devices:

Equation 4–1.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

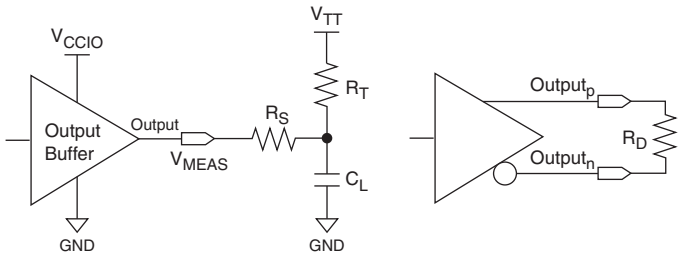
t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–44.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 4–44 using the above equation. Figure 4–7 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 4–7. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–7:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*	—	—	—	3.135	—	0	1.5675
LVCMOS *(4)*	—	—	—	3.135	—	0	1.5675
2.5 V *(4)*	—	—	—	2.375	—	0	1.1875
1.8 V *(4)*	—	—	—	1.710	—	0	0.855
1.5 V *(4)*	—	—	—	1.425	—	0	0.7125
PCI *(5)*	—	—	—	2.970	—	10	1.485
PCI-X *(5)*	—	—	—	2.970	—	10	1.485
SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
SSTL-18 Class I	25	—	50	1.660	0.790	0	0.83
SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.8-V HSTL Class I	—	—	50	1.660	0.790	0	0.83
1.8-V HSTL Class II	—	—	25	1.660	0.790	0	0.83
1.5-V HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	—	—	—	1.140	—	0	0.570
Differential SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50	—	50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.5-V differential HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V differential HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.8-V differential HSTL Class I	—	—	50	1.660	0.790	0	0.83

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

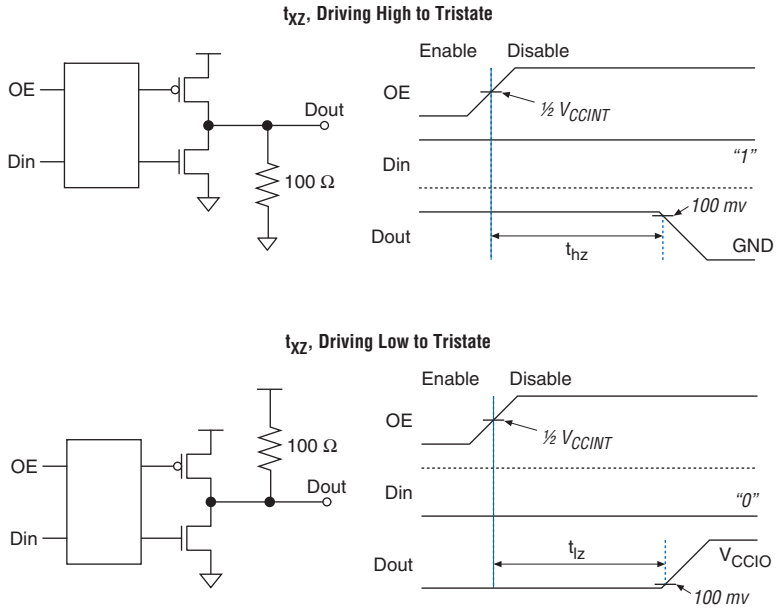
I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
1.8-V differential HSTL Class II	—	—	25	1.660	0.790	0	0.83
LVDS	—	100	—	2.325	—	0	1.1625
LVPECL	—	100	—	3.135	—	0	1.5675

Notes to Table 4–44:

(1) Input measurement point at internal node is 0.5 V_{CCINT}.
(2) Output measuring point for V_{MEAS} at buffer output is 0.5 V_{CCIO}.
(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Figure 4–8 and Figure 4–9 show the measurement setup for output disable and output enable timing.

Figure 4–8. Measurement Setup for t_{xz} *(Note 1)*



Note to Figure 4–8:

(1) V_{CCINT} is 1.12 V for this measurement.

Figure 4–9. Measurement Setup for t_{zx}

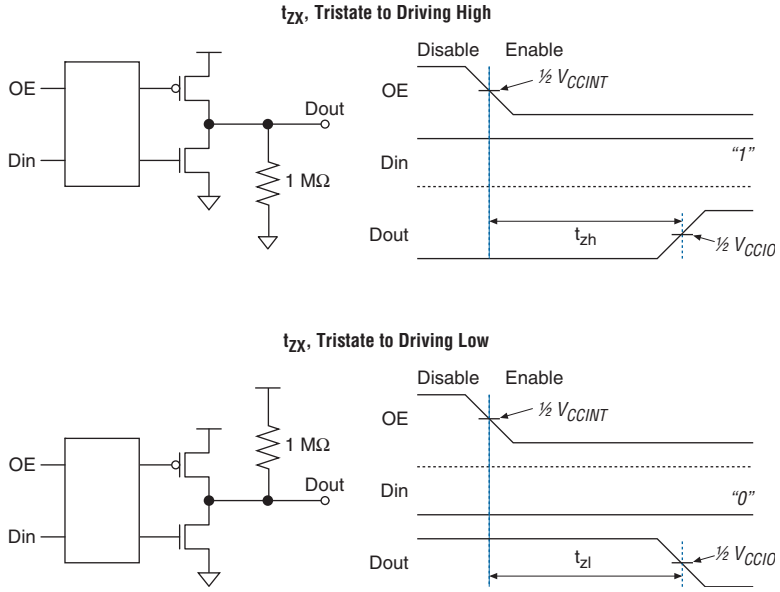


Table 4–45 specifies the input timing measurement setup.

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 1 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135	—	3.135	1.5675
LVCMOS *(5)*	3.135	—	3.135	1.5675
2.5 V *(5)*	2.375	—	2.375	1.1875
1.8 V *(5)*	1.710	—	1.710	0.855
1.5 V *(5)*	1.425	—	1.425	0.7125
PCI *(6)*	2.970	—	2.970	1.485
PCI-X *(6)*	2.970	—	2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 2 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325	—	0.100	1.1625
LVPECL	3.135	—	0.100	1.5675

Notes to Table 4–45:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–46 specifies the intra clock skew between any two clock networks driving any registers in the Arria GX device.

Table 4–46. Clock Network Specifications

Name	Description	Min	Typ	Max	Units
Clock skew adder EP1AGX20/35 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX50/60 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX90 *(1)*	Inter-clock network, same side	—	—	± 55	ps
	Inter-clock network, entire chip	—	—	± 110	ps

Note to Table 4–46:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–47 for default capacitive loading of different I/O standards.

Table 4–47. Default Loading of Different I/O Standards for Arria GX Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Units
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF

Table 4–47. Default Loading of Different I/O Standards for Arria GX Devices (Part 2 of 2)

I/O Standard	Capacitive Load	Units
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.5-V differential HSTL Class I	0	pF
1.5-V differential HSTL Class II	0	pF
1.8-V differential HSTL Class I	0	pF
1.8-V differential HSTL Class II	0	pF
LVDS	0	pF

Typical Design Performance

The following section describes the typical design performance for the Arria GX device family.

User I/O Pin Timing

Table 4–48 through Table 4–77 show user I/O pin timing for Arria GX devices. I/O buffer t_{SU}, t_H, and t_{CO} are reported for the cases when I/O clock is driven by a non-PLL global clock (GCLK) and a PLL driven global clock (GCLK-PLL). For t_{SU}, t_H, and t_{CO} using regional clock, add the value from the adder tables listed for each device to the GCLK/GCLK-PLL values for the device.

EP1AGX20 I/O Timing Parameters

Table 4–48 through Table 4–51 show the maximum I/O timing parameters for EP1AGX20 devices for I/O standards which support general purpose I/O pins.

Table 4–48 describes the row pin delay adders when using the regional clock in Arria GX devices.

Table 4–48. EP1AGX20 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.117	0.117	0.273	ns
RCLK PLL input adder	0.011	0.011	0.019	ns
RCLK output adder	–0.117	–0.117	–0.273	ns
RCLK PLL output adder	–0.011	–0.011	–0.019	ns

Table 4–49 describes I/O timing specifications.

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_{H}	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_{H}	–2.425	–2.425	–5.287	ns

Table 4–50 describes I/O timing specifications.

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–51 describes I/O timing specifications.

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.909	2.909	6.541	ns
		GCLK PLL	t_{CO}	1.467	1.467	3.435	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.697	2.697	6.169	ns
		GCLK PLL	t_{CO}	1.255	1.255	3.063	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.671	2.671	6.000	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.894	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.649	2.649	5.875	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.769	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.642	2.642	5.877	ns
		GCLK PLL	t_{CO}	1.200	1.200	2.771	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.672	2.672	5.874	ns
		GCLK PLL	t_{CO}	1.230	1.230	2.768	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.644	2.644	5.796	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.690	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.651	2.651	5.764	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.658	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.638	2.638	5.746	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.640	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.627	2.627	5.724	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.618	ns
2.5 V	4 mA	GCLK	t_{CO}	2.726	2.726	6.201	ns
		GCLK PLL	t_{CO}	1.284	1.284	3.095	ns
2.5 V	8 mA	GCLK	t_{CO}	2.674	2.674	5.939	ns
		GCLK PLL	t_{CO}	1.232	1.232	2.833	ns
2.5 V	12 mA	GCLK	t_{CO}	2.653	2.653	5.822	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.716	ns
2.5 V	16 mA	GCLK	t_{CO}	2.635	2.635	5.748	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.642	ns
1.8 V	2 mA	GCLK	t_{CO}	2.766	2.766	7.193	ns
		GCLK PLL	t_{CO}	1.324	1.324	4.087	ns
1.8 V	4 mA	GCLK	t_{CO}	2.771	2.771	6.419	ns
		GCLK PLL	t_{CO}	1.329	1.329	3.313	ns

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.695	2.695	6.155	ns
		GCLK PLL	t_{CO}	1.253	1.253	3.049	ns
1.8 V	8 mA	GCLK	t_{CO}	2.697	2.697	6.064	ns
		GCLK PLL	t_{CO}	1.255	1.255	2.958	ns
1.8 V	10 mA	GCLK	t_{CO}	2.651	2.651	5.987	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.881	ns
1.8 V	12 mA	GCLK	t_{CO}	2.652	2.652	5.930	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.824	ns
1.5 V	2 mA	GCLK	t_{CO}	2.746	2.746	6.723	ns
		GCLK PLL	t_{CO}	1.304	1.304	3.617	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	6.154	ns
		GCLK PLL	t_{CO}	1.240	1.240	3.048	ns
1.5 V	6 mA	GCLK	t_{CO}	2.685	2.685	6.036	ns
		GCLK PLL	t_{CO}	1.243	1.243	2.930	ns
1.5 V	8 mA	GCLK	t_{CO}	2.644	2.644	5.983	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.877	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.629	2.629	5.762	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.650	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.712	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.600	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.590	2.590	5.639	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.527	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.591	2.591	5.626	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.514	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.609	2.609	5.603	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.491	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.605	2.605	5.611	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.499	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.605	2.605	5.609	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.497	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.664	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.558	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.634	2.634	5.649	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.537	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.612	2.612	5.638	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.526	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.616	2.616	5.644	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.532	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.637	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.525	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.591	2.591	5.401	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.289	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.593	2.593	5.412	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.300	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.593	2.593	5.421	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.309	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.663	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.633	2.633	5.641	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.529	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.615	2.615	5.643	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.531	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.615	2.615	5.645	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.533	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.609	2.609	5.643	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.531	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.596	2.596	5.455	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.343	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.599	2.599	5.465	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.353	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.601	2.601	5.478	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.366	ns

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V PCI	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–52 through Table 4–53 list EP1AGX20 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–52 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–52. EP1AGX20 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.117	0.117	0.273	ns
RCLK PLL input adder	0.011	0.011	0.019	ns
RCLK output adder	–0.117	–0.117	–0.273	ns
RCLK PLL output adder	–0.011	–0.011	–0.019	ns

Table 4–53 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–53. EP1AGX20 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.081	0.081	0.223	ns
RCLK PLL input adder	–0.012	–0.012	–0.008	ns
RCLK output adder	–0.081	–0.081	–0.224	ns
RCLK PLL output adder	1.11	1.11	2.658	ns

EP1AGX35 I/O Timing Parameters

Table 4–54 through Table 4–57 list the maximum I/O timing parameters for EP1AGX35 devices for I/O standards which support general purpose I/O pins.

Table 4–54 lists I/O timing specifications.

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.561	1.561	3.556	ns
		t_H	–1.456	–1.456	–3.279	ns
	GCLK PLL	t_{SU}	2.980	2.980	6.628	ns
		t_H	–2.875	–2.875	–6.351	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.561	1.561	3.556	ns
		t_H	–1.456	–1.456	–3.279	ns
	GCLK PLL	t_{SU}	2.980	2.980	6.628	ns
		t_H	–2.875	–2.875	–6.351	ns
2.5 V	GCLK	t_{SU}	1.573	1.573	3.537	ns
		t_H	–1.468	–1.468	–3.260	ns
	GCLK PLL	t_{SU}	2.992	2.992	6.609	ns
		t_H	–2.887	–2.887	–6.332	ns
1.8 V	GCLK	t_{SU}	1.639	1.639	3.744	ns
		t_H	–1.534	–1.534	–3.467	ns
	GCLK PLL	t_{SU}	3.058	3.058	6.816	ns
		t_H	–2.953	–2.953	–6.539	ns
1.5 V	GCLK	t_{SU}	1.642	1.642	3.839	ns
		t_H	–1.537	–1.537	–3.562	ns
	GCLK PLL	t_{SU}	3.061	3.061	6.911	ns
		t_H	–2.956	–2.956	–6.634	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.385	1.385	3.009	ns
		t_H	–1.280	–1.280	–2.732	ns
	GCLK PLL	t_{SU}	2.804	2.804	6.081	ns
		t_H	–2.699	–2.699	–5.804	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.385	1.385	3.009	ns
		t_H	–1.280	–1.280	–2.732	ns
	GCLK PLL	t_{SU}	2.804	2.804	6.081	ns
		t_H	–2.699	–2.699	–5.804	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-18 CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–55 lists I/O timing specifications.

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–56 lists I/O timing specifications.

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–57 lists I/O timing specifications.

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.909	2.909	6.541	ns
		GCLK PLL	t_{CO}	1.467	1.467	3.435	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.697	2.697	6.169	ns
		GCLK PLL	t_{CO}	1.255	1.255	3.063	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.671	2.671	6.000	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.894	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.649	2.649	5.875	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.769	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.642	2.642	5.877	ns
		GCLK PLL	t_{CO}	1.200	1.200	2.771	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.672	2.672	5.874	ns
		GCLK PLL	t_{CO}	1.230	1.230	2.768	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.644	2.644	5.796	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.690	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.651	2.651	5.764	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.658	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.638	2.638	5.746	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.640	ns

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.627	2.627	5.724	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.618	ns
2.5 V	4 mA	GCLK	t_{CO}	2.726	2.726	6.201	ns
		GCLK PLL	t_{CO}	1.284	1.284	3.095	ns
2.5 V	8 mA	GCLK	t_{CO}	2.674	2.674	5.939	ns
		GCLK PLL	t_{CO}	1.232	1.232	2.833	ns
2.5 V	12 mA	GCLK	t_{CO}	2.653	2.653	5.822	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.716	ns
2.5 V	16 mA	GCLK	t_{CO}	2.635	2.635	5.748	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.642	ns
1.8 V	2 mA	GCLK	t_{CO}	2.766	2.766	7.193	ns
		GCLK PLL	t_{CO}	1.324	1.324	4.087	ns
1.8 V	4 mA	GCLK	t_{CO}	2.771	2.771	6.419	ns
		GCLK PLL	t_{CO}	1.329	1.329	3.313	ns
1.8 V	6 mA	GCLK	t_{CO}	2.695	2.695	6.155	ns
		GCLK PLL	t_{CO}	1.253	1.253	3.049	ns
1.8 V	8 mA	GCLK	t_{CO}	2.697	2.697	6.064	ns
		GCLK PLL	t_{CO}	1.255	1.255	2.958	ns
1.8 V	10 mA	GCLK	t_{CO}	2.651	2.651	5.987	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.881	ns
1.8 V	12 mA	GCLK	t_{CO}	2.652	2.652	5.930	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.824	ns
1.5 V	2 mA	GCLK	t_{CO}	2.746	2.746	6.723	ns
		GCLK PLL	t_{CO}	1.304	1.304	3.617	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	6.154	ns
		GCLK PLL	t_{CO}	1.240	1.240	3.048	ns
1.5 V	6 mA	GCLK	t_{CO}	2.685	2.685	6.036	ns
		GCLK PLL	t_{CO}	1.243	1.243	2.930	ns
1.5 V	8 mA	GCLK	t_{CO}	2.644	2.644	5.983	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.877	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.629	2.629	5.762	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.650	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.712	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.600	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.590	2.590	5.639	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.527	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.591	2.591	5.626	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.514	ns

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.609	2.609	5.603	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.491	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.605	2.605	5.611	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.499	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.605	2.605	5.609	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.497	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.664	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.558	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.634	2.634	5.649	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.537	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.612	2.612	5.638	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.526	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.616	2.616	5.644	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.532	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.637	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.525	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.591	2.591	5.401	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.289	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.593	2.593	5.412	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.300	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.593	2.593	5.421	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.309	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.663	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.633	2.633	5.641	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.529	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.615	2.615	5.643	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.531	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.615	2.615	5.645	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.533	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.609	2.609	5.643	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.531	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.596	2.596	5.455	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.343	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.599	2.599	5.465	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.353	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.601	2.601	5.478	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.366	ns
3.3-V PCI	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–58 through Table 4–59 list EP1AGX35 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–58 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–58. EP1AGX35 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.126	0.126	0.281	ns
RCLK PLL input adder	0.011	0.011	0.018	ns
RCLK output adder	–0.126	–0.126	–0.281	ns
RCLK PLL output adder	–0.011	–0.011	–0.018	ns

Table 4–59 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–59. EP1AGX35 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.099	0.099	0.254	ns
RCLK PLL input adder	–0.012	–0.012	–0.01	ns
RCLK output adder	–0.086	–0.086	–0.244	ns
RCLK PLL output adder	1.253	1.253	3.133	ns

EP1AGX50 I/O Timing Parameters

Table 4–60 through Table 4–63 list the maximum I/O timing parameters for EP1AGX50 devices for I/O standards which support general purpose I/O pins.

Table 4–60 lists I/O timing specifications.

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
2.5 V	GCLK	t_{SU}	1.562	1.562	3.523	ns
		t_H	–1.457	–1.457	–3.246	ns
	GCLK PLL	t_{SU}	2.990	2.990	6.607	ns
		t_H	–2.885	–2.885	–6.330	ns
1.8 V	GCLK	t_{SU}	1.628	1.628	3.730	ns
		t_H	–1.523	–1.523	–3.453	ns
	GCLK PLL	t_{SU}	3.056	3.056	6.814	ns
		t_H	–2.951	–2.951	–6.537	ns
1.5 V	GCLK	t_{SU}	1.631	1.631	3.825	ns
		t_H	–1.526	–1.526	–3.548	ns
	GCLK PLL	t_{SU}	3.059	3.059	6.909	ns
		t_H	–2.954	–2.954	–6.632	ns

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS I	GCLK	t_{SU}	1.375	1.375	2.997	ns
		t_H	–1.270	–1.270	–2.720	ns
	GCLK PLL	t_{SU}	2.802	2.802	6.079	ns
		t_H	–2.697	–2.697	–5.802	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.375	1.375	2.997	ns
		t_H	–1.270	–1.270	–2.720	ns
	GCLK PLL	t_{SU}	2.802	2.802	6.079	ns
		t_H	–2.697	–2.697	–5.802	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.406	1.406	3.104	ns
		t_H	–1.301	–1.301	–2.827	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.407	1.407	3.106	ns
		t_H	–1.302	–1.302	–2.829	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.406	1.406	3.104	ns
		t_H	–1.301	–1.301	–2.827	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.407	1.407	3.106	ns
		t_H	–1.302	–1.302	–2.829	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.432	1.432	3.232	ns
		t_H	–1.327	–1.327	–2.955	ns
	GCLK PLL	t_{SU}	2.860	2.860	6.316	ns
		t_H	–2.755	–2.755	–6.039	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.433	1.433	3.234	ns
		t_H	–1.328	–1.328	–2.957	ns
	GCLK PLL	t_{SU}	2.860	2.860	6.316	ns
		t_H	–2.755	–2.755	–6.039	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–61 lists I/O timing specifications.

Table 4–61. EP1AGX50 Column Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
2.5 V	GCLK	t_{SU}	1.252	1.252	2.884	ns
		t_H	–1.147	–1.147	–2.607	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.991	ns
		t_H	–2.589	–2.589	–5.714	ns
1.8 V	GCLK	t_{SU}	1.318	1.318	3.094	ns
		t_H	–1.213	–1.213	–2.817	ns
	GCLK PLL	t_{SU}	2.760	2.760	6.201	ns
		t_H	–2.655	–2.655	–5.924	ns
1.5 V	GCLK	t_{SU}	1.321	1.321	3.187	ns
		t_H	–1.216	–1.216	–2.910	ns
	GCLK PLL	t_{SU}	2.763	2.763	6.294	ns
		t_H	–2.658	–2.658	–6.017	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.104	1.104	2.466	ns
		t_H	–0.999	–0.999	–2.189	ns
	GCLK PLL	t_{SU}	2.546	2.546	5.573	ns
		t_H	–2.441	–2.441	–5.296	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.074	1.074	2.424	ns
		t_H	–0.969	–0.969	–2.147	ns
	GCLK PLL	t_{SU}	2.539	2.539	5.564	ns
		t_H	–2.434	–2.434	–5.287	ns

Table 4–61. EP1AGX50 Column Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.104	1.104	2.466	ns
		t_H	–0.999	–0.999	–2.189	ns
	GCLK PLL	t_{SU}	2.546	2.546	5.573	ns
		t_H	–2.441	–2.441	–5.296	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.074	1.074	2.424	ns
		t_H	–0.969	–0.969	–2.147	ns
	GCLK PLL	t_{SU}	2.539	2.539	5.564	ns
		t_H	–2.434	–2.434	–5.287	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.122	1.122	2.594	ns
		t_H	–1.017	–1.017	–2.317	ns
	GCLK PLL	t_{SU}	2.564	2.564	5.701	ns
		t_H	–2.459	–2.459	–5.424	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.094	1.094	2.557	ns
		t_H	–0.989	–0.989	–2.280	ns
	GCLK PLL	t_{SU}	2.557	2.557	5.692	ns
		t_H	–2.452	–2.452	–5.415	ns
3.3-V PCI	GCLK	t_{SU}	1.247	1.247	2.890	ns
		t_H	–1.142	–1.142	–2.613	ns
	GCLK PLL	t_{SU}	2.689	2.689	5.997	ns
		t_H	–2.584	–2.584	–5.720	ns
3.3-V PCI-X	GCLK	t_{SU}	1.247	1.247	2.890	ns
		t_H	–1.142	–1.142	–2.613	ns
	GCLK PLL	t_{SU}	2.689	2.689	5.997	ns
		t_H	–2.584	–2.584	–5.720	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–62 lists I/O timing specifications.

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.915	2.915	6.713	ns
		GCLK PLL	t_{CO}	1.487	1.487	3.629	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.787	2.787	6.073	ns
		GCLK PLL	t_{CO}	1.359	1.359	2.989	ns

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.731	2.731	6.036	ns
		GCLK PLL	t_{CO}	1.303	1.303	2.952	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.787	2.787	6.073	ns
		GCLK PLL	t_{CO}	1.359	1.359	2.989	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.681	2.681	5.767	ns
		GCLK PLL	t_{CO}	1.253	1.253	2.683	ns
2.5 V	4 mA	GCLK	t_{CO}	2.770	2.770	6.047	ns
		GCLK PLL	t_{CO}	1.342	1.342	2.963	ns
2.5 V	8 mA	GCLK	t_{CO}	2.667	2.667	5.789	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.705	ns
2.5 V	12 mA	GCLK	t_{CO}	2.648	2.648	5.675	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.591	ns
1.8 V	2 mA	GCLK	t_{CO}	2.840	2.840	7.066	ns
		GCLK PLL	t_{CO}	1.412	1.412	3.982	ns
1.8 V	4 mA	GCLK	t_{CO}	2.829	2.829	6.287	ns
		GCLK PLL	t_{CO}	1.401	1.401	3.203	ns
1.8 V	6 mA	GCLK	t_{CO}	2.718	2.718	5.986	ns
		GCLK PLL	t_{CO}	1.290	1.290	2.902	ns
1.8 V	8 mA	GCLK	t_{CO}	2.687	2.687	5.872	ns
		GCLK PLL	t_{CO}	1.259	1.259	2.788	ns
1.5 V	2 mA	GCLK	t_{CO}	2.800	2.800	6.565	ns
		GCLK PLL	t_{CO}	1.372	1.372	3.481	ns
1.5 V	4 mA	GCLK	t_{CO}	2.693	2.693	5.964	ns
		GCLK PLL	t_{CO}	1.265	1.265	2.880	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.636	2.636	5.626	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.544	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.550	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.468	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.578	2.578	5.419	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.337	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.625	2.625	5.570	ns
		GCLK PLL	t_{CO}	1.197	1.197	2.486	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.628	2.628	5.497	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.415	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.604	2.604	5.480	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.398	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.607	2.607	5.459	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.377	ns

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.606	2.606	5.480	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.396	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.608	2.608	5.442	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.360	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.590	2.590	5.438	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.356	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.594	2.594	5.427	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.345	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.585	2.585	5.426	ns
		GCLK PLL	t_{CO}	1.158	1.158	2.344	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.605	2.605	5.457	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.373	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.607	2.607	5.441	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.359	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.592	2.592	5.433	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.351	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–63 lists I/O timing specifications.

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.948	2.948	6.608	ns
		GCLK PLL	t_{CO}	1.476	1.476	3.447	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.722	2.722	6.204	ns
		GCLK PLL	t_{CO}	1.264	1.264	3.075	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.694	2.694	6.024	ns
		GCLK PLL	t_{CO}	1.238	1.238	2.906	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.670	2.670	5.896	ns
		GCLK PLL	t_{CO}	1.216	1.216	2.781	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.660	2.660	5.895	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.783	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.695	2.695	5.893	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.780	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.663	2.663	5.809	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.702	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.666	2.666	5.776	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.670	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.651	2.651	5.758	ns
		GCLK PLL	t_{CO}	1.205	1.205	2.652	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.638	2.638	5.736	ns
		GCLK PLL	t_{CO}	1.194	1.194	2.630	ns
2.5 V	4 mA	GCLK	t_{CO}	2.754	2.754	6.240	ns
		GCLK PLL	t_{CO}	1.293	1.293	3.107	ns
2.5 V	8 mA	GCLK	t_{CO}	2.697	2.697	5.963	ns
		GCLK PLL	t_{CO}	1.241	1.241	2.845	ns
2.5 V	12 mA	GCLK	t_{CO}	2.672	2.672	5.837	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.728	ns
2.5 V	16 mA	GCLK	t_{CO}	2.654	2.654	5.760	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.654	ns
1.8 V	2 mA	GCLK	t_{CO}	2.804	2.804	7.295	ns
		GCLK PLL	t_{CO}	1.333	1.333	4.099	ns
1.8 V	4 mA	GCLK	t_{CO}	2.808	2.808	6.479	ns
		GCLK PLL	t_{CO}	1.338	1.338	3.325	ns
1.8 V	6 mA	GCLK	t_{CO}	2.717	2.717	6.195	ns
		GCLK PLL	t_{CO}	1.262	1.262	3.061	ns
1.8 V	8 mA	GCLK	t_{CO}	2.719	2.719	6.098	ns
		GCLK PLL	t_{CO}	1.264	1.264	2.970	ns
1.8 V	10 mA	GCLK	t_{CO}	2.671	2.671	6.012	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.893	ns
1.8 V	12 mA	GCLK	t_{CO}	2.671	2.671	5.953	ns
		GCLK PLL	t_{CO}	1.219	1.219	2.836	ns
1.5 V	2 mA	GCLK	t_{CO}	2.779	2.779	6.815	ns
		GCLK PLL	t_{CO}	1.313	1.313	3.629	ns
1.5 V	4 mA	GCLK	t_{CO}	2.703	2.703	6.210	ns
		GCLK PLL	t_{CO}	1.249	1.249	3.060	ns
1.5 V	6 mA	GCLK	t_{CO}	2.705	2.705	6.118	ns
		GCLK PLL	t_{CO}	1.252	1.252	2.942	ns
1.5 V	8 mA	GCLK	t_{CO}	2.660	2.660	6.014	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.889	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.648	2.648	5.777	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.675	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.628	2.628	5.722	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.625	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.606	2.606	5.649	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.552	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.606	2.606	5.636	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.539	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.601	2.601	5.634	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.537	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.643	2.643	5.749	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.639	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.649	2.649	5.708	ns
		GCLK PLL	t_{CO}	1.203	1.203	2.607	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.686	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.588	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.630	2.630	5.685	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.586	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.625	2.625	5.669	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.572	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.614	2.614	5.635	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.538	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.623	2.623	5.613	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.516	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.616	2.616	5.621	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.524	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.616	2.616	5.619	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.522	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.676	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.570	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.645	2.645	5.659	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.562	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.623	2.623	5.648	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.551	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.627	2.627	5.654	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.557	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.619	2.619	5.647	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.550	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.602	2.602	5.574	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.314	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.604	2.604	5.578	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.325	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.604	2.604	5.577	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.334	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.675	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.569	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.644	2.644	5.651	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.554	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.653	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.556	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.626	2.626	5.655	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.558	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.620	2.620	5.653	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.556	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.607	2.607	5.573	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.368	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.610	2.610	5.571	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.378	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.612	2.612	5.581	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.391	ns
3.3-V PCI	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–64 through Table 4–65 list EP1AGX50 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–64 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–64. EP1AGX50 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.151	0.151	0.329	ns
RCLK PLL input adder	0.011	0.011	0.016	ns
RCLK output adder	–0.151	–0.151	–0.329	ns
RCLK PLL output adder	–0.011	–0.011	–0.016	ns

Table 4–65 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–65. EP1AGX50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.146	0.146	0.334	ns
RCLK PLL input adder	–1.713	–1.713	–3.645	ns
RCLK output adder	–0.146	–0.146	–0.336	ns
RCLK PLL output adder	1.716	1.716	4.488	ns

EP1AGX60 I/O Timing Parameters

Table 4–66 through Table 4–69 list the maximum I/O timing parameters for EP1AGX60 devices for I/O standards which support general purpose I/O pins.

Table 4–66 lists I/O timing specifications.

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
2.5 V	GCLK	t_{SU}	1.425	1.425	3.094	ns
		t_H	–1.320	–1.320	–2.817	ns
	GCLK PLL	t_{SU}	2.987	2.987	6.517	ns
		t_H	–2.882	–2.882	–6.240	ns

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8 V	GCLK	t_{SU}	1.477	1.477	3.275	ns
		t_H	–1.372	–1.372	–2.998	ns
	GCLK PLL	t_{SU}	3.049	3.049	6.718	ns
		t_H	–2.944	–2.944	–6.441	ns
1.5 V	GCLK	t_{SU}	1.480	1.480	3.370	ns
		t_H	–1.375	–1.375	–3.093	ns
	GCLK PLL	t_{SU}	3.052	3.052	6.813	ns
		t_H	–2.947	–2.947	–6.536	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.237	1.237	2.566	ns
		t_H	–1.132	–1.132	–2.289	ns
	GCLK PLL	t_{SU}	2.800	2.800	5.990	ns
		t_H	–2.695	–2.695	–5.713	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.237	1.237	2.566	ns
		t_H	–1.132	–1.132	–2.289	ns
	GCLK PLL	t_{SU}	2.800	2.800	5.990	ns
		t_H	–2.695	–2.695	–5.713	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns
LVDS	GCLK	t_{SU}	1.208	1.208	2.664	ns
		t_H	–1.103	–1.103	–2.387	ns
	GCLK PLL	t_{SU}	2.767	2.767	6.083	ns
		t_H	–2.662	–2.662	–5.806	ns

Table 4–67 lists I/O timing specifications.

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
2.5 V	GCLK	t_{SU}	1.134	1.134	2.475	ns
		t_H	–1.029	–1.029	-2.198	ns
	GCLK PLL	t_{SU}	2.704	2.704	5.910	ns
		t_H	–2.599	–2.599	-5.633	ns
1.8 V	GCLK	t_{SU}	1.200	1.200	2.685	ns
		t_H	–1.095	–1.095	-2.408	ns
	GCLK PLL	t_{SU}	2.770	2.770	6.120	ns
		t_H	–2.665	–2.665	-5.843	ns
1.5 V	GCLK	t_{SU}	1.203	1.203	2.778	ns
		t_H	–1.098	–1.098	-2.501	ns
	GCLK PLL	t_{SU}	2.773	2.773	6.213	ns
		t_H	–2.668	–2.668	-5.936	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	-1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	-5.111	ns

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	–1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	–5.111	ns
SSTL-18 CLASS I	GCLK	t_{SU}	0.986	0.986	2.057	ns
		t_H	–0.881	–0.881	–1.780	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.492	ns
		t_H	–2.451	–2.451	–5.215	ns
SSTL-18 CLASS II	GCLK	t_{SU}	0.987	0.987	2.058	ns
		t_H	–0.882	–0.882	–1.781	ns
	GCLK PLL	t_{SU}	2.558	2.558	5.495	ns
		t_H	–2.453	–2.453	–5.218	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	0.986	0.986	2.057	ns
		t_H	–0.881	–0.881	–1.780	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.492	ns
		t_H	–2.451	–2.451	–5.215	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	0.987	0.987	2.058	ns
		t_H	–0.882	–0.882	–1.781	ns
	GCLK PLL	t_{SU}	2.558	2.558	5.495	ns
		t_H	–2.453	–2.453	–5.218	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.004	1.004	2.185	ns
		t_H	–0.899	–0.899	–1.908	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.620	ns
		t_H	–2.469	–2.469	–5.343	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.005	1.005	2.186	ns
		t_H	–0.900	–0.900	–1.909	ns
	GCLK PLL	t_{SU}	2.576	2.576	5.623	ns
		t_H	–2.471	–2.471	–5.346	ns
3.3-V PCI	GCLK	t_{SU}	1.129	1.129	2.481	ns
		t_H	–1.024	–1.024	–2.204	ns
	GCLK PLL	t_{SU}	2.699	2.699	5.916	ns
		t_H	–2.594	–2.594	–5.639	ns
3.3-V PCI-X	GCLK	t_{SU}	1.129	1.129	2.481	ns
		t_H	–1.024	–1.024	–2.204	ns
	GCLK PLL	t_{SU}	2.699	2.699	5.916	ns
		t_H	–2.594	–2.594	–5.639	ns

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	0.980	0.980	2.062	ns
		t_{H}	–0.875	–0.875	–1.785	ns
	GCLK PLL	t_{SU}	2.557	2.557	5.512	ns
		t_{H}	–2.452	–2.452	–5.235	ns

Table 4–68 lists I/O timing specifications.

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.052	3.052	7.142	ns
		GCLK PLL	t_{CO}	1.490	1.490	3.719	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.868	2.868	6.465	ns
		GCLK PLL	t_{CO}	1.306	1.306	3.042	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.818	2.818	6.196	ns
		GCLK PLL	t_{CO}	1.256	1.256	2.773	ns
2.5 V	4 mA	GCLK	t_{CO}	2.907	2.907	6.476	ns
		GCLK PLL	t_{CO}	1.345	1.345	3.053	ns
2.5 V	8 mA	GCLK	t_{CO}	2.804	2.804	6.218	ns
		GCLK PLL	t_{CO}	1.242	1.242	2.795	ns
2.5 V	12 mA	GCLK	t_{CO}	2.785	2.785	6.104	ns
		GCLK PLL	t_{CO}	1.223	1.223	2.681	ns
1.8 V	2 mA	GCLK	t_{CO}	2.991	2.991	7.521	ns
		GCLK PLL	t_{CO}	1.419	1.419	4.078	ns
1.8 V	4 mA	GCLK	t_{CO}	2.980	2.980	6.742	ns
		GCLK PLL	t_{CO}	1.408	1.408	3.299	ns
1.8 V	6 mA	GCLK	t_{CO}	2.869	2.869	6.441	ns
		GCLK PLL	t_{CO}	1.297	1.297	2.998	ns
1.8 V	8 mA	GCLK	t_{CO}	2.838	2.838	6.327	ns
		GCLK PLL	t_{CO}	1.266	1.266	2.884	ns
1.5 V	2 mA	GCLK	t_{CO}	2.951	2.951	7.020	ns
		GCLK PLL	t_{CO}	1.379	1.379	3.577	ns
1.5 V	4 mA	GCLK	t_{CO}	2.844	2.844	6.419	ns
		GCLK PLL	t_{CO}	1.272	1.272	2.976	ns

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.774	2.774	6.057	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.633	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.750	2.750	5.981	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.716	2.716	5.850	ns
		GCLK PLL	t_{CO}	1.153	1.153	2.426	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.776	2.776	6.025	ns
		GCLK PLL	t_{CO}	1.204	1.204	2.582	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.780	2.780	5.954	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.511	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.756	2.756	5.937	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.494	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.759	2.759	5.916	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.473	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.757	2.757	5.935	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.492	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.760	2.760	5.899	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.456	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.742	2.742	5.895	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.452	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.746	2.746	5.884	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.441	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.737	2.737	5.883	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.440	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	5.912	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.469	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.759	2.759	5.898	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.455	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.744	2.744	5.890	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.447	ns
LVDS	—	GCLK	t_{CO}	2.787	2.787	6.037	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.618	ns

Table 4–69 lists I/O timing specifications.

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.036	3.036	6.963	ns
		GCLK PLL	t_{CO}	1.466	1.466	3.528	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.824	2.824	6.591	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.156	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.798	2.798	6.422	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.987	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.776	2.776	6.297	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.862	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.769	2.769	6.299	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.864	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.799	2.799	6.296	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.861	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.771	2.771	6.218	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.783	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.778	2.778	6.186	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.751	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.765	2.765	6.168	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.733	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.754	2.754	6.146	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.711	ns
2.5 V	4 mA	GCLK	t_{CO}	2.853	2.853	6.623	ns
		GCLK PLL	t_{CO}	1.283	1.283	3.188	ns
2.5 V	8 mA	GCLK	t_{CO}	2.801	2.801	6.361	ns
		GCLK PLL	t_{CO}	1.231	1.231	2.926	ns
2.5 V	12 mA	GCLK	t_{CO}	2.780	2.780	6.244	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.809	ns
2.5 V	16 mA	GCLK	t_{CO}	2.762	2.762	6.170	ns
		GCLK PLL	t_{CO}	1.192	1.192	2.735	ns
1.8 V	2 mA	GCLK	t_{CO}	2.893	2.893	7.615	ns
		GCLK PLL	t_{CO}	1.323	1.323	4.180	ns
1.8 V	4 mA	GCLK	t_{CO}	2.898	2.898	6.841	ns
		GCLK PLL	t_{CO}	1.328	1.328	3.406	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.822	2.822	6.577	ns
		GCLK PLL	t_{CO}	1.252	1.252	3.142	ns
1.8 V	8 mA	GCLK	t_{CO}	2.824	2.824	6.486	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.051	ns
1.8 V	10 mA	GCLK	t_{CO}	2.778	2.778	6.409	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.974	ns
1.8 V	12 mA	GCLK	t_{CO}	2.779	2.779	6.352	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.917	ns
1.5 V	2 mA	GCLK	t_{CO}	2.873	2.873	7.145	ns
		GCLK PLL	t_{CO}	1.303	1.303	3.710	ns
1.5 V	4 mA	GCLK	t_{CO}	2.809	2.809	6.576	ns
		GCLK PLL	t_{CO}	1.239	1.239	3.141	ns
1.5 V	6 mA	GCLK	t_{CO}	2.812	2.812	6.458	ns
		GCLK PLL	t_{CO}	1.242	1.242	3.023	ns
1.5 V	8 mA	GCLK	t_{CO}	2.771	2.771	6.405	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.970	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.757	2.757	6.184	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.744	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.740	2.740	6.134	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.694	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.718	2.718	6.061	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.621	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.719	2.719	6.048	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.608	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.715	2.715	6.046	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.606	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.753	2.753	6.155	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.720	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.758	2.758	6.116	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.676	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.737	2.737	6.097	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.657	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.742	2.742	6.095	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.655	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.736	2.736	6.081	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.641	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.725	2.725	6.047	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.607	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.737	2.737	6.025	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.585	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.733	2.733	6.033	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.593	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.733	2.733	6.031	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.591	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	6.086	ns
		GCLK PLL	t_{CO}	1.186	1.186	2.651	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.762	2.762	6.071	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.631	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.740	2.740	6.060	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.620	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.744	2.744	6.066	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.626	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.736	2.736	6.059	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.619	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.719	2.719	5.823	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.383	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.721	2.721	5.834	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.394	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.721	2.721	5.843	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.403	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	6.085	ns
		GCLK PLL	t_{CO}	1.186	1.186	2.650	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.761	2.761	6.063	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.623	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.743	2.743	6.065	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.625	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.743	2.743	6.067	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.627	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.737	2.737	6.065	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.625	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.724	2.724	5.877	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.437	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.727	2.727	5.887	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.447	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.729	2.729	5.900	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.460	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V PCI	—	GCLK	t_{CO}	2.882	2.882	6.213	ns
		GCLK PLL	t_{CO}	1.312	1.312	2.778	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.882	2.882	6.213	ns
		GCLK PLL	t_{CO}	1.312	1.312	2.778	ns
LVDS	—	GCLK	t_{CO}	3.746	3.746	7.396	ns
		GCLK PLL	t_{CO}	2.185	2.185	3.973	ns

Table 4–70 through Table 4–71 list EP1AGX60 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–70 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–70. EP1AGX60 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.138	0.138	0.311	ns
RCLK PLL input adder	–0.003	–0.003	–0.006	ns
RCLK output adder	–0.138	–0.138	–0.311	ns
RCLK PLL output adder	0.003	0.003	0.006	ns

Table 4–71 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–71. EP1AGX60 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.153	0.153	0.344	ns
RCLK PLL input adder	–1.066	–1.066	–2.338	ns
RCLK output adder	–0.153	–0.153	–0.343	ns
RCLK PLL output adder	1.721	1.721	4.486	ns

EP1AGX90 I/O Timing Parameters

Table 4–72 through Table 4–75 list the maximum I/O timing parameters for EP1AGX90 devices for I/O standards which support general purpose I/O pins.

Table 4–72 lists I/O timing specifications.

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
2.5 V	GCLK	t_{SU}	1.307	1.307	2.854	ns
		t_H	–1.202	–1.202	–2.577	ns
	GCLK PLL	t_{SU}	3.378	3.378	6.998	ns
		t_H	–3.273	–3.273	–6.721	ns
1.8 V	GCLK	t_{SU}	1.381	1.381	3.073	ns
		t_H	–1.276	–1.276	–2.796	ns
	GCLK PLL	t_{SU}	3.434	3.434	7.191	ns
		t_H	–3.329	–3.329	–6.914	ns
1.5 V	GCLK	t_{SU}	1.384	1.384	3.168	ns
		t_H	–1.279	–1.279	–2.891	ns
	GCLK PLL	t_{SU}	3.437	3.437	7.286	ns
		t_H	–3.332	–3.332	–7.009	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.185	1.185	2.575	ns
		t_H	–1.080	–1.080	–2.298	ns
	GCLK PLL	t_{SU}	3.238	3.238	6.693	ns
		t_H	–3.133	–3.133	–6.416	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.183	1.183	2.569	ns
		t_H	–1.078	–1.078	–2.292	ns
	GCLK PLL	t_{SU}	3.261	3.261	6.725	ns
		t_H	–3.156	–3.156	–6.448	ns
LVDS	GCLK	t_{SU}	1.098	1.098	2.439	ns
		t_H	–0.993	–0.993	–2.162	ns
	GCLK PLL	t_{SU}	3.160	3.160	6.566	ns
		t_H	–3.055	–3.055	–6.289	ns

Table 4–73 lists I/O timing specifications.

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
2.5 V	GCLK	t_{SU}	1.028	1.028	2.272	ns
		t_H	–0.923	–0.923	–1.995	ns
	GCLK PLL	t_{SU}	3.092	3.092	6.407	ns
		t_H	–2.987	–2.987	–6.130	ns

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.8 V	GCLK	t_{SU}	1.094	1.094	2.482	ns
		t_H	–0.989	–0.989	–2.205	ns
	GCLK PLL	t_{SU}	3.158	3.158	6.617	ns
		t_H	–3.053	–3.053	–6.340	ns
1.5 V	GCLK	t_{SU}	1.097	1.097	2.575	ns
		t_H	–0.992	–0.992	–2.298	ns
	GCLK PLL	t_{SU}	3.161	3.161	6.710	ns
		t_H	–3.056	–3.056	–6.433	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.844	0.844	1.751	ns
		t_H	–0.739	–0.739	–1.474	ns
	GCLK PLL	t_{SU}	2.908	2.908	5.886	ns
		t_H	–2.803	–2.803	–5.609	ns
SSTL-2 CLASS II	GCLK	t_{SU}	0.844	0.844	1.751	ns
		t_H	–0.739	–0.739	–1.474	ns
	GCLK PLL	t_{SU}	2.908	2.908	5.886	ns
		t_H	–2.803	–2.803	–5.609	ns
SSTL-18 CLASS I	GCLK	t_{SU}	0.880	0.880	1.854	ns
		t_H	–0.775	–0.775	–1.577	ns
	GCLK PLL	t_{SU}	2.944	2.944	5.989	ns
		t_H	–2.839	–2.839	–5.712	ns
SSTL-18 CLASS II	GCLK	t_{SU}	0.883	0.883	1.858	ns
		t_H	–0.778	–0.778	–1.581	ns
	GCLK PLL	t_{SU}	2.947	2.947	5.993	ns
		t_H	–2.842	–2.842	–5.716	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	0.880	0.880	1.854	ns
		t_H	–0.775	–0.775	–1.577	ns
	GCLK PLL	t_{SU}	2.944	2.944	5.989	ns
		t_H	–2.839	–2.839	–5.712	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	0.883	0.883	1.858	ns
		t_H	–0.778	–0.778	–1.581	ns
	GCLK PLL	t_{SU}	2.947	2.947	5.993	ns
		t_H	–2.842	–2.842	–5.716	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	0.898	0.898	1.982	ns
		t_H	–0.793	–0.793	–1.705	ns
	GCLK PLL	t_{SU}	2.962	2.962	6.117	ns
		t_H	–2.857	–2.857	–5.840	ns

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	0.901	0.901	1.986	ns
		t_H	–0.796	–0.796	–1.709	ns
	GCLK PLL	t_{SU}	2.965	2.965	6.121	ns
		t_H	–2.860	–2.860	–5.844	ns
3.3-V PCI	GCLK	t_{SU}	1.023	1.023	2.278	ns
		t_H	–0.918	–0.918	–2.001	ns
	GCLK PLL	t_{SU}	3.087	3.087	6.413	ns
		t_H	–2.982	–2.982	–6.136	ns
3.3-V PCI-X	GCLK	t_{SU}	1.023	1.023	2.278	ns
		t_H	–0.918	–0.918	–2.001	ns
	GCLK PLL	t_{SU}	3.087	3.087	6.413	ns
		t_H	–2.982	–2.982	–6.136	ns
LVDS	GCLK	t_{SU}	0.891	0.891	1.920	ns
		t_H	–0.786	–0.786	–1.643	ns
	GCLK PLL	t_{SU}	2.963	2.963	6.066	ns
		t_H	–2.858	–2.858	–5.789	ns

Table 4–74 lists I/O timing specifications.

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.170	3.170	7.382	ns
		GCLK PLL	t_{CO}	1.099	1.099	3.238	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	3.042	3.042	6.742	ns
		GCLK PLL	t_{CO}	0.971	0.971	2.598	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.986	2.986	6.705	ns
		GCLK PLL	t_{CO}	0.915	0.915	2.561	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	3.042	3.042	6.742	ns
		GCLK PLL	t_{CO}	0.971	0.971	2.598	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.936	2.936	6.436	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.292	ns
2.5 V	4 mA	GCLK	t_{CO}	3.025	3.025	6.716	ns
		GCLK PLL	t_{CO}	0.954	0.954	2.572	ns
2.5 V	8 mA	GCLK	t_{CO}	2.922	2.922	6.458	ns
		GCLK PLL	t_{CO}	0.851	0.851	2.314	ns
2.5 V	12 mA	GCLK	t_{CO}	2.903	2.903	6.344	ns
		GCLK PLL	t_{CO}	0.832	0.832	2.200	ns

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	2 mA	GCLK	t_{CO}	3.087	3.087	7.723	ns
		GCLK PLL	t_{CO}	1.034	1.034	3.605	ns
1.8 V	4 mA	GCLK	t_{CO}	3.076	3.076	6.944	ns
		GCLK PLL	t_{CO}	1.023	1.023	2.826	ns
1.8 V	6 mA	GCLK	t_{CO}	2.965	2.965	6.643	ns
		GCLK PLL	t_{CO}	0.912	0.912	2.525	ns
1.8 V	8 mA	GCLK	t_{CO}	2.934	2.934	6.529	ns
		GCLK PLL	t_{CO}	0.881	0.881	2.411	ns
1.5 V	2 mA	GCLK	t_{CO}	3.047	3.047	7.222	ns
		GCLK PLL	t_{CO}	0.994	0.994	3.104	ns
1.5 V	4 mA	GCLK	t_{CO}	2.940	2.940	6.621	ns
		GCLK PLL	t_{CO}	0.887	0.887	2.503	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.890	2.890	6.294	ns
		GCLK PLL	t_{CO}	0.824	0.824	2.157	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.866	2.866	6.218	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.081	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.832	2.832	6.087	ns
		GCLK PLL	t_{CO}	0.766	0.766	1.950	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.872	2.872	6.227	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.109	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.878	2.878	6.162	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.006	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.854	2.854	6.145	ns
		GCLK PLL	t_{CO}	0.776	0.776	1.989	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.857	2.857	6.124	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.968	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.853	2.853	6.137	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.019	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.858	2.858	6.107	ns
		GCLK PLL	t_{CO}	0.780	0.780	1.951	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.840	2.840	6.103	ns
		GCLK PLL	t_{CO}	0.762	0.762	1.947	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.844	2.844	6.092	ns
		GCLK PLL	t_{CO}	0.766	0.766	1.936	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.835	2.835	6.091	ns
		GCLK PLL	t_{CO}	0.757	0.757	1.935	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.852	2.852	6.114	ns
		GCLK PLL	t_{CO}	0.799	0.799	1.996	ns

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.857	2.857	6.106	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.950	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.842	2.842	6.098	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.942	ns
LVDS	—	GCLK	t_{CO}	2.898	2.898	6.265	ns
		GCLK PLL	t_{CO}	0.831	0.831	2.129	ns

Table 4–75 lists I/O timing specifications.

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.141	3.141	7.164	ns
		GCLK PLL	t_{CO}	1.077	1.077	3.029	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.929	2.929	6.792	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.657	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.903	2.903	6.623	ns
		GCLK PLL	t_{CO}	0.839	0.839	2.488	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.881	2.881	6.498	ns
		GCLK PLL	t_{CO}	0.817	0.817	2.363	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.874	2.874	6.500	ns
		GCLK PLL	t_{CO}	0.810	0.810	2.365	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.904	2.904	6.497	ns
		GCLK PLL	t_{CO}	0.840	0.840	2.362	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.876	2.876	6.419	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.284	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.883	2.883	6.387	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.252	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.870	2.870	6.369	ns
		GCLK PLL	t_{CO}	0.806	0.806	2.234	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.859	2.859	6.347	ns
		GCLK PLL	t_{CO}	0.795	0.795	2.212	ns
2.5 V	4 mA	GCLK	t_{CO}	2.958	2.958	6.824	ns
		GCLK PLL	t_{CO}	0.894	0.894	2.689	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.906	2.906	6.562	ns
		GCLK PLL	t_{CO}	0.842	0.842	2.427	ns
2.5 V	12 mA	GCLK	t_{CO}	2.885	2.885	6.445	ns
		GCLK PLL	t_{CO}	0.821	0.821	2.310	ns
2.5 V	16 mA	GCLK	t_{CO}	2.867	2.867	6.371	ns
		GCLK PLL	t_{CO}	0.803	0.803	2.236	ns
1.8 V	2 mA	GCLK	t_{CO}	2.998	2.998	7.816	ns
		GCLK PLL	t_{CO}	0.934	0.934	3.681	ns
1.8 V	4 mA	GCLK	t_{CO}	3.003	3.003	7.042	ns
		GCLK PLL	t_{CO}	0.939	0.939	2.907	ns
1.8 V	6 mA	GCLK	t_{CO}	2.927	2.927	6.778	ns
		GCLK PLL	t_{CO}	0.863	0.863	2.643	ns
1.8 V	8 mA	GCLK	t_{CO}	2.929	2.929	6.687	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.552	ns
1.8 V	10 mA	GCLK	t_{CO}	2.883	2.883	6.610	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.475	ns
1.8 V	12 mA	GCLK	t_{CO}	2.884	2.884	6.553	ns
		GCLK PLL	t_{CO}	0.820	0.820	2.418	ns
1.5 V	2 mA	GCLK	t_{CO}	2.978	2.978	7.346	ns
		GCLK PLL	t_{CO}	0.914	0.914	3.211	ns
1.5 V	4 mA	GCLK	t_{CO}	2.914	2.914	6.777	ns
		GCLK PLL	t_{CO}	0.850	0.850	2.642	ns
1.5 V	6 mA	GCLK	t_{CO}	2.917	2.917	6.659	ns
		GCLK PLL	t_{CO}	0.853	0.853	2.524	ns
1.5 V	8 mA	GCLK	t_{CO}	2.876	2.876	6.606	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.471	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.859	2.859	6.381	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.250	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.842	2.842	6.331	ns
		GCLK PLL	t_{CO}	0.780	0.780	2.200	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.820	2.820	6.258	ns
		GCLK PLL	t_{CO}	0.758	0.758	2.127	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.821	2.821	6.245	ns
		GCLK PLL	t_{CO}	0.759	0.759	2.114	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.817	2.817	6.243	ns
		GCLK PLL	t_{CO}	0.755	0.755	2.112	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.858	2.858	6.356	ns
		GCLK PLL	t_{CO}	0.794	0.794	2.221	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.860	2.860	6.313	ns
		GCLK PLL	t_{CO}	0.798	0.798	2.182	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.839	2.839	6.294	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.163	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.844	2.844	6.292	ns
		GCLK PLL	t_{CO}	0.782	0.782	2.161	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.838	2.838	6.278	ns
		GCLK PLL	t_{CO}	0.776	0.776	2.147	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.827	2.827	6.244	ns
		GCLK PLL	t_{CO}	0.765	0.765	2.113	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.839	2.839	6.222	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.091	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.835	2.835	6.230	ns
		GCLK PLL	t_{CO}	0.773	0.773	2.099	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.835	2.835	6.228	ns
		GCLK PLL	t_{CO}	0.773	0.773	2.097	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.861	2.861	6.287	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.152	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.864	2.864	6.268	ns
		GCLK PLL	t_{CO}	0.802	0.802	2.137	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.842	2.842	6.257	ns
		GCLK PLL	t_{CO}	0.780	0.780	2.126	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.846	2.846	6.263	ns
		GCLK PLL	t_{CO}	0.784	0.784	2.132	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.838	2.838	6.256	ns
		GCLK PLL	t_{CO}	0.776	0.776	2.125	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.821	2.821	6.020	ns
		GCLK PLL	t_{CO}	0.759	0.759	1.889	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.823	2.823	6.031	ns
		GCLK PLL	t_{CO}	0.761	0.761	1.900	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.823	2.823	6.040	ns
		GCLK PLL	t_{CO}	0.761	0.761	1.909	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.861	2.861	6.286	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.151	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.863	2.863	6.260	ns
		GCLK PLL	t_{CO}	0.801	0.801	2.129	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.845	2.845	6.262	ns
		GCLK PLL	t_{CO}	0.783	0.783	2.131	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.845	2.845	6.264	ns
		GCLK PLL	t_{CO}	0.783	0.783	2.133	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.839	2.839	6.262	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.131	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.826	2.826	6.074	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.943	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.829	2.829	6.084	ns
		GCLK PLL	t_{CO}	0.767	0.767	1.953	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.831	2.831	6.097	ns
		GCLK PLL	t_{CO}	0.769	0.769	1.966	ns
3.3-V PCI	—	GCLK	t_{CO}	2.987	2.987	6.414	ns
		GCLK PLL	t_{CO}	0.923	0.923	2.279	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.987	2.987	6.414	ns
		GCLK PLL	t_{CO}	0.923	0.923	2.279	ns
LVDS	—	GCLK	t_{CO}	3.835	3.835	7.541	ns
		GCLK PLL	t_{CO}	1.769	1.769	3.404	ns

Table 4–76 through Table 4–77 list the EP1AGX90 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–76 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–76. EP1AGX90 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.175	0.175	0.418	ns
RCLK PLL input adder	0.007	0.007	0.015	ns
RCLK output adder	–0.175	–0.175	–0.418	ns
RCLK PLL output adder	–0.007	–0.007	–0.015	ns

Table 4–77 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–77. EP1AGX90 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.138	0.138	0.354	ns
RCLK PLL input adder	–1.697	–1.697	–3.607	ns
RCLK output adder	–0.138	–0.138	–0.353	ns
RCLK PLL output adder	1.966	1.966	5.188	ns

Dedicated Clock Pin Timing

Table 4–79 through Table 4–98 list clock pin timing for Arria GX devices when the clock is driven by the global clock, regional clock, periphery clock, and a PLL.

Table 4–78 lists Arria GX clock timing parameters.

Table 4–78. Arria GX Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL inclk pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL inclk pad to I/O output register

EP1AGX20 Clock Timing Parameters

Table 4–79 through Table 4–80 list the GCLK clock timing parameters for EP1AGX20 devices.

Table 4–79 lists clock timing specifications.

Table 4–79. EP1AGX20 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
tcin	1.394	1.394	3.161	ns
tcout	1.399	1.399	3.155	ns
tpllcin	–0.027	–0.027	0.091	ns
tpllcout	–0.022	–0.022	0.085	ns

Table 4–80 lists clock timing specifications.

Table 4–80. EP1AGX20 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.655	1.655	3.726	ns
t_{COUT}	1.655	1.655	3.726	ns
t_{PLLCIN}	0.236	0.236	0.655	ns
$t_{PLLCOUT}$	0.236	0.236	0.655	ns

Table 4–81 through Table 4–82 list the RCLK clock timing parameters for EP1AGX20 devices.

Table 4–81 lists clock timing specifications.

Table 4–81. EP1AGX20 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.283	1.283	2.901	ns
t_{COUT}	1.288	1.288	2.895	ns
t_{PLLCIN}	–0.034	–0.034	0.077	ns
$t_{PLLCOUT}$	–0.029	–0.029	0.071	ns

Table 4–82 lists clock timing specifications.

Table 4–82. EP1AGX20 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.569	1.569	3.487	ns
t_{COUT}	1.569	1.569	3.487	ns
t_{PLLCIN}	0.278	0.278	0.706	ns
$t_{PLLCOUT}$	0.278	0.278	0.706	ns

EP1AGX35 Clock Timing Parameters

Table 4–83 through Table 4–84 list the GCLK clock timing parameters for EP1AGX35 devices.

Table 4–83 lists clock timing specifications.

Table 4–83. EP1AGX35 Row Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.394	1.394	3.161	ns
t_{COUT}	1.399	1.399	3.155	ns

Table 4–83. EP1AGX35 Row Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{PLLCIN}	–0.027	–0.027	0.091	ns
$t_{PLLCOUT}$	–0.022	–0.022	0.085	ns

Table 4–84 lists clock timing specifications.

Table 4–84. EP1AGX35 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.655	1.655	3.726	ns
t_{COUT}	1.655	1.655	3.726	ns
t_{PLLCIN}	0.236	0.236	0.655	ns
$t_{PLLCOUT}$	0.236	0.236	0.655	ns

Table 4–85 through Table 4–86 list the RCLK clock timing parameters for EP1AGX35 devices.

Table 4–85 lists clock timing specifications.

Table 4–85. EP1AGX35 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.283	1.283	2.901	ns
t_{COUT}	1.288	1.288	2.895	ns
t_{PLLCIN}	–0.034	–0.034	0.077	ns
$t_{PLLCOUT}$	–0.029	–0.029	0.071	ns

Table 4–86 lists clock timing specifications.

Table 4–86. EP1AGX35 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.569	1.569	3.487	ns
t_{COUT}	1.569	1.569	3.487	ns
t_{PLLCIN}	0.278	0.278	0.706	ns
$t_{PLLCOUT}$	0.278	0.278	0.706	ns

EP1AGX50 Clock Timing Parameters

Table 4–87 through Table 4–88 list the GCLK clock timing parameters for EP1AGX50 devices.

Table 4–87 lists clock timing specifications.

Table 4–87. EP1AGX50 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.529	1.529	3.587	ns
t_{COUT}	1.534	1.534	3.581	ns
t_{PLLCIN}	–0.024	–0.024	0.181	ns
$t_{PLLCOUT}$	–0.019	–0.019	0.175	ns

Table 4–88 lists clock timing specifications.

Table 4–88. EP1AGX50 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.793	1.793	4.165	ns
t_{COUT}	1.793	1.793	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–89 through Table 4–90 list the RCLK clock timing parameters for EP1AGX50 devices.

Table 4–89 lists clock timing specifications.

Table 4–89. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.396	1.396	3.287	ns
t_{COUT}	1.401	1.401	3.281	ns
t_{PLLCIN}	–0.017	–0.017	0.195	ns
$t_{PLLCOUT}$	–0.012	–0.012	0.189	ns

Table 4–90 lists clock timing specifications.

Table 4–90. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.653	1.653	3.841	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX60 Clock Timing Parameters

Table 4–91 to Table 4–92 on page 4–82 list the GCLK clock timing parameters for EP1AGX60 devices.

Table 4–91 lists clock timing specifications.

Table 4–91. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.531	1.531	3.593	ns
t_{COUT}	1.536	1.536	3.587	ns
t_{PLLCIN}	–0.023	–0.023	0.188	ns
$t_{PLLCOUT}$	–0.018	–0.018	0.182	ns

Table 4–92 lists clock timing specifications.

Table 4–92. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.792	1.792	4.165	ns
t_{COUT}	1.792	1.792	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–93 through Table 4–94 list the RCLK clock timing parameters for EP1AGX60 devices.

Table 4–93 lists clock timing specifications.

Table 4–93. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.382	1.382	3.268	ns
t_{COUT}	1.387	1.387	3.262	ns
t_{PLLCIN}	–0.031	–0.031	0.174	ns
$t_{PLLCOUT}$	–0.026	–0.026	0.168	ns

Table 4–94 lists clock timing specifications.

Table 4–94. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.649	1.649	3.835	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX90 Clock Timing Parameters

Table 4–95 through Table 4–96 list the GCLK clock timing parameters for EP1AGX90 devices.

Table 4–95 lists clock timing specifications.

Table 4–95. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.630	1.630	3.799	ns
t_{COUT}	1.635	1.635	3.793	ns
t_{PLLCIN}	–0.422	–0.422	–0.310	ns
$t_{PLLCOUT}$	–0.417	–0.417	–0.316	ns

Table 4–96 lists clock timing specifications.

Table 4–96. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.904	1.904	4.376	ns
t_{COUT}	1.904	1.904	4.376	ns
t_{PLLCIN}	–0.153	–0.153	0.254	ns
$t_{PLLCOUT}$	–0.153	–0.153	0.254	ns

Table 4–97 through Table 4–98 list the RCLK clock timing parameters for EP1AGX90 devices.

Table 4–97 lists clock timing specifications.

Table 4–97. EP1AGX90 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.462	1.462	3.407	ns
t_{COUT}	1.467	1.467	3.401	ns
t_{PLLCIN}	–0.430	–0.430	–0.322	ns
$t_{PLLCOUT}$	–0.425	–0.425	–0.328	ns

Table 4–98 lists clock timing specifications.

Table 4–98. EP1AGX90 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.760	1.760	4.011	ns
t_{COUT}	1.760	1.760	4.011	ns
t_{PLLCIN}	–0.118	–0.118	0.303	ns
$t_{PLLCOUT}$	–0.118	–0.118	0.303	ns

Block Performance

Table 4–99 shows the Arria GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) or MegaCore functions for finite impulse response (FIR) and fast Fourier transform (FFT) designs.

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
DSP block	9 x 9-bit multiplier	0	0	1	335.35
	18 x 18-bit multiplier	0	0	2	285.0
	18 x 18-bit multiplier	0	0	4	335.35
	36 x 36-bit multiplier	0	0	8	174.4
	36 x 36-bit multiplier	0	0	8	285.0
	18-bit 4-tap FIR filter	0	0	8	163.0
Larger Designs	8-bit 16-tap parallel FIR filter	0	0	4	163.0

IOE Programmable Delay

For IOE programmable delay, refer to Table 4–100 through Table 4–101.

Table 4–100 lists IOE programmable delays.

Table 4–100. Arria GX IOE Programmable Delay on Row Pins

Parameter	Paths Affected	Available Settings	Fast Model				–6 Speed Grade		Units
			Industrial		Commercial				
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	8	0	1.782	0	1.782	0	4.124	ns
Input delay from pin to input register	Pad to I/O input register	64	0	2.054	0	2.054	0	4.689	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.332	0	0.332	0	0.717	ns
Output enable pin delay	txz/tzx	2	0	0.32	0	0.32	0	0.693	ns

Table 4–101 lists IOE programmable delays.

Table 4–101. Arria GX IOE Programmable Delay on Column Pins

Parameter	Paths Affected	Available Settings	Fast Model				–6 Speed Grade		Units
			Industrial		Commercial				
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	8	0	1.781	0	1.781	0	4.132	ns
Input delay from pin to input register	Pad to I/O input register	64	0	2.053	0	2.053	0	4.697	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.332	0	0.332	0	0.717	ns
Output enable pin delay	txz/tzx	2	0	0.32	0	0.32	0	0.693	ns

Maximum Input and Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 4–105, Table 4–106, and Table 4–107 provide output toggle rates at the default capacitive loading. Use the Quartus II software to obtain output toggle rates at loads different from the default capacitive loading.

Table 4–102 shows the maximum input clock toggle rates for Arria GX device column I/O pins.

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
3.3-V PCI	420	MHz
3.3-V PCI-X	420	MHz

Table 4–103 shows the maximum input clock toggle rates for Arria GX device row I/O pins.

Table 4–103. Arria GX Maximum Input Toggle Rate for Row I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
LVDS	392	MHz

Table 4–104 shows the maximum input clock toggle rates for Arria GX device dedicated clock pins.

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	373	MHz
3.3-V LVCMOS	373	MHz
2.5 V	373	MHz
1.8 V	373	MHz
1.5 V	373	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
3.3-V PCI	373	MHz

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V PCI-X	373	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
1.2-V HSTL	233	MHz
DIFFERENTAL SSTL-2	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.2-V HSTL	233	MHz
LVDS	640	MHz
LVDS *(1)*	373	MHz

Note to Table 4–104:

(1) This set of numbers refers to the VIO dedicated input clock pins.

Table 4–105 shows the maximum output clock toggle rates for Arria GX device column I/O pins.

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 1 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 2 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 3 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	607	MHz
	12 mA	654	MHz
1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
3.3-V PCI	—	626	MHz
3.3-V PCI-X	—	626	MHz

Table 4–106 shows the maximum output clock toggle rates for Arria GX device row I/O pins.

Table 4–106. Arria GX Maximum Output Toggle Rate for Row I/O Pins

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz

Table 4–106. Arria GX Maximum Output Toggle Rate for Row I/O Pins

I/O Standards	Drive Strength	–6 Speed Grade	Units
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
LVDS	—	598	MHz

Table 4–107 lists maximum output clock rate for dedicated clock pins.

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 1 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10mA	607	MHz
	12 mA	654	MHz
1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
	24 mA	278	MHz
DIFFERENTIAL SSTL-2	8 mA	280	MHz
	12 mA	327	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 3 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
DIFFERENTIAL 1.8-V SSTL CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	607	MHz
	12 mA	654	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
	24 mA	278	MHz
3.3-V PCI	—	626	MHz
3.3-V PCI-X	—	626	MHz
LVDS	—	280	MHz
HYPERTRANSPORT	—	116	MHz
LVPECL	—	280	MHz
3.3-V LVTTL	SERIES_25_OHMS	327	MHz
	SERIES_50_OHMS	327	MHz
3.3-V LVCMOS	SERIES_25_OHMS	280	MHz
	SERIES_50_OHMS	280	MHz
2.5 V	SERIES_25_OHMS	280	MHz
	SERIES_50_OHMS	280	MHz
1.8 V	SERIES_25_OHMS	420	MHz
	SERIES_50_OHMS	420	MHz

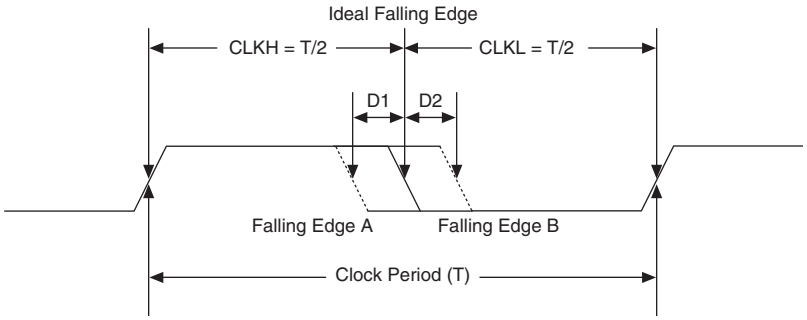
Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
1.5 V	SERIES_50_OHMS	373	MHz
SSTL-2 CLASS I	SERIES_50_OHMS	467	MHz
SSTL-2 CLASS II	SERIES_25_OHMS	467	MHz
SSTL-18 CLASS I	SERIES_50_OHMS	327	MHz
SSTL-18 CLASS II	SERIES_25_OHMS	420	MHz
1.8-V HSTL CLASS I	SERIES_50_OHMS	561	MHz
1.8-V HSTL CLASS II	SERIES_25_OHMS	420	MHz
1.5-V HSTL CLASS I	SERIES_50_OHMS	467	MHz
1.2-V HSTL	SERIES_50_OHMS	233	MHz
DIFFERENTIAL SSTL-2	SERIES_50_OHMS	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	SERIES_25_OHMS	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	SERIES_50_OHMS	327	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	SERIES_25_OHMS	420	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	SERIES_50_OHMS	561	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	SERIES_25_OHMS	420	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	SERIES_50_OHMS	467	MHz
DIFFERENTIAL 1.2-V HSTL	SERIES_50_OHMS	233	MHz

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 4–10. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (refer to Figure 4–10). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 4–10. Duty Cycle Distortion



DCD expressed in absolution derivation, for example, D1 or D2 in Figure 4–10, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

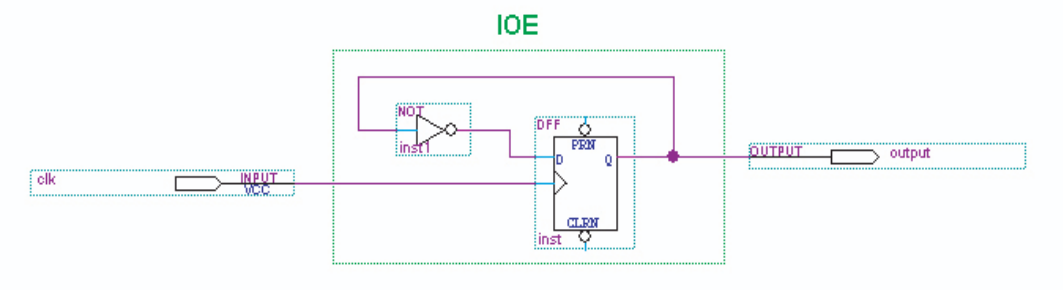
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

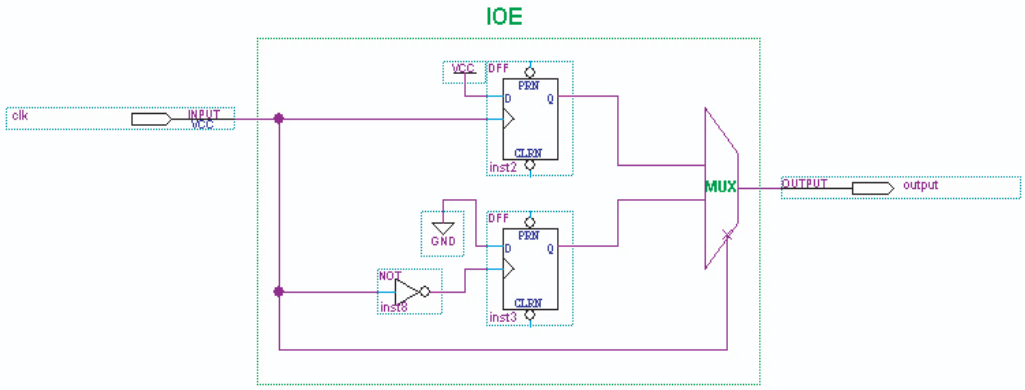
DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 4–11). Therefore, any DCD present on the input clock signal or caused by the clock input buffer or different input I/O standard does not transfer to the output signal.

Figure 4–11. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 4–12). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 4–12. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Table 4–108 through Table 4–113 show the maximum DCD in absolution derivation for different I/O standards on Arria GX devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 4–108. Maximum DCD for Non-DDIO Output on Row I/O Pins

Row I/O Output Standard	Maximum DCD (ps) for Non-DDIO Output	
	–6 Speed Grade	Units
3.3-V LVTTTL	275	ps
3.3-V LVCMOS	155	ps
2.5 V	135	ps
1.8 V	180	ps
1.5-V LVCMOS	195	ps
SSTL-2 Class I	145	ps
SSTL-2 Class II	125	ps
SSTL-18 Class I	85	ps
1.8-V HSTL Class I	100	ps
1.5-V HSTL Class I	115	ps
LVDS	80	ps

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 125 ps (see Table 4–109). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1/f = 1 / 267\ \text{MHz} = 3.745\ \text{ns} = 3{,}745\ \text{ps}$$

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 125 ps) / 3,745 ps = 46.66% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 125 ps) / 3,745 ps = 53.33% (for high boundary)

Therefore, the DCD percentage for the output clock at 267 MHz is from 46.66% to 53.33%.

Table 4–109. Maximum DCD for Non-DDIO Output on Column I/O Pins

Column I/O Output Standard I/O Standard	Maximum DCD (ps) for Non-DDIO Output	Units
	–6 Speed Grade	
3.3-V LVTTL	220	ps
3.3-V LVCMOS	175	ps
2.5 V	155	ps
1.8 V	110	ps
1.5-V LVCMOS	215	ps
SSTL-2 Class I	135	ps
SSTL-2 Class II	130	ps
SSTL-18 Class I	115	ps
SSTL-18 Class II	100	ps
1.8-V HSTL Class I	110	ps
1.8-V HSTL Class II	110	ps
1.5-V HSTL Class I	115	ps
1.5-V HSTL Class II	80	ps
1.2-V HSTL-12	200	ps
LVPECL	80	ps

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
LVDS	180	180	180	180	180	ps

Note to Table 4–110:

(1) Table 4–110 assumes the input clock has zero DCD.

Table 4–111. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path *(Note 1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

Note to Table 4–111:

(1) Table 4–111 assumes the input clock has zero DCD.

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	105	ps
3.3-V LVCMOS	75	ps
2.5V	90	ps
1.8V	100	ps
1.5-V LVCMOS	100	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
SSTL-18 Class I	65	ps
1.8-V HSTL Class I	70	ps
1.5-V HSTL Class I	70	ps
LVDS	180	ps

Table 4–113. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Column DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	160	ps
3.3-V LVCMOS	110	ps
2.5V	95	ps
1.8V	100	ps
1.5-V LVCMOS	155	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps
SSTL-18 Class I	65	ps
SSTL-18 Class II	80	ps
1.8-V HSTL Class I	70	ps
1.8-V HSTL Class II	70	ps
1.5-V HSTL Class I	70	ps
1.5-V HSTL Class II	100	ps
1.2-V HSTL	155	ps
LVPECL	180	ps

High-Speed I/O Specifications

Table 4–114 lists high-speed timing specifications definitions.

Table 4–114. High-Speed Timing Specifications and Definitions (Part 1 of 2)

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.

Table 4–114. High-Speed Timing Specifications and Definitions (Part 2 of 2)

High-Speed Timing Specifications	Definitions
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 4–115 shows the high-speed I/O timing specifications.

Table 4–115. High-Speed I/O Specifications (Part 1 of 2) *Note (1), (2)*

Symbol	Conditions	–6 Speed Grade			Units
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16	—	420	MHz
	W = 1 (SERDES bypass, LVDS only)	16	—	500	MHz
	W = 1 (SERDES used, LVDS only)	150	—	640	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150	—	840	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*	—	700	Mbps
	J = 1 (LVDS only)	*(4)*	—	500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150	—	840	Mbps
TCCS	All differential I/O standards	—	—	200	ps
SW	All differential I/O standards	440	—	—	ps
Output jitter	—	—	—	190	ps
Output t_{RISE}	All differential I/O standards	—	—	290	ps
Output t_{FALL}	All differential I/O standards	—	—	290	ps
t_{DUTY}	—	45	50	55	%
DPA run length	—	—	—	6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter	0.44	—	—	UI

Table 4–115. High-Speed I/O Specifications (Part 2 of 2) *Note (1), (2)*

Symbol	Conditions			–6 Speed Grade			Units
				Min	Typ	Max	
DPA lock time	Standard	Training Pattern	Transition Density		—	—	Number of repetitions
	SPI-4	000000000011 11111111	10%	256	—	—	
	Parallel Rapid I/O	00001111	25%	256	—	—	
		10010000	50%	256	—	—	
	Miscellaneous	10101010	100%	256	—	—	
		01010101	—	256	—	—	

Notes to Table 4–115:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.

PLL Timing Specifications

Table 4–116 and Table 4–117 describe the Arria GX PLL specifications when operating in both the commercial junction temperature range (0 to 85 C) and the industrial junction temperature range (–40 to 100 C), except for the clock switchover and phase-shift stepping features. These two features are only supported from the 0 to 100 C junction temperature range.

Table 4–116. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Units
f_{IN}	Input clock frequency	2	—	500	MHz
f_{INPFD}	Input frequency to the PFD	2	—	420	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
f_{ENDUTY}	External feedback input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤ 0.85 MHz	—	0.5	—	ns (peak-to-peak)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz	—	1.0	—	ns (peak-to-peak)
$t_{OUTJITTER}$	Dedicated clock output period jitter	50	100	250	ps (p-p)
t_{FCOMP}	External feedback compensation time	—	—	10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*	—	550	MHz
$f_{SCANCLK}$	Scanclk frequency	—	—	100	MHz
$t_{CONFIGEPLL}$	Time required to reconfigure scan chains for EPLLs	—	$174/f_{SCANCLK}$	—	ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*		*(1)*	MHz
$f_{OUTDUTY}$	Duty cycle for external clock output	45	50	55	%
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of device configuration	—	0.03	1	ms
t_{DLOCK}	Time required for the PLL to lock dynamically after automatic clock switchover between two identical clock frequencies	—	—	1	ms
$f_{SWITCHOVER}$	Frequency range where the clock switchover performs properly	1.5	1	500	MHz
f_{CLBW}	PLL closed-loop bandwidth	0.13	1.2	16.9	MHz
f_{VCO}	PLL VCO operating range	300	—	840	MHz
f_{SS}	Spread-spectrum modulation frequency	100	—	500	kHz
% spread	Percent down spread for a given clock frequency	0.4	0.5	0.6	%
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±30	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10	—	—	ns
$t_{ARESET_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high.	500	—	—	ns

Table 4–116. Enhanced PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.	—	—	2	us

Notes to Table 4–116:

(1) This is limited by the I/O f_{MAX}.

(2) If the counter cascading feature of the PLL is used, there is no minimum output clock frequency.

Table 4–117. Fast PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Units
f_{IN}	Input clock frequency	16.08	—	640	MHz
f_{INPFD}	Input frequency to the PFD	16.08	—	500	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz	—	0.5	—	ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz	—	1.0	—	ns (p-p)
f_{VCO}	Upper VCO frequency range	300	—	840	MHz
	Lower VCO frequency range	150	—	420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875	—	550	MHz
	PLL output frequency to LVDS or DPA clock	150	—	840	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875	—	*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs	—	$75/f_{SCANCLK}$	—	ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration	—	0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns

Table 4–117. Fast PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{ARESET_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500	—	—	ns

Note to Table 4–117:

(1) This is limited by the I/O f_{MAX}.

External Memory Interface Specifications

Table 4–118 through Table 4–122 list Arria GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–118. DLL Frequency Range Specifications

Frequency Mode	Frequency Range (MHz)
0	100 to 175
1	150 to 230
2	200 to 310

Table 4–119. DQS Jitter Specifications for DLL-Delayed Clock (tDQS_JITTER) , *(Note 1)*

Number of DQS Delay Buffer Stages *(2)*	Commercial (ps)	Industrial (ps)
1	80	110
2	110	130
3	130	180
4	160	210

Notes to Table 4–119:

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.

(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–120. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})

Number of DQS Delay Buffer Stages	–6 Speed Grade (ps)
1	35
2	70
3	105
4	140

Table 4–121. DQS Bus Clock Skew Adder Specifications ($t_{DQS_CLOCK_SKEW_ADDER}$)

Mode	DQS Clock Skew Adder (ps)
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

Table 4–122. DQS Phase Offset Delay Per Stage (ps) *Note (1), (2), (3)*

Speed Grade	Positive Offset		Negative Offset	
	Min	Max	Min	Max
–6	10	16	8	12

Notes to Table 4–122:

(1) The delay settings are linear.
(2) The valid settings for phase offset are –32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–13 shows the timing requirements for the JTAG signals

Figure 4–13. Arria GX JTAG Waveforms.

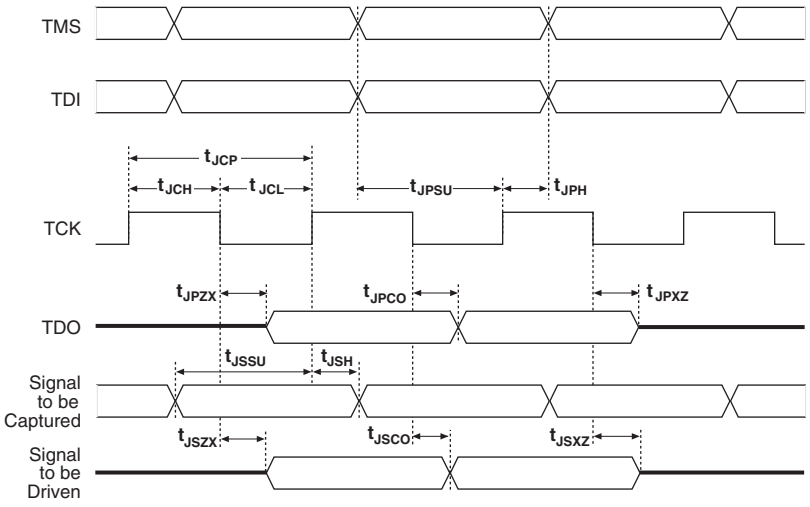


Table 4–123 lists the JTAG timing parameters and values for Arria GX devices.

Table 4–123. Arria GX JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Units
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	12	—	ns
t_{JCL}	TCK clock low time	12	—	ns
t_{JPSU}	JTAG port setup time	4	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	9	ns
t_{JPZX}	JTAG port high impedance to valid output	—	9	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	9	ns
t_{JSSU}	Capture register setup time	4	—	ns
t_{JSH}	Capture register hold time	5	—	ns
t_{JSCO}	Update register clock to output	—	12	ns
t_{JSZX}	Update register high impedance to valid output	—	12	ns
t_{JSXZ}	Update register valid output to high impedance	—	12	ns

Document Revision History

Table 4–124 lists the revision history for this chapter.

Table 4–124. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Updated Table 4–104, Table 4–105, and Table 4–106. ■ Document template update. ■ Minor text edits.	—
April 2009 v1.4	■ Updated Table 4–6 and Table 4–7. ■ Updated "Maximum Input and Output Clock Toggle Rate" section.	—
May 2008 v1.3	Updated: ■ Table 4–5 ■ Table 4–7 ■ Table 4–8 ■ Table 4–9 ■ Table 4–10 ■ Table 4–11 ■ Table 4–12 ■ Table 4–13 ■ Table 4–14 ■ Table 4–15 ■ Table 4–16 ■ Table 4–17 ■ Table 4–43 ■ Table 4–116 ■ Table 4–117	—
	Updated: ■ Figure 4–4	—
	Minor text edits.	—
August 2007 v1.2	Removed "Preliminary" from each page.	—
	Removed "Preliminary" note from Tables 4–44, 4–45, and 4–47.	—
	Added "Referenced Documents" section.	—
June 2007 v1.1	Updated Table 4–99.	—
	Added GIGE information.	—
May 2007 v1.0	Initial release.	—

5. Reference and Ordering Information

AGX51005-2.0

Software

Arria® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Development Software Handbook* .

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris 8/9, Linux Red Hat v7.3, Linux Red Hat Enterprise 3, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

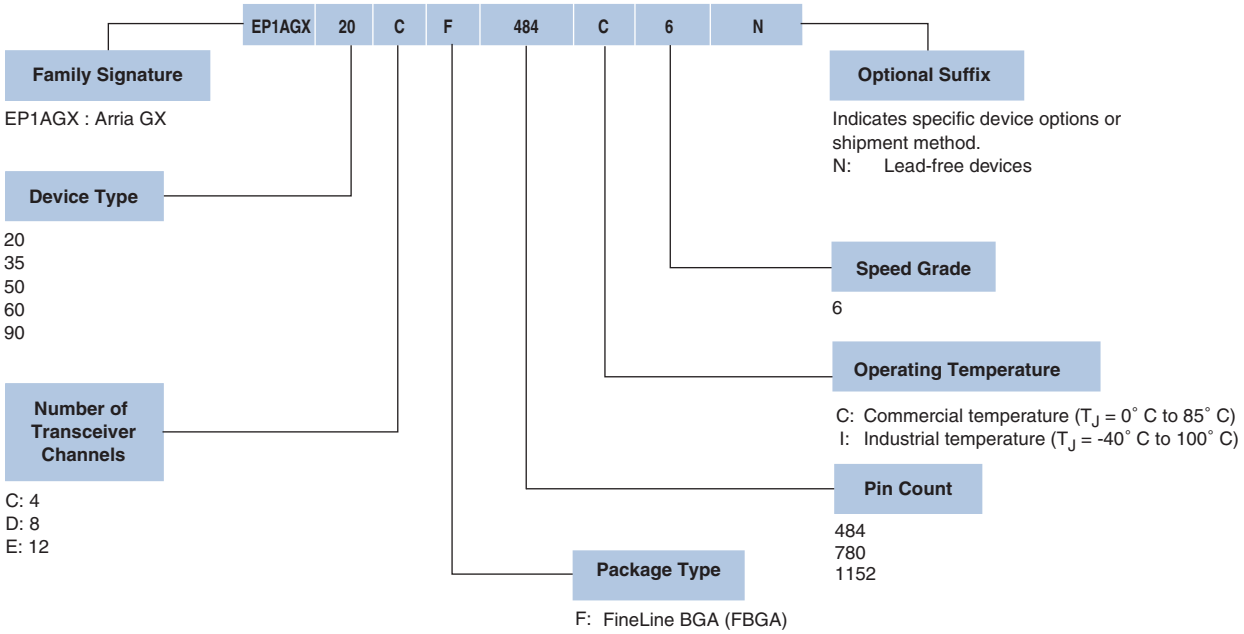
Arria GX device pin-outs are available on the Altera web site at www.altera.com.

Ordering Information

Figure 5–1 describes the ordering codes for Arria GX devices.

For more information on a specific package, refer to the *Package Information for Arria GX Devices* chapter.

Figure 5–1. Arria GX Device Packaging Ordering Information



Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
August 2007, v1.1	Added the "Referenced Documents" section.	—
May 2007, v1.0	Initial Release.	—

About this Handbook

This handbook provides comprehensive information about the Altera® Arria® GX family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, see the following table.

Contact *(Note 1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Email	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions that this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names and dialog box titles. For example, **Save As** dialog box.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, dialog box options, software utility names, and other GUI labels. For example, **\qdesigns** directory, **d:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicates document titles. For example, *AN 519: Stratix IV Design Guidelines*.
Italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file.
Initial Capital Letters	Indicates keyboard keys and menu names. For example, Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. Active-low signals are denoted by suffix `n`. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
↵	The angled arrow instructs you to press **Enter**.
	The feet direct you to more information about a particular topic.

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