THE DATASHEET OF

ADUM4221ARIZ

Isolated, Half Bridge Gate Driver with Adjustable Dead Time, 4 A Output

Data Sheet

ADuM4221

FEATURES

- 4 A peak current (<2 Ω R_{DSON_x})
- 2.5 V to 6.5 V logic input voltage
- 4.5 V to 35 V output supply voltage
- UVLO V_{DD1} positive going threshold: 2.5 V maximum
- Multiple UVLO options for V_{DDA} and V_{DDB} positive going threshold
  - Grade A: 4.5 V maximum
  - Grade B: 7.5 V maximum
  - Grade C: 11.6 V maximum
- Precise timing characteristics
  - 44 ns maximum propagation delay
- Adjustable dead time
- CMOS input logic levels
- High common-mode transient immunity: 150 kV/µs
- High junction temperature operation: 125°C
- Default low output
- Safety and regulatory approvals (pending)
  - UL recognition per UL 1577
    - 5700 V rms for 1 minute duration
  - CSA Component Acceptance Notice 5A (pending)
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-11
    - V_{IORM} = 849 V peak
- Increased creepage wide body, 16-lead SOIC_IC

APPLICATIONS

- Switching power supplies
- Isolated IGBT/MOSFET gate drives
- Industrial inverters
- Gallium nitride (GaN)/silicon carbide (SiC) compatible

FUNCTIONAL BLOCK DIAGRAM

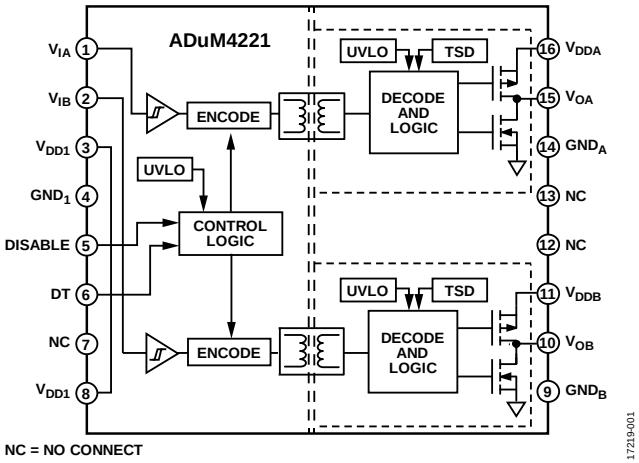

Figure 1.

GENERAL DESCRIPTION

The ADuM4221 is a 4 A isolated, half bridge gate driver that employs the Analog Devices, Inc., iCoupler® technology to provide independent and isolated high-side and low-side outputs. The ADuM4221 provides 5700 V rms isolation in the increased creepage wide body, 16-lead SOIC_IC package. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The isolators operate with a logic input voltage ranging from 2.5 V to 6.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM4221 offers the benefit of true, galvanic isolation between the input and each output.

The ADuM4221 has a built in overlap protection and allows for dead time adjustment. A single resistor between the dead time pin (DT) and the GND_1 pin sets the dead time on the secondary side between the high-side and the low-side outputs.

An internal thermal shutdown (TSD) sets outputs low if the internal temperature on the ADuM4221 exceeds the TSD temperature. As a result, the ADuM4221 provides reliable control over the switching characteristics of the insulated gate bipolar transistor (IGBT)/metal-oxide semiconductor field effect transistor (MOSFET) configurations over a wide range of positive or negative switching voltages.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

7/2020—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to GND_I, high-side voltages referenced to GND_A, GND_B, 2.5 V ≤ V_{DD1} ≤ 6.5 V, 4.5 V ≤ V_{DDA},V_{DDB} ≤ 35 V, and T_J = −40°C to +125°C, unless otherwise noted. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, and V_{DDA} and V_{DDB} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic Input Voltage	V_{DD1}	2.5		6.5	V	
Output Supply Voltage	V_{DDA}, V_{DDB}	4.5		35	V	
Input Supply Current, Quiescent	$I_{DD1 (Q)}$					
Input A High or Input B High			7.2	10	mA	
Both Inputs Low			1.4	2.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DD2 (Q)}$					
Output Channel						
High			1.4	2.6	mA	
Low			1.6	2.1	mA	
Input Currents	I_{IA}, I_{IB}	−1	+0.01	+1	µA	
Input Voltage						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DD1}			V	2.5 V ≤ V_{DD1} ≤ 5 V
		3.5			V	V_{DD1} > 5 V
Logic Low	V_{IL}			0.3 × V_{DD1}	V	2.5 V ≤ V_{DD1} ≤ 5 V
				1.5	V	V_{DD1} > 5 V
Undervoltage Lockout (UVLO)						
V_{DD1} Positive Going Threshold	$V_{VDD1UV+}$		2.45	2.5	V	
V_{DD1} Negative Going Threshold	$V_{VDD1UV-}$	2.3	2.35		V	
V_{DD1} Hysteresis	$V_{VDD1UVH}$		0.1		V	
V_{DDA} and V_{DDB} Positive Going Threshold	$V_{VDDAUV+}$,		4.4	4.5	V	Grade A
	$V_{VDDBUV+}$		7.3	7.5	V	Grade B
			11.3	11.6	V	Grade C
V_{DDA} and V_{DDB} Negative Going Threshold	$V_{VDDAUV-}$,	4.1	4.2		V	Grade A
	$V_{VDDBUV-}$	6.9	7.1		V	Grade B
		10.8	11.1		V	Grade C
V_{DDA} and V_{DDB} Hysteresis	$V_{VDDAUVH}$,		0.2		V	Grade A
	$V_{VDDBUVH}$		0.2		V	Grade B
			0.2		V	Grade C
TSD						
Positive Edge	T_{TSD_POS}		155		°C	
Hysteresis	T_{TSD_HYST}		30		°C	
Drive Strength						
Pull-Down Negative Metal Oxide Semiconductor (NMOS) On Resistance	R_{DSON_N}		0.6	1.6	Ω	Tested at 250 mA, V_{DDx} = 15 V
			0.6	1.6	Ω	Tested at 1 A, V_{DDx} = 15 V
Pull-Up Positive Metal Oxide Semiconductor (PMOS) On Resistance	R_{DSON_P}		0.8	1.8	Ω	Tested at 250 mA, V_{DDx} = 15 V
			0.8	1.8	Ω	Tested at 1 A, V_{DDx} = 15 V
Peak Current	I_{PEAK}		4		A	V_{DDA},V_{DDB} = 15 V, 2 Ω gate resistance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
Pulse Width		50			ns	Load capacitance (C_L) = 2.2 nF, V_{DD1} = 5 V, V_{DDA} and V_{DDB} = 15 V, external gate resistor (R_G) = 5.1 Ω
Propagation Delay[1]						C_L = 2.2 nF, V_{DD1} = 5 V, V_{DDA} and V_{DDB} = 15 V, and R_G = 5.1Ω
Rising Edge	t_{DLH}	19	25	33	ns	
Falling Edge	t_{DHL}	21	30	44	ns	
Time to Disable	t_{DIS}	21	25	44	ns	
Time to Enable	t_{EN}	19	25	33	ns	
Delay Skew[2]	t_{PSK}			22	ns	C_L = 2.2 nF, R_G = 5.1 Ω
Pulse Width Distortion	t_{PWD}		5	16	ns	C_L = 2.2 nF, V_{DD1} = 5 V, V_{DDA} and V_{DDB} = 15 V, R_G = 5.1 Ω
Channel to Channel Matching[3]	t_{PSKCD}		1.5	10	ns	C_L = 2.2 nF, V_{DD1} = 5 V, V_{DDA} and V_{DDB} = 15 V, see Figure 19
Output Rise and Fall Time (10% to 90%)	t_R/t_F	14	25	34	ns	C_L = 2.2 nF, V_{DD1} = 5 V, V_{DDA} and V_{DDB} = 15 V, R_G = 5.1 Ω, see Figure 26
Adjustable Dead Time	DT					C_L = 2.2 nF, V_{DD1} = 5 V, V_{DDA} and V_{DDB} = 15 V, R_G = 5.1 Ω
		1809	2320	2831	ns	Dead time resistor (R_{DT}) = 500 kΩ
		742	938	1135	ns	R_{DT} = 200 kΩ
		48	62	76	ns	R_{DT} = 10 kΩ

[1] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 26 for the waveforms of the propagation delay parameters.
[2] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 26 for the waveforms of the propagation delay parameters.
[3] Channel to channel matching is the absolute value of the difference in propagation delays between two channels on a single device.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM4221 is pending approval by the organizations listed in Table 3.

Table 3.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN VDE V 0884-11 (VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012
Single Protection, 5700 V rms Isolation Voltage	IEC 62368, Third Edition	Basic insulation, 900 V peak, V_{IOSM} = 9850 V peak	GB4943.1-2011
	Basic insulation at 830 V rms (1173 V peak)	Reinforced insulation, 849 V peak, V_{IOSM} = 8000 V peak	Basic insulation at 800 V rms (1131 V peak)
	Reinforced insulation at 415 V rms (586 V peak)		Reinforced insulation at 400 V rms (565 V peak)
	IEC 60601-1, Edition 3.1		
	Reinforced insulation (2 MOPP), 250 V rms (353V peak)		
	CSA 61010-1-12 and IEC 61010-1, Third Edition		
	Basic insulation at 300 V rms mains, 800 V secondary (1089 V peak)		
	Reinforced insulation at 300 V rms mains, 400 V secondary (565 V peak)		
File E214100	File 205078	File 2471900-4880-0003	File (pending)

[1] In accordance with UL 1577, each ADuM4221 is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.
[2] In accordance with DIN VDE V 0884-11, each ADuM4221 is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board, PCB (PCB Clearance)	L (PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Protective circuits ensure maintenance of the safety data.

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input to Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1019	V peak
Maximum Rated Transient Isolation Voltage		V_{IOTM}	8000	V peak
Surge Isolation Voltage		V_{IOSM}		
Basic	V peak = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time		9850	V peak
Reinforced	V peak = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time		8000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.77	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

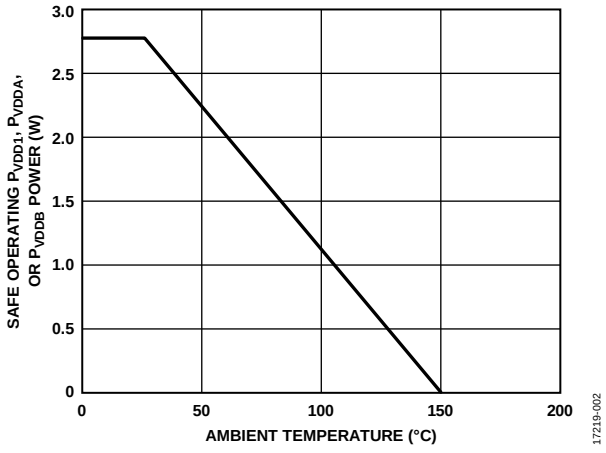


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
T_J	−40°C to +125°C
Supply Voltages	
V_{DD1}[1]	2.5 V to 6.5 V
V_{DDA} and V_{DDB}[2]	4.5 V to 35 V
Common-Mode Transient Immunity	
Static[3]	−150 kV/µs to +150 kV/µs
Dynamic[4]	−150 kV/µs to +150 kV/µs
Dead Time Resistor Range	10 kΩ to 500 kΩ

[1] Referenced to GND_1.
[2] Referenced to GND_A,GND_B.
[3] Static common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_A and GND_B with the inputs held either high or low such that the output voltage remains either above $0.8 \times V_{DDA}$ and V_{DDB} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.
[4] Dynamic common-mode transient immunity is defined as the largest dv/dt between GND_1 and GND_A and GND_B with the switching edge coincident with the transient test pulse. Operation with transients above recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Voltage Ranges	
Supply	
V_{DD1}	−0.2 V to +7 V
V_{DDA} and V_{DDB}	−0.3 V to +40 V
Input[1] (V_{IA}, V_{IB}, and DISABLE)	−0.3 V to +7 V
Output[2]	
V_{OA}	−0.3 V to V_{DDA} + 0.3 V
V_{OB}	−0.3 V to V_{DDB} + 0.3 V
V_{OA} Transient for 200 ns	−2 V to V_{DDA} + 0.3 V
V_{OB} Transient for 200 ns	−2 V to V_{DDB} + 0.3 V
Temperature Range	
Storage (T_{ST})	−55°C to +150°C
T_J	−40°C to +125°C
Common-Mode Transients[3] (CM_H, CM_L)	−200 kV/µs to +200 kV/µs

[1] Rating assumes V_{DD1} is above 2.5 V. V_{IA} and V_{IB} are rated up to 6.5 V when V_{DD1} is unpowered.
[2] Referenced to GND_2, maximum of 40 V.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top characterization parameter.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Unit
RI-16-2	45	16.67	°C/W

[1] 4-layer PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Rating	Unit	Constraint
AC Voltage			
Bipolar Waveform			
Basic Insulation	900	V peak	20 year minimum insulation lifetime per VDE-0884-11
Reinforced Insulation	849	V peak	20 year minimum insulation lifetime per VDE-0884-11
DC Voltage			
Basic Insulation	1660	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60664-1, Pollution Degree 2, Material Group I
Reinforced Insulation	830	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60664-1, Pollution Degree 2, Material Group I

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

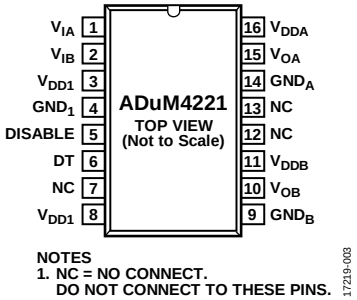


Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.[1]	Mnemonic	Description
1	V_{IA}	Logic Input A.
2	V_{IB}	Logic Input B.
3, 8	V_{DD1}	Input Supply Voltage.
4	GND_1	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. The DISABLE pin disables the isolator inputs and refresh circuits.
6	DT	Dead Time Control Input. The resistor connected from the DT pin to ground sets the dead time between the output transitions.
7, 12, 13	NC	No Connect. Do not connect to these pins.
9	GND_B	Ground Reference for Output B.
10	V_{OB}	Output B.
11	V_{DDB}	Output B Supply Voltage.
14	GND_A	Ground Reference for Output A.
15	V_{OA}	Output A.
16	V_{DDA}	Output A Supply Voltage.

[1] Pin 3 and Pin 8 are internally connected. Connecting both the V_{DD1} pins to the V_{DD1} input supply is recommended.

Table 11. Truth Table (Positive Logic with Dead Time)

DISABLE[1]	V_{IA} Input[1]	V_{IB} Input[1]	V_{DD1} State	V_{DDA} and V_{DDB} State	V_{OA} Output	V_{OB} Output	Notes
Low	Low	Low	Powered	Powered	Low	Low	Output transition begins after dead time expires
Low	Low	High	Powered	Powered	Low	High	Output transition begins after dead time expires
Low	High	Low	Powered	Powered	High	Low	Output transition begins after dead time expires
Low	High	High	Powered	Powered	Low	Low	Output transition begins after dead time expires
High	X	X	Powered	Powered	Low	Low	Device is disabled
X	X	X	Unpowered	Powered	Low	Low	Output returns to input state after V_{DD1} power restoration
X	X	X	Powered	Unpowered	Low	Low	Output remains low

[1] X means don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

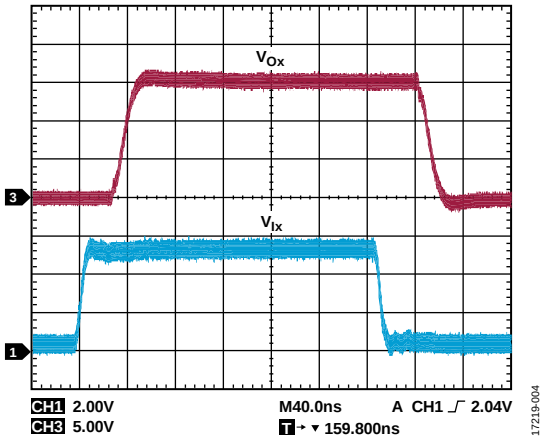


Figure 4. Output Waveform for 2 nF Load and 3.9 Ω Series Gate Resistor with 15 V Output Supply

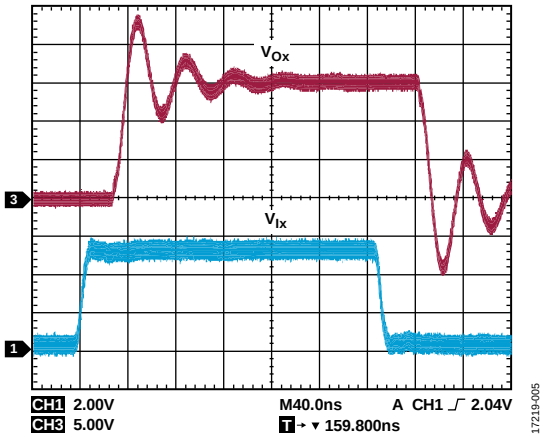


Figure 5. Output Waveform for 2 nF Load and 0 Ω Series Gate Resistor with 15 V Output Supply

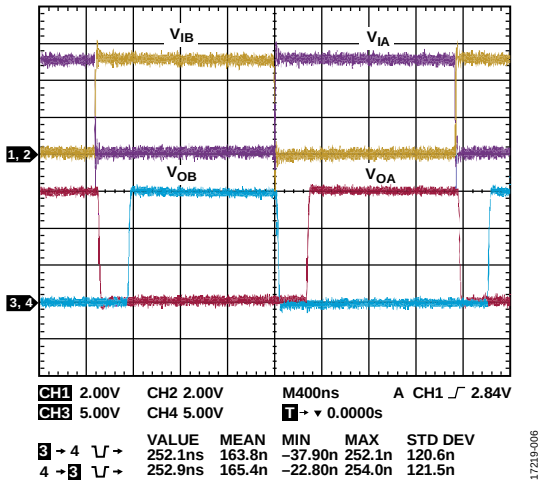


Figure 6. Dead Time Operation Between Input and Output with 50 kΩ Dead Time Resistor

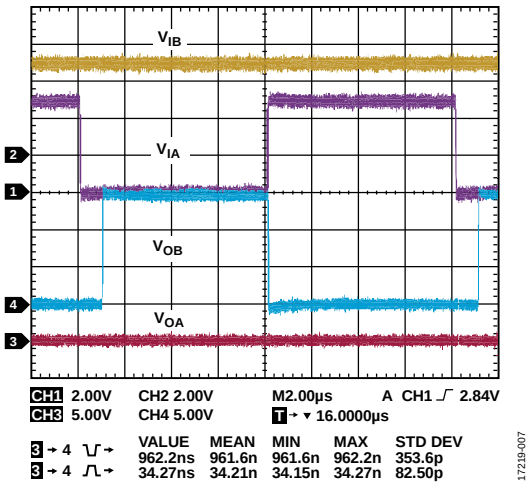


Figure 7. Dead Time Operation Between Input and Output with 200 kΩ Dead Time Resistor and One Input Held High

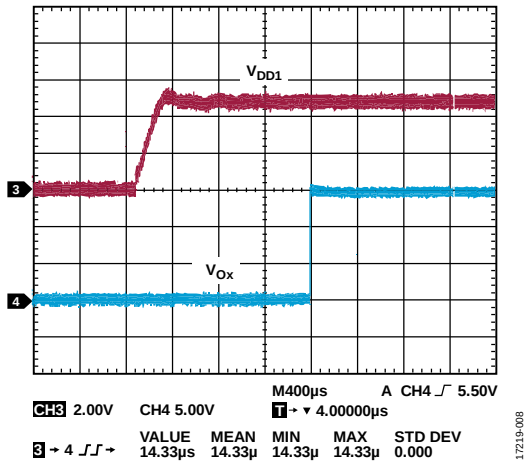


Figure 8. Typical V_{DD1} Delay to Output Waveform, $V_{Ix} = V_{DD1}$

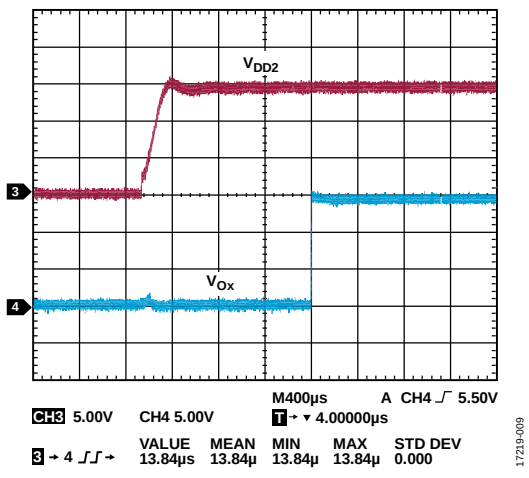


Figure 9. Typical V_{DD2} Delay to Output Waveform, $V_{Ix} = V_{DD1}$ (V_{DD2} Refers to V_{DDA} or V_{DDB})

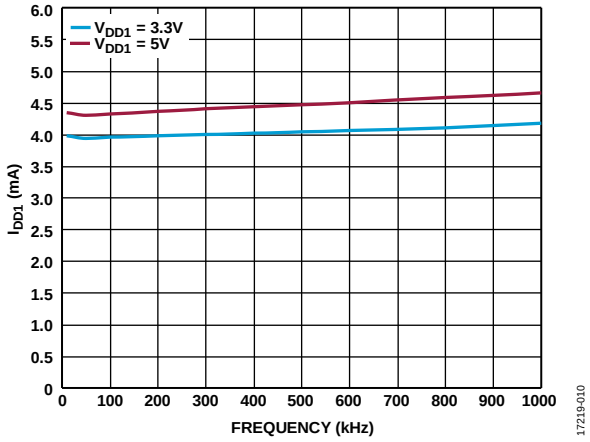


Figure 10. V_{DD1} Current (I_{DD1}) vs. Frequency for V_{DD1} = 3.3 V and V_{DD1} = 5 V, 50% Duty Cycle

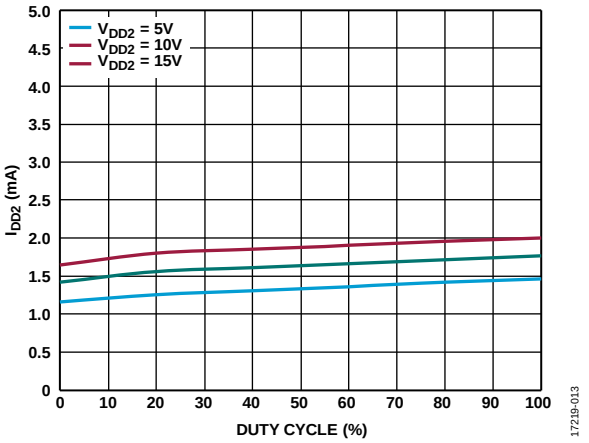


Figure 13. I_{DD2} vs. Duty Cycle for V_{DD2} = 5 V, V_{DD2} = 10 V, and V_{DD2} = 15 V, V_{DD1} = 5 V (V_{DD2} Refers to V_{DDA} or V_{DDB})

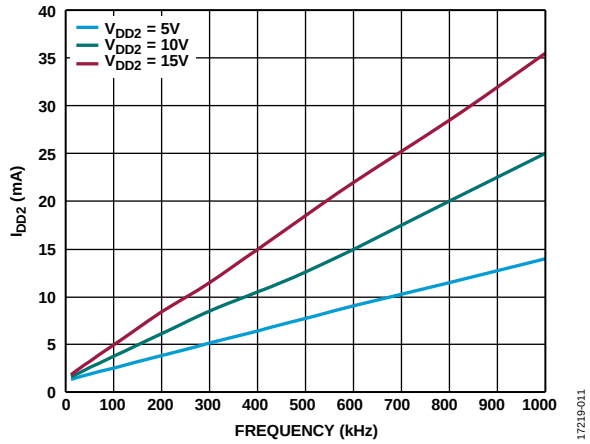


Figure 11. V_{DD2} Current (I_{DD2}) vs. Frequency for V_{DD2} = 5 V, V_{DD2} = 10 V, and V_{DD2} = 15 V, 50% Duty Cycle, 2 nF Load (V_{DD2} Refers to V_{DDA} or V_{DDB})

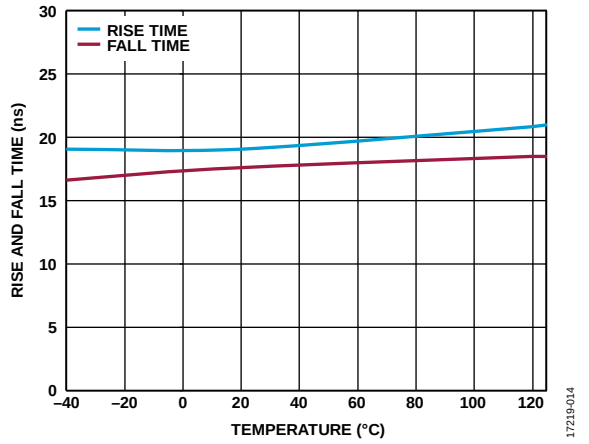


Figure 14. Rise and Fall Time vs. Temperature with a 3.9 Ω Series Gate Resistor for a 2 nF Load and a 15 V Output Supply

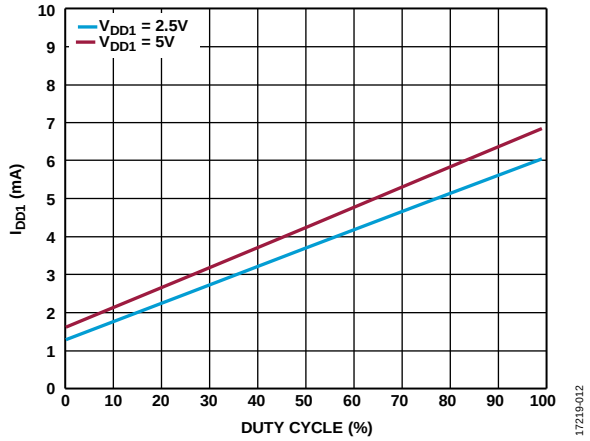


Figure 12. I_{DD1} vs. Duty Cycle for V_{DD1} = 2.5 V and V_{DD1} = 5 V, V_{DD2} = 15 V (V_{DD2} Refers to V_{DDA} or V_{DDB})

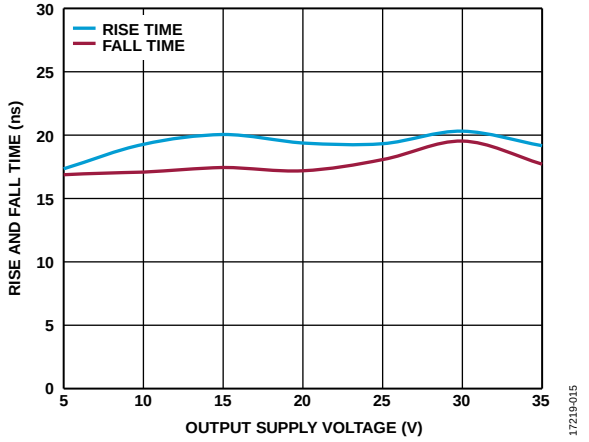


Figure 15. Rise and Fall Time vs. Output Supply Voltage with a 3.9 Ω Series Gate Resistor for a 2 nF Load

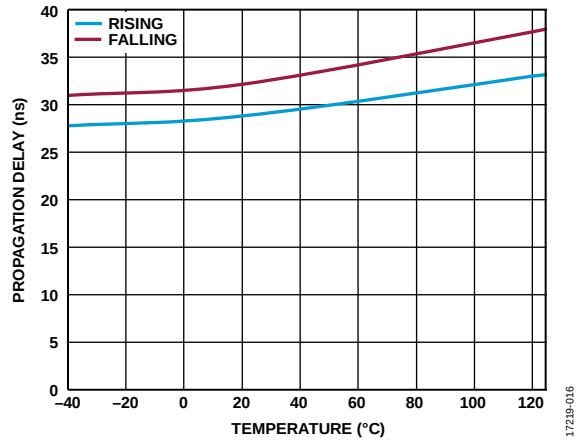


Figure 16. Propagation Delay vs. Temperature

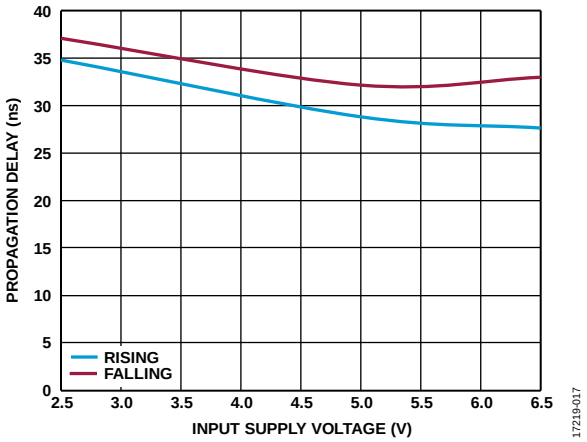


Figure 17. Propagation Delay vs. Input Supply Voltage, Rising and Falling, V_{DD2} = 15 V (V_{DD2} Refers to V_{DDA} or V_{DDB})

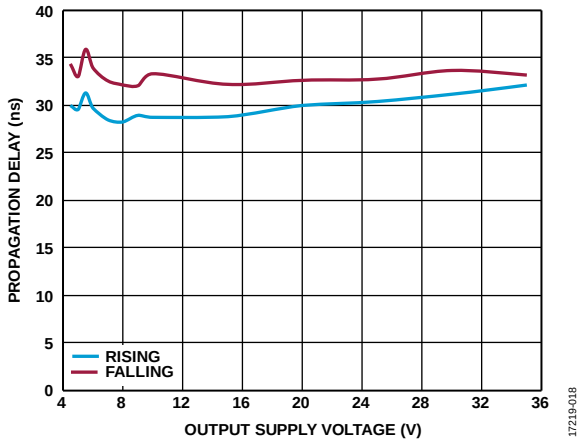


Figure 18. Propagation Delay vs. Output Supply Voltage, Rising and Falling, V_{DD1} = 5 V

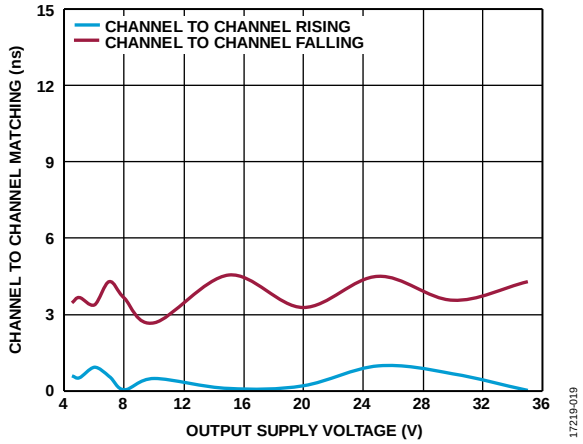


Figure 19. Channel to Channel Matching vs. Output Supply Voltage, Rising and Falling

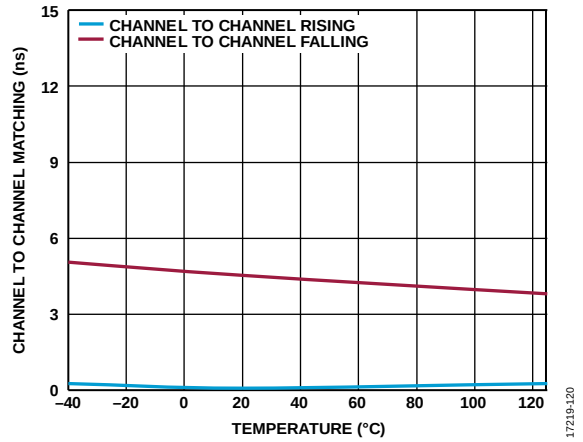


Figure 20. Channel to Channel Matching vs. Temperature, Rising and Falling, V_{DD2} = 15 V (V_{DD2} Refers to V_{DDA} or V_{DDB})

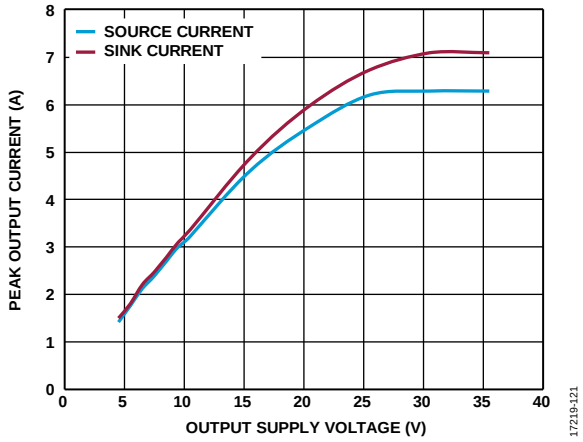


Figure 21. Peak Output Current vs. Output Supply Voltage with a 2.2 Ω Series Gain Resistor

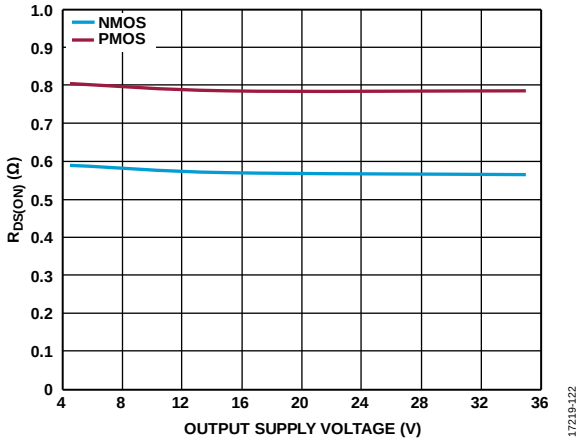


Figure 22. Output Resistance ($R_{DS(ON)}$) vs. Output Supply Voltage for NMOS and PMOS, V_{DD1} = 5 V

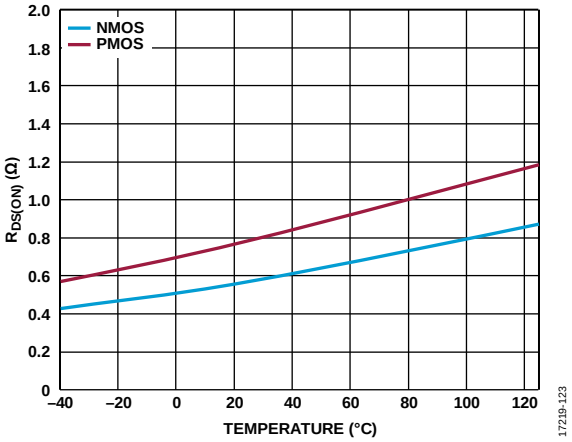


Figure 23. $R_{DS(ON)}$ vs. Temperature for NMOS and PMOS

THEORY OF OPERATION

Gate drivers are required where fast rise times of switching device gates are desired. The gate signal for most enhancement type power devices is referred to a source or emitter node. The gate driver must have the ability to follow this source or emitter node, necessitating isolation between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a CMOS output reduce the total delay time and increase the final drive strength of the driver.

The ADuM4221 achieves isolation between the control side and output side of the gate driver by means of a high frequency carrier that transmits data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation.

The encoding scheme used by the ADuM4221 is a positive logic on/off keying (OOK), a high signal transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices, driving in situations where shoot through conditions can exist. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques such as differential coil layout. Figure 24 illustrates the encoding used by the ADuM4221.

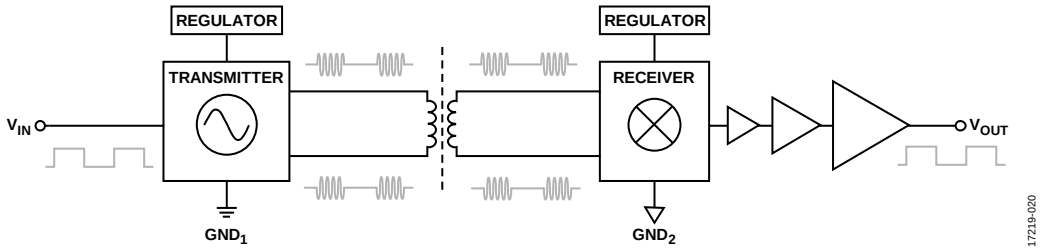


Figure 24. Operational Block Diagram of OOK Encoding (V_{IN} Is the Input Voltage, and V_{OUT} Is the Output Voltage.)

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4221 requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins, as shown in Figure 25. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass. On the output power supply pin, V_{DDA} or V_{DDB}, it is also recommended to add a 10 µF capacitor to provide the charge required to drive the gate capacitance at the ADuM4221 outputs. On the output supply pin, avoid the use of vias with a bypass capacitor or use multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must be as short as possible.

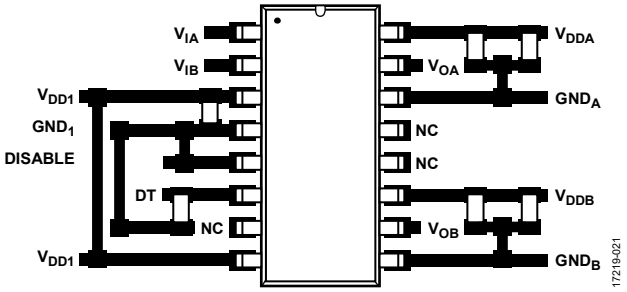


Figure 25. Recommended PCB Layout

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay parameter describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM4221 specifies the rising edge propagation delay (t_{DLH}) as the time between the rising input high logic threshold (V_{IH}) to the output rising (t_R) 10% threshold (see Figure 26). Likewise, the falling edge propagation delay (t_{DHL}) is the time between the input falling logic low threshold (V_{IL}) and the output falling (t_F) 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

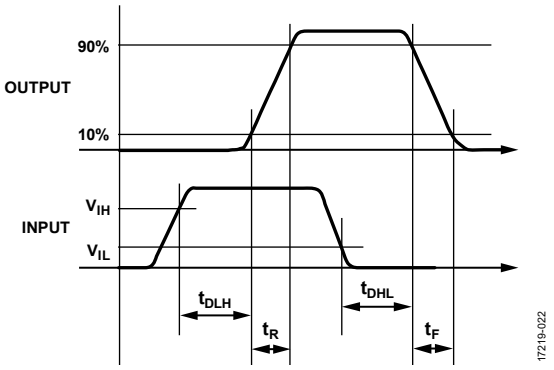


Figure 26. Propagation Delay Parameters

Channel to channel matching is the maximum amount that the propagation delay differs between channels within a single component.

Propagation delay skew is the maximum amount that the propagation delay differs between multiple components operating under the same conditions.

PEAK CURRENT RATING

The ADuM4221 has two output channels, and each channel connects to the gate of the power device through an external series gate resistor. The output driver MOSFETs of the gate driver IC can source or sink more than 6 A (per V_{OA} and V_{OB}). In a practical application, to control the drive strength and to spread the power dissipation of driving the gate to outside of the gate driver IC, standard external series gate resistors are used. The output current of the gate driver is shown in Figure 21 of the Typical Performance Characteristics section.

PROTECTION FEATURES

TSD

If the internal temperature of the ADuM4221 exceeds 155°C (typical), the device enters TSD. During the TSD time, the gate drive is disabled. When TSD occurs, the device does not leave TSD until the internal temperature drops below 125°C (typical), at which time, the device exits shutdown.

UVLO

The ADuM4221 has UVLO protections for both the primary and secondary side of the device. If either the primary or secondary side voltages are below the falling edge UVLO, the device outputs a low signal. After the ADuM4221 is powered above the rising edge UVLO threshold, the device outputs the signal found at the input. To account for small voltage source ripple, hysteresis is built into the UVLO. The primary side UVLO thresholds are common among all models.

OUTPUT LOAD CHARACTERISTICS

The output signals depend on the characteristics of the output load, which is typically an N channel MOSFET. The driver output response to an N channel MOSFET load with a gate voltage (V_{GATE}) can be modeled with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 27.

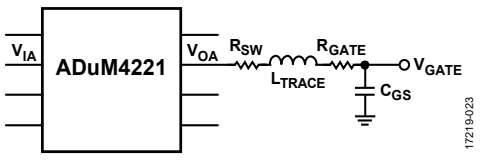


Figure 27. Resistor, Inductor, and Capacitor (RLC) Model of the Gate of an N Channel MOSFET

R_{SW} is the switch resistance of the internal driver output, which is approximately 2 Ω. R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of approximately 1 Ω and a C_{GS} of between 2 nF and 10 nF. L_{TRACE} is the inductance of the PCB trace, typically a value of 5 nH or less for a well designed layout with a short and wide connection from the ADuM4221 output to the gate of the MOSFET. The following equation defines the Q factor of the RLC circuit, which indicates how the output responds to a step change. For a well damped output, Q is less than 1.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

Output ringing is reduced by adding a series gate resistance to dampen the response. The waveforms in Figure 4 show a correctly damped example with a 2 nF load and a 3.9 Ω external series gate resistor. The waveforms in Figure 5 show an underdamped example with a 2 nF load and a 0 Ω external series gate resistor.

ADJUSTABLE DEAD TIME CONTROL

The ADuM4221 includes overlap protection such that the gate driver outputs (V_{OA} and V_{OB}) cannot simultaneously go high even if both inputs are high. Additionally, the ADuM4221 also has a dead time control pin (DT) that can adjust the delay between the output high-side and low-side transitions by using a single resistor between the DT pin and ground (see Figure 30). The relation between R_{DT} and the obtained dead time is shown in Figure 28.

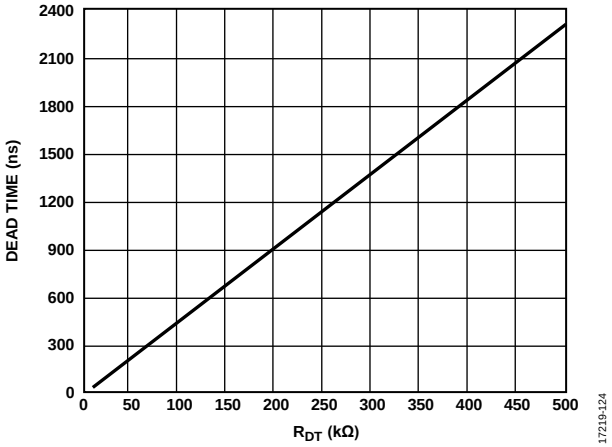


Figure 28. Dead Time vs. Dead Time Resistor

Use the following equation, to calculate the required amount of dead time:

$$DT\,(\text{ns}) \approx 5 \times R_{DT}\,(\text{k}\Omega)$$

The V_{Ox} pin reacts to the V_{Ix} pin depending on the dead time value set by the R_{DT} resistor. The DT pin controls the edge transitions between V_{OA} and V_{OB}. Dead time only affects the rising edge transition of the gate drive signal, and dead time operation is shown in Figure 29.

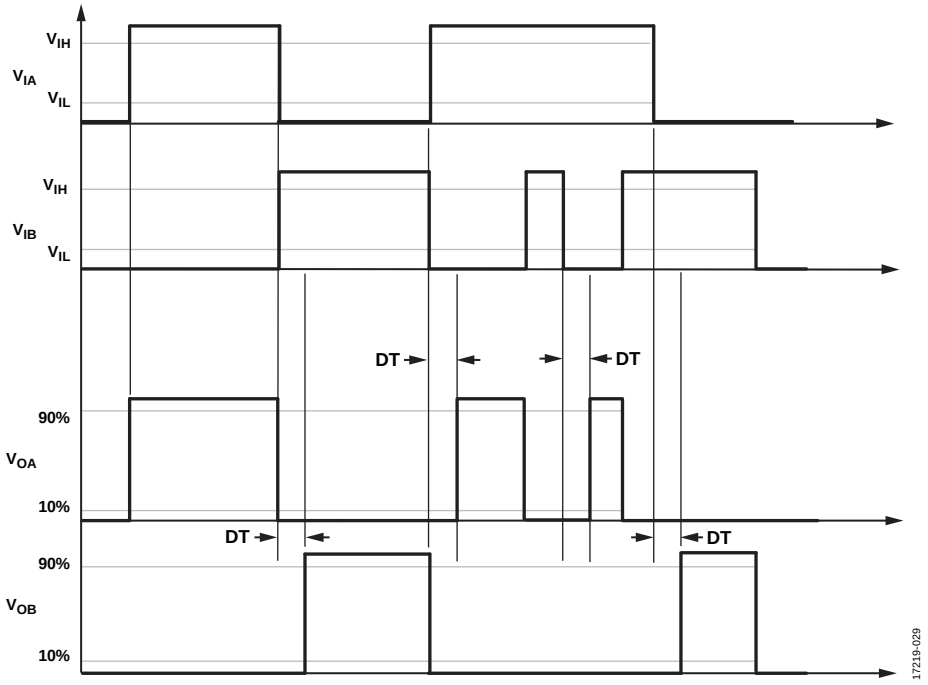


Figure 29. Dead Time Operation for Different Input Transitions

BOOT STRAPPED, HALF BRIDGE OPERATION

The ADuM4221 is well suited for operating two output gate signals referenced to separate grounds, as in the case for a half bridge configuration. Because isolated auxiliary supplies are often expensive, it is beneficial to reduce the amount of supplies.

One method to reduce power supplies is to use a boot strapped configuration for the high-side supply of the ADuM4221. In this topology, the decoupling capacitor (C_A) acts as the energy storage for the high-side supply and is filled whenever the low-side switch is closed, bringing GND_A to GND_B (see Figure 30). During the C_A charging time, control the dv/dt of the V_{DDA} voltage to reduce the possibility of glitches on the output. To control the dv/dt of the V_{DDA} voltage, introduce a series resistance (R_{BOOT}) into the C_A charging path.

Note that in Figure 30, D_{BOOT} is the bootstrapped diode, C_{DD1} is the decoupling capacitor on the input side, and C_B is the decoupling capacitor for the driver low-side supply.

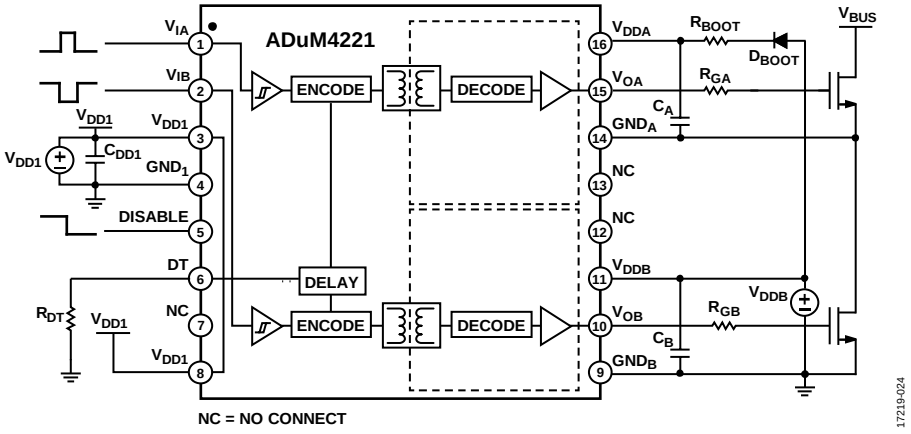


Figure 30. Circuit of Bootstrapped Half Bridge Operation

POWER DISSIPATION

When driving a MOSFET or IGBT gate, the driver must dissipate power. This power is not insignificant and can lead to TSD if considerations are not made. The gate of an IGBT can be approximately simulated as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance of a given MOSFET or IGBT, C_{ISS}, and multiply this capacitance by a factor of 3 to 5 to arrive at a conservative estimate of the approximate load being driven. With this value, the estimated total power dissipation in the system due to the switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DD2} - GND_2)^2 \times f_{SW}$$

where:
$C_{EST} = C_{ISS} \times 5$.
f_{SW} is the switching frequency of the IGBT.

Alternately, use the gate charge as follows:

$$P_{DISS} = Q_G \times (V_{DD2} - GND_2) \times f_{SW}$$

where Q_G is the total gate charge of the device being driven. This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4221device.

$$P_{DISS\_ADuM4221} = P_{DISS} \times 0.5(R_{DSON\_P}/(R_{GON} + R_{DSON\_P}) + 0.5(R_{DSON\_N}/(R_{GOFF} + R_{DSON\_N}))$$

Take the power dissipation found inside the chip and multiply it by θ_{JA} to see the rise above ambient temperature that the ADuM4221 experiences, then multiplied this value by two because there are two channels.

$$T_{ADuM4221} = \theta_{JA} \times 2 \times P_{DISS\_ADuM4221} + T_A$$

For the device to remain within specification, $T_{ADuM4221}$ must not exceed 125°C. If $T_{ADuM4221}$ exceeds the TSD rising edge, the device enters TSD, and the output remains low until the TSD falling edge is crossed.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM4221 is resistant to external magnetic fields. The limitation on the ADuM4221 magnetic field immunity is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which falsely sets or resets of the decoder can occur (see Figure 31 and Figure 32).

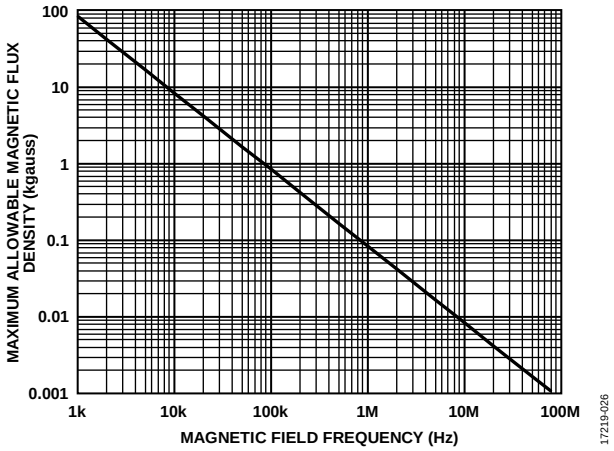


Figure 31. Maximum Allowable External Magnetic Flux Density

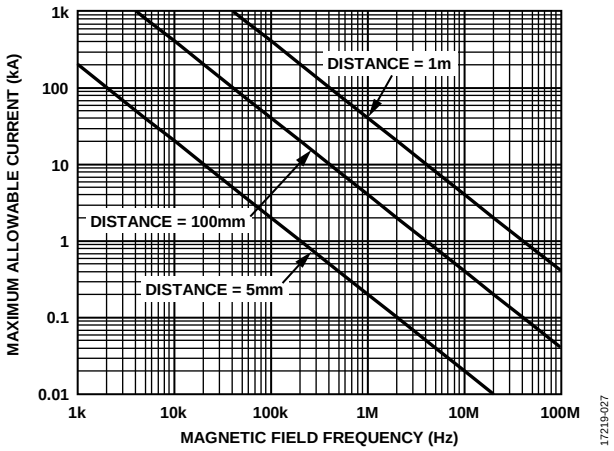


Figure 32. Maximum Allowable Current for Various Current to ADuM4221 Spacings

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4221.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values detailed in Table 9 summarize the peak voltage for 20 years of service life for a bipolar ac operating condition, and the maximum CSA and VDE approved working voltages. In many cases, the approved working voltage is higher than the 20 year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4221 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 33, Figure 34, and Figure 35 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst condition for *i*Coupler products and is the 20 year operating lifetime that Analog Devices recommends for the maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. Unipolar ac or dc voltage operation allows operation at higher working voltages while still achieving a 20 year service life. Any cross insulation voltage waveform that does not conform to Figure 34 or Figure 35 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 20 year lifetime voltage value listed in Table 9.

The voltage presented in Figure 34 is shown as sinusoidal for illustration purposes only. This voltage is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

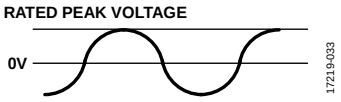


Figure 33. Bipolar AC Waveform

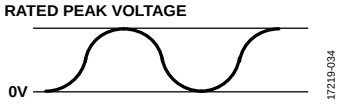


Figure 34. Unipolar AC Waveform

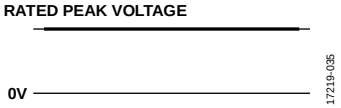
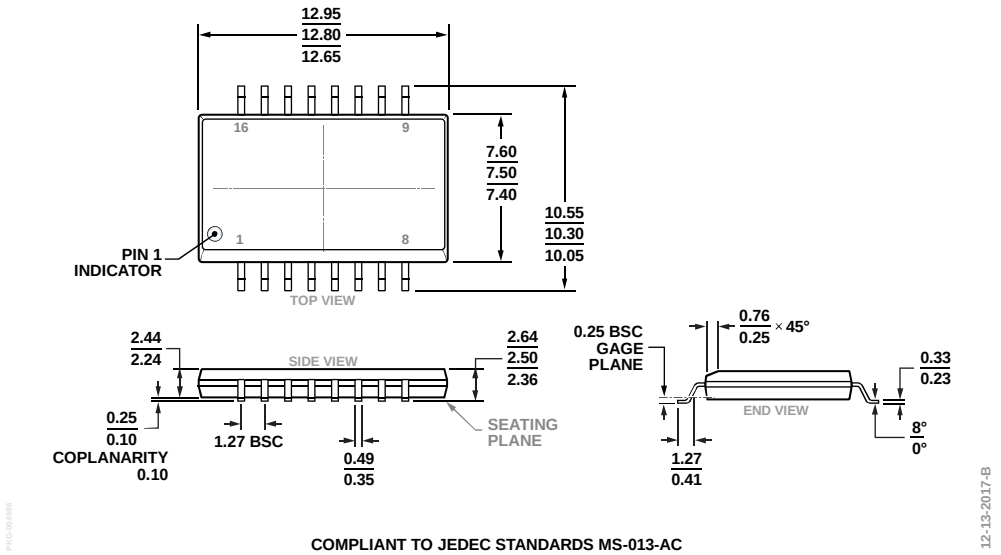


Figure 35. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC

Figure 36. 16-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]
(RI-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Inputs	Minimum Output Voltage (V)	Adjustable Dead Time	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuM4221ARIZ	V_{IA}, V_{IB}	4.5	Yes	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221ARIZ-RL	V_{IA}, V_{IB}	4.5	Yes	−40°C to +125°C	16-Lead SOIC_IC, 13″ Tape and Reel	RI-16-2	1,000
ADuM4221BRIZ	V_{IA}, V_{IB}	7.5	Yes	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221BRIZ-RL	V_{IA}, V_{IB}	7.5	Yes	−40°C to +125°C	16-Lead SOIC_IC, 13″ Tape and Reel	RI-16-2	1,000
ADuM4221CRIZ	V_{IA}, V_{IB}	11.6	Yes	−40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221CRIZ-RL	V_{IA}, V_{IB}	11.6	Yes	−40°C to +125°C	16-Lead SOIC_IC, 13″ Tape and Reel	RI-16-2	1,000
EVAL-ADuM4221EBZ					Evaluation Board		

[1] Z = RoHS Compliant Part.

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- Excess Inventory Management