THE DATASHEET OF

AD5612YKSZ-2500RL7

2.7 V to 5.5 V, <100 µA, 8-/10-/12-Bit *nano*DACs with I²C Compatible Interface in LFCSP and SC70

Data Sheet

AD5602/AD5612/AD5622

FEATURES

- Single 8-, 10-, 12-bit DACs, 2 LSB INL
- 6-lead LFCSP and SC70 packages
- Micropower operation: 100 µA maximum at 5 V
- Power down to <150 nA at 3 V
- 2.7 V to 5.5 V power supply
- Guaranteed monotonic by design
- Power-on reset to 0 V with brownout detection
- 3 power-down functions
- I²C compatible serial interface supports standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes
- On-chip output buffer amplifier, rail-to-rail operation

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

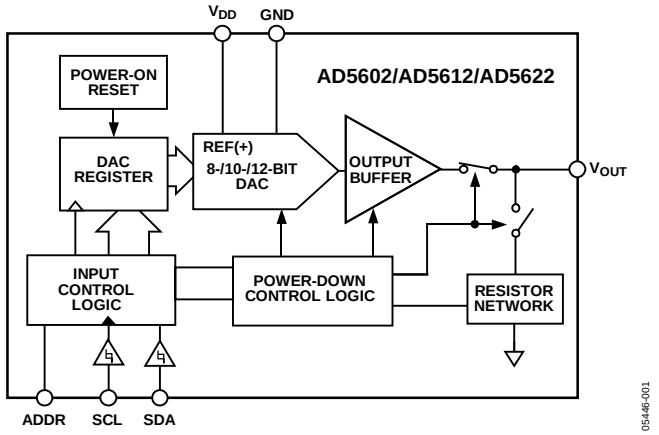

Figure 1.

Table 1. Related Devices

Device No.	Description
AD5601/AD5611/AD5621	2.7 V to 5.5 V, <100 µA, 8-, 10-, 12-bit *nano*DAC with SPI interface in tiny LFCSP and SC70 packages

GENERAL DESCRIPTION

The AD5602/AD5612/AD5622, members of the *nano*DAC® family, are single 8-, 10-, 12-bit buffered voltage-out digital-to-analog converters (DAC) that operate from a single 2.7 V to 5.5 V supply, consuming <100 µA at 5 V. These DACs come in tiny LFCSP and SC70 packages. Each DAC contains an on-chip precision output amplifier that allows rail-to-rail output swing to be achieved.

The AD5602/AD5612/AD5622 use a 2-wire I²C compatible serial interface that operates in standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes.

The references for AD5602/AD5612/AD5622 derive from the power supply inputs to give the widest dynamic output range. Each device incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place to the device. The devices contain a power-down feature that reduces the current consumption of the devices to <150 nA at 3 V and provides software selectable output loads while in power-down mode. The devices are put into power-down mode over the serial interface. The low power consumption of the AD5602/AD5612/AD5622 in normal operation makes them ideally suited for use in portable, battery operated equipment. The typical power consumption is 0.4 mW at 5 V.

PRODUCT HIGHLIGHTS

1. Available in 6-lead LFCSP and SC70 packages.
2. Maximum 100 µA power consumption, single-supply operation. These devices operate from a single 2.7 V to 5.5 V supply, typically consuming 0.2 mW at 3 V and 0.4 mW at 5 V, making them ideal for battery-powered applications.
3. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a typical slew rate of 0.5 V/µs.
4. Reference derived from the power supply.
5. Standard, fast, and high speed mode I²C interface.
6. Designed for very low power consumption.
7. Power-down capability. When powered down, the DAC typically consumes <150 nA at 3 V.
8. Power-on reset and brownout detection.

Rev. E
Document Feedback

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5/2012—Rev. B to Rev. C

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8/2005—Rev. 0 to Rev. A

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6/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A, B, W, Y Versions[1] Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					DAC output unloaded
Resolution				Bits	
AD5602	8				
AD5612	10				
AD5622	12				
Relative Accuracy[2]					
AD5602			±0.5	LSB	B, Y versions
AD5612			±0.5	LSB	B, Y versions
			±4	LSB	A version
AD5622			±2	LSB	B, Y versions
			±6	LSB	A, W versions
Differential Nonlinearity[2]			±1	LSB	Guaranteed monotonic by design
Zero Code Error		0.5	10	mV	All 0s loaded to DAC register
Offset Error		±0.063	±10	mV	
Full-Scale Error		0.5		mV	All 1s loaded to DAC register
Gain Error		±0.0004	±0.037	% of FSR	
Zero Code Error Drift		5		μV/°C	
Gain Temperature Coefficient		2		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		6	10	μs	Code ¼ to ¾
Slew Rate		0.5		V/μs	
Capacitive Load Stability		470		pF	$R_L = \infty$
		1000		pF	R_L = 2 kΩ
Output Noise Spectral Density		120		nV/Hz	DAC code = midscale, 10 kHz
Noise		2			DAC code = midscale, 0.1 Hz to 10 Hz bandwidth
Digital-to-Analog Glitch Impulse		5		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.2		nV-sec	
DC Output Impedance		0.5		Ω	
Short Circuit Current		15		mA	V_{DD} = 3 V/5 V
LOGIC INPUTS (SDA, SCL)					
I_{IN}, Input Current			±1	μA	
V_{INL}, Input Low Voltage			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage	0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			V	
LOGIC OUTPUTS (OPEN DRAIN)					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating State Leakage Current			±1	μA	
Floating State Output Capacitance		2		pF	

Parameter	A, B, W, Y Versions[1] Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)					DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		75	100	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		60	90	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 4.5 V to 5.5 V		0.3	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.15	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}		96		%	I_{LOAD} = 2 mA, V_{DD} = 5 V

[1] Temperature ranges for A, B versions: −40°C to +125°C, typical at 25°C.
[2] Linearity calculated using a reduced code range 64 to 4032.
[3] Guaranteed by design and characterization, not production tested.

I²C TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz, unless otherwise noted.[1]

Table 3.

Parameter	Test Conditions/Comments[2]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
f_{SCL}[3]	Standard mode		100	KHz	Serial clock frequency
	Fast mode		400	KHz	
	High speed mode, C_B = 100 pF		3.4	MHz	
	High speed mode, C_B = 400 pF		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode, C_B = 100 pF	60		ns	
	High speed mode, C_B = 400 pF	120		ns	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode, C_B = 100 pF	160		ns	
	High speed mode, C_B = 400 pF	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High speed mode, C_B = 100 pF	0	70	ns	
	High speed mode, C_B = 400 pF	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	

Parameter	Test Conditions/Comments[2]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{SP}[4]	Fast mode	0	50	ns	Pulse width of spike suppressed
	High speed mode	0	10	ns	

[1] See Figure 2. High speed mode timing specification applies to the AD5602-1/AD5612-1/AD5622-1 only. Standard and fast mode timing specifications apply to the AD5602-1/AD5612-1/AD5622-1 and the AD5602-2/AD5612-2/AD5622-2.
[2] C_B refers to the capacitance on the bus line.
[3] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the device.
[4] Input filtering on the SCL and SDA inputs suppress noise spikes that are less than 50 ns for fast mode or 10 ns for high speed mode.

TIMING DIAGRAM

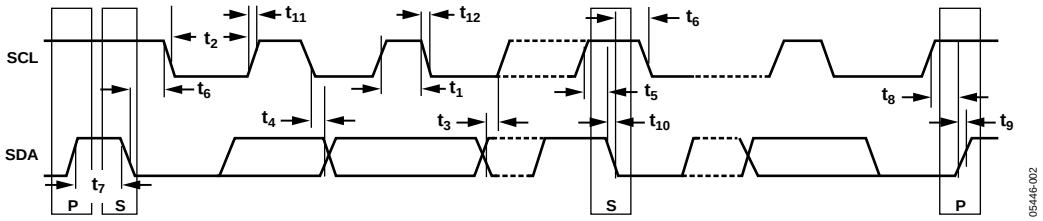

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to + 7.0 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +160°C
Maximum Junction Temperature	150°C
SC70 Package	
θ_{JA} Thermal Impedance	332°C/W
θ_{JC} Thermal Impedance	120°C/W
LFCSP Package	
θ_{JA} Thermal Impedance	95°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	2.0 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

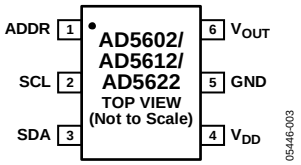

Figure 3. SC70 Pin Configuration

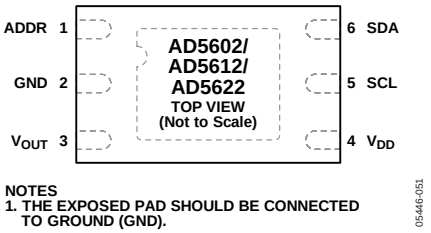

Figure 4. LFCSP Pin Configuration

Table 5. SC70 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 7).
2	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
3	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that is pulled to the supply with an external pull-up resistor.
4	V_{DD}	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V, and V_{DD} are decoupled to GND.
5	GND	Ground. The ground reference point for all circuitry on the devices.
6	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.

Table 6. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 7).
2	GND	Ground. The ground reference point for all circuitry on the device.
3	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
4	V_{DD}	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V, and V_{DD} are decoupled to GND.
5	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
6	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that are pulled to the supply with an external pull-up resistor.
	EPAD	Exposed Pad. The exposed pad is connected to ground (GND).

TYPICAL PERFORMANCE CHARACTERISTICS

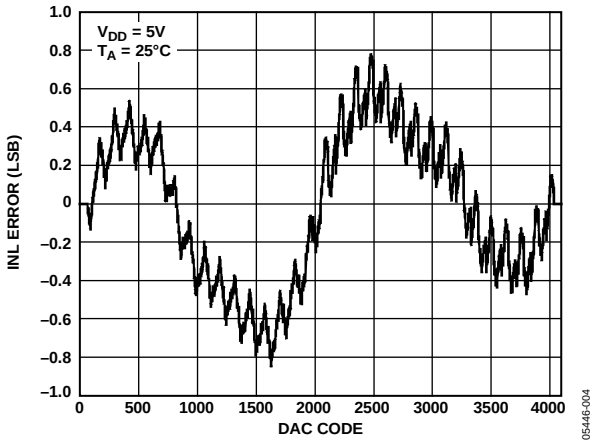

Figure 5. Typical AD5622 Integral Nonlinearity Error

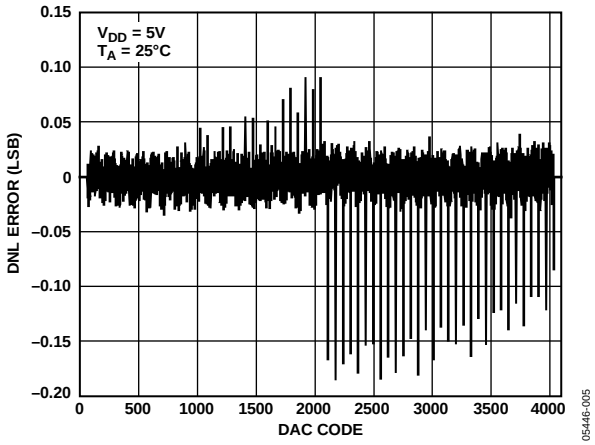

Figure 6. Typical AD5622 Differential Nonlinearity Error

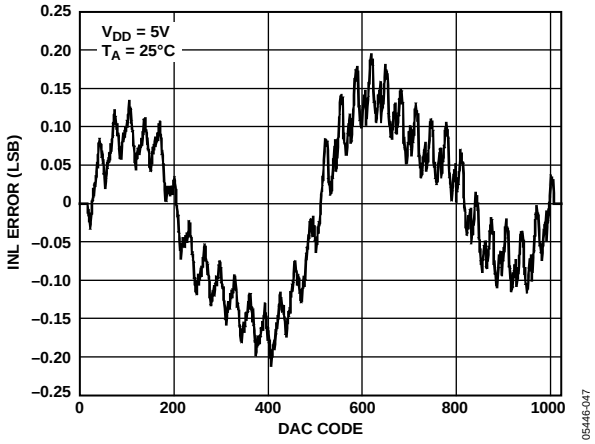

Figure 7. Typical AD5612 Integral Nonlinearity Error

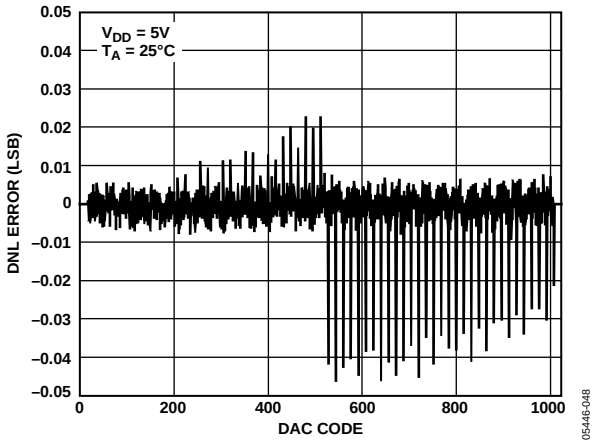

Figure 8. Typical AD5612 Differential Nonlinearity Error

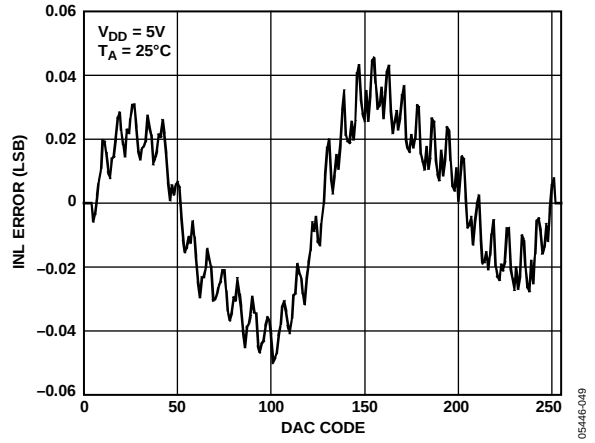

Figure 9. Typical AD5602 Integral Nonlinearity Error

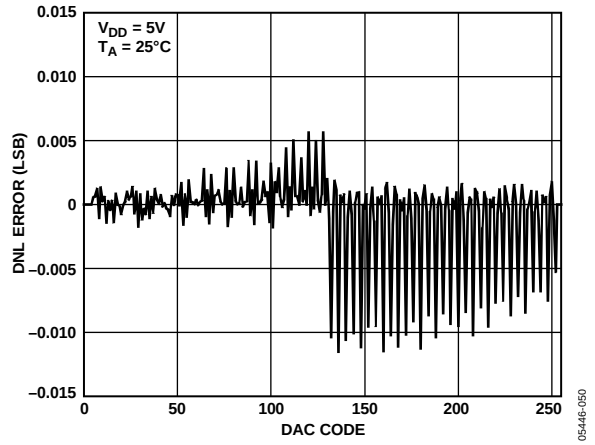

Figure 10. Typical AD5602 Differential Nonlinearity Error

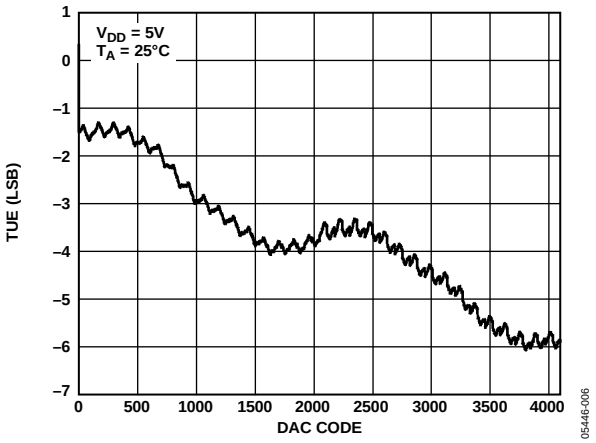

Figure 11. Typical AD5622 Total Unadjusted Error

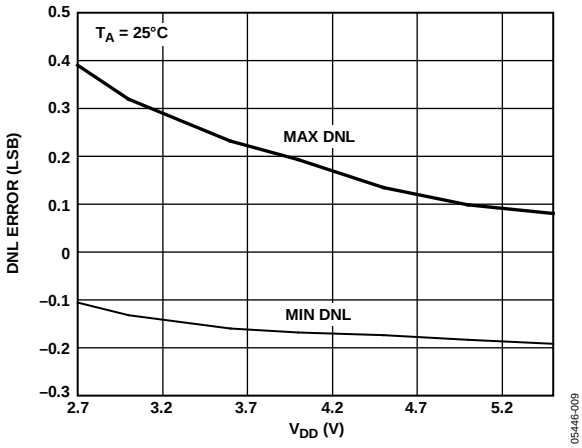

Figure 14. AD5622 DNL Error vs. Supply

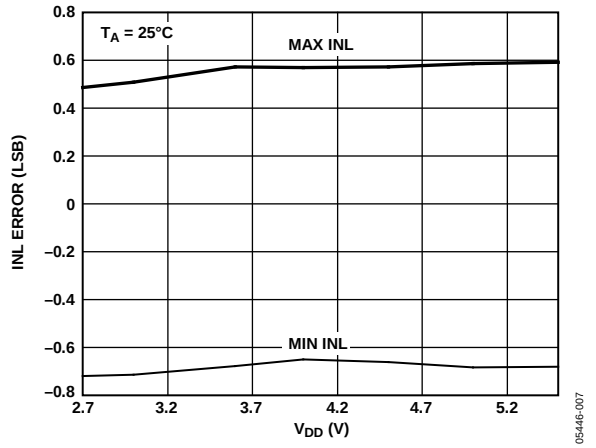

Figure 12. AD5622 INL Error vs. Supply

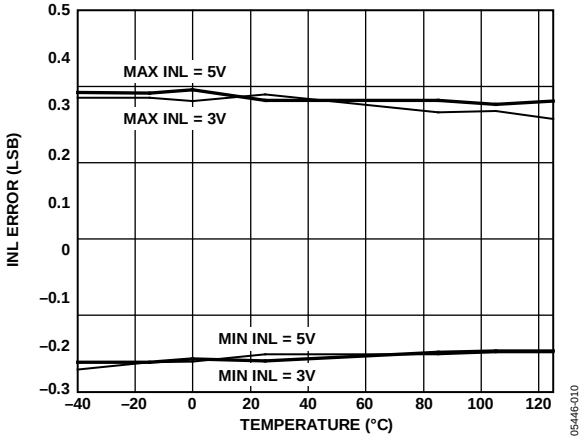

Figure 15. AD5622 INL Error vs. Temperature (3 V/5 V Supply)

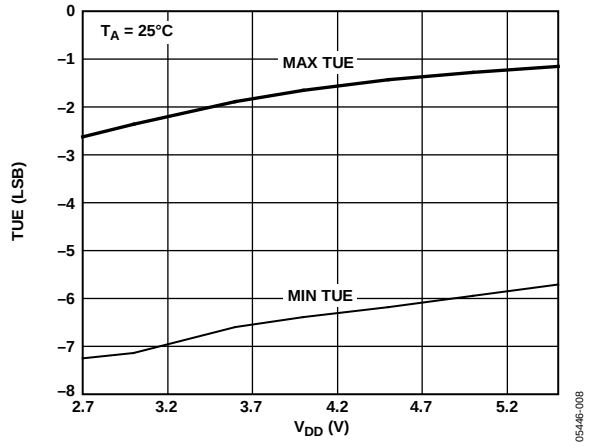

Figure 13. AD5622 Total Unadjusted Error vs. Supply

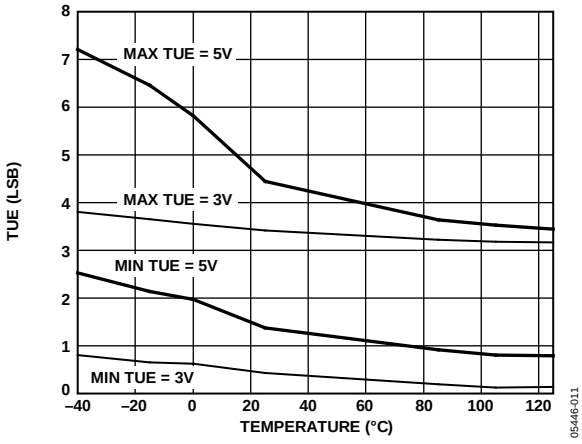

Figure 16. AD5622 Total Unadjusted Error vs. Temperature (3 V/5 V Supply)

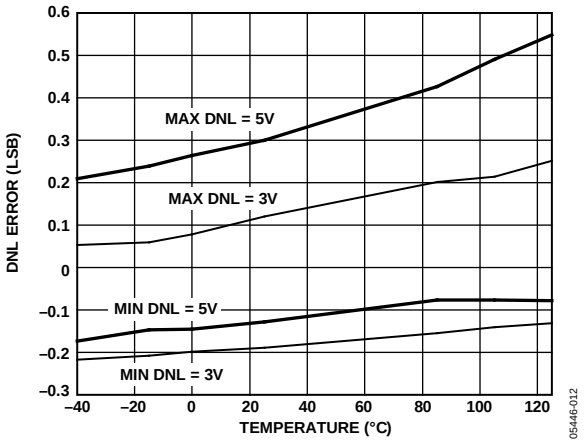

Figure 17. AD5622 DNL Error vs. Temperature (3 V/5 V Supply)

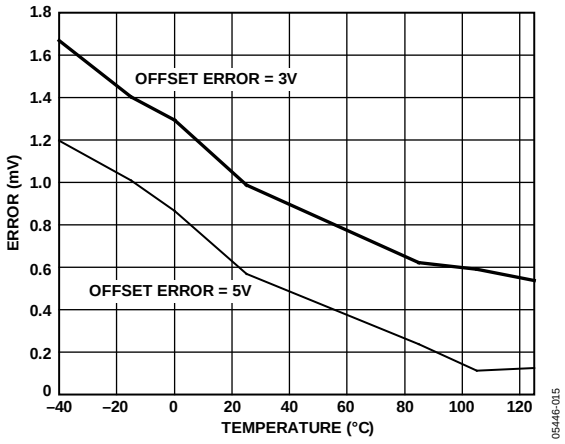

Figure 20. Offset Error vs. Temperature (3 V/5 V Supply)

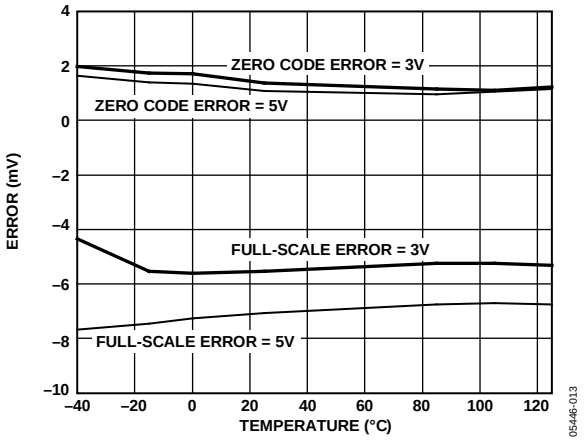

Figure 18. Zero Code/Full-Scale Error vs. Temperature (3 V/5 V Supply)

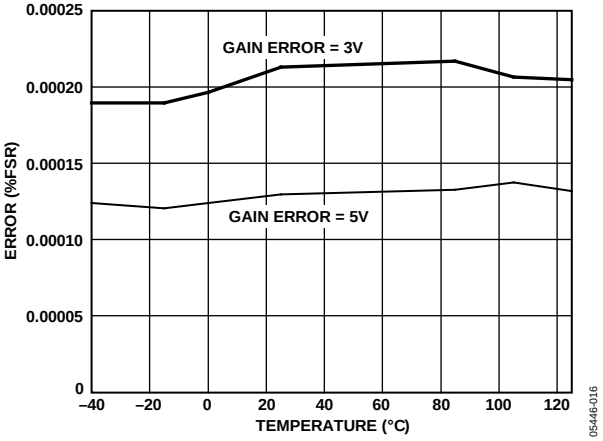

Figure 21. Gain Error vs. Temperature (3 V/5 V Supply)

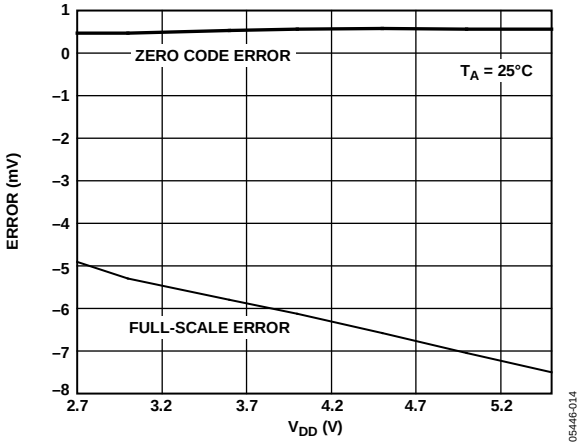

Figure 19. Zero Code/Full-Scale Error vs. Supply Voltage

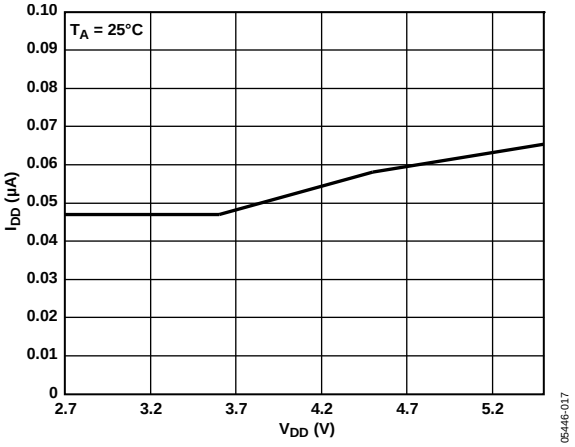

Figure 22. Supply Current vs. Supply Voltage

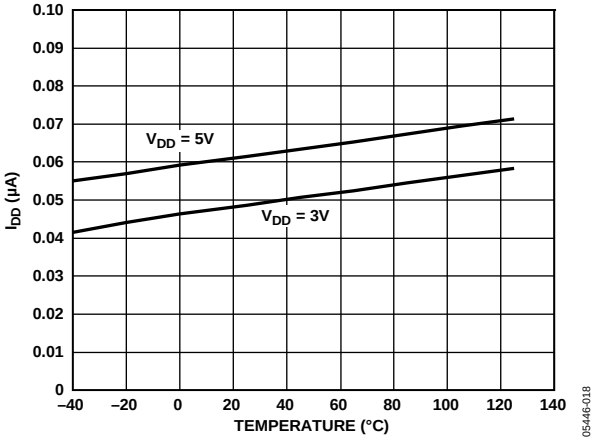

Figure 23. Supply Current vs. Temperature (3 V/5 V Supply)

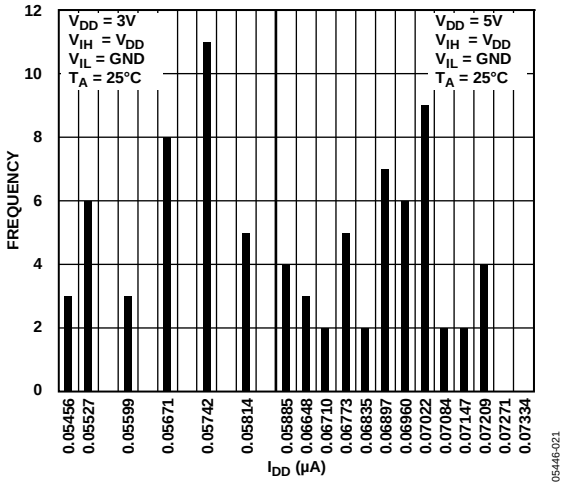

Figure 26. I_{DD} Histogram (3 V/5 V Supply)

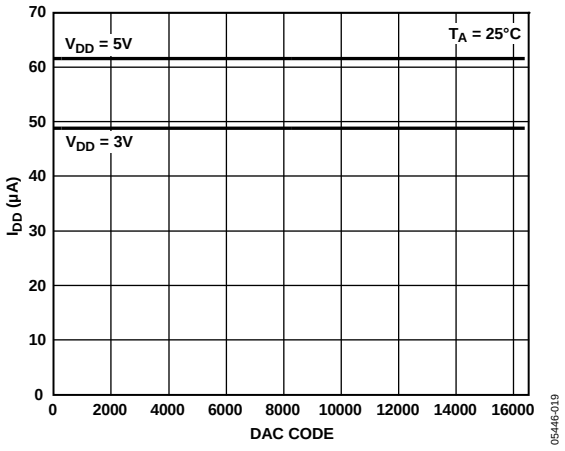

Figure 24. Supply Current vs. Digital Input Code

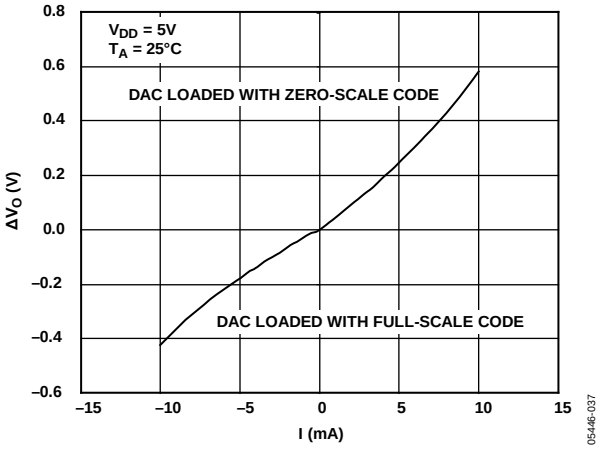

Figure 27. Sink and Source Capability

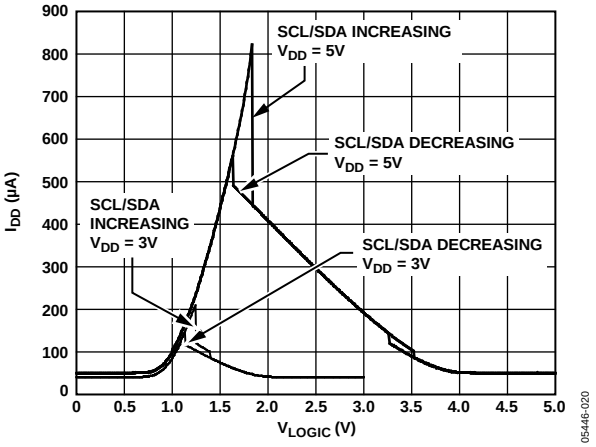

Figure 25. Supply Current vs. SCL/SDA Logic Voltage

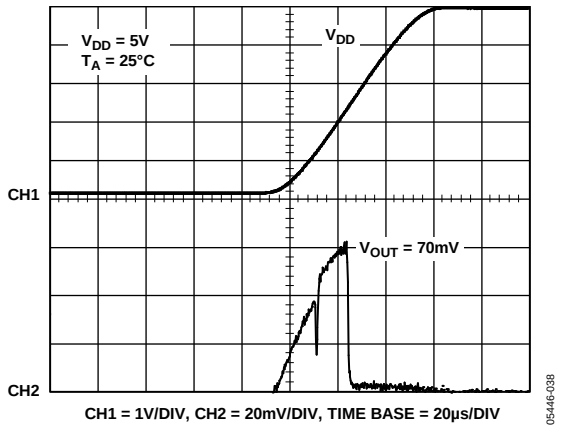

Figure 28. Power On Reset to 0 V

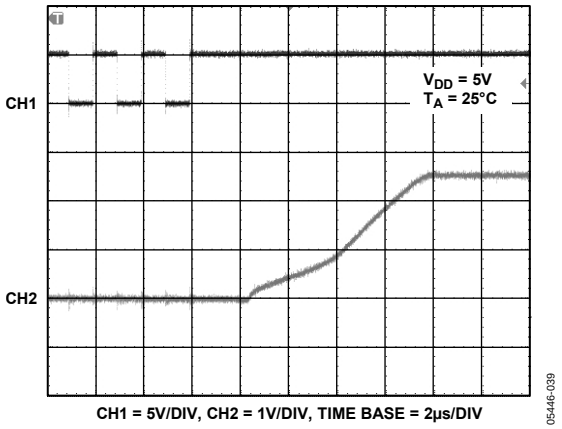

Figure 29. Exiting Power-Down Mode

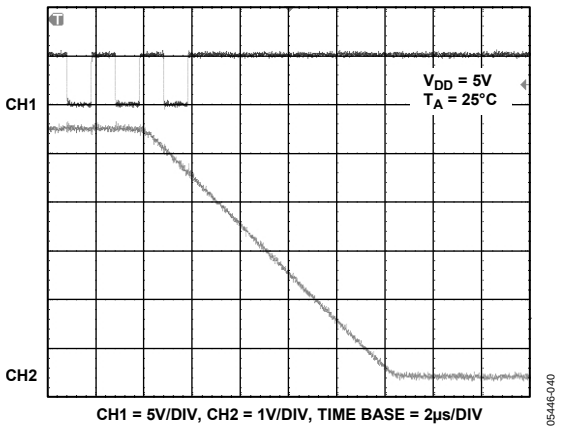

Figure 30. Full-Scale Settling Time

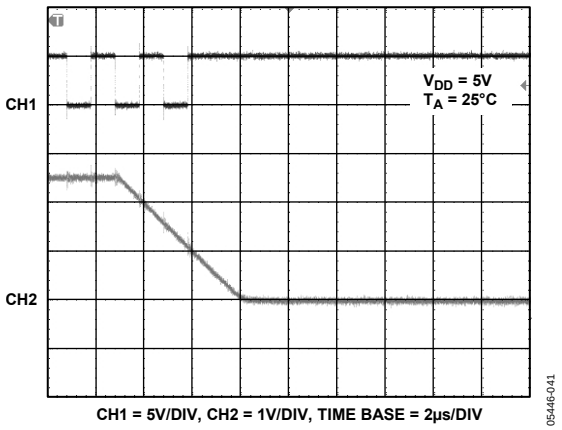

Figure 31. Half Scale Settling Time

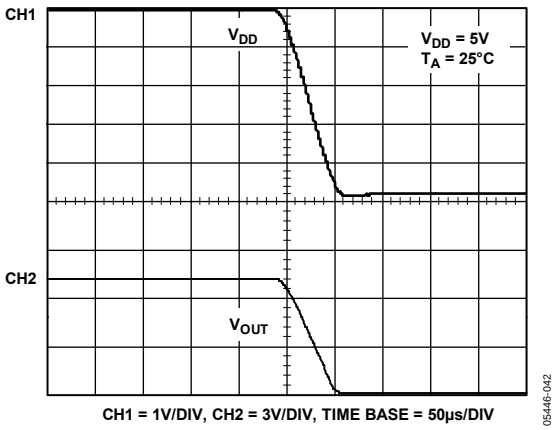

Figure 32. V_{OUT} vs. V_{DD}

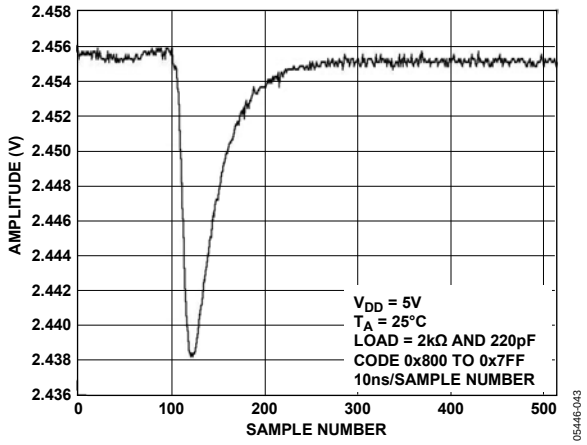

Figure 33. DAC Glitch Impulse

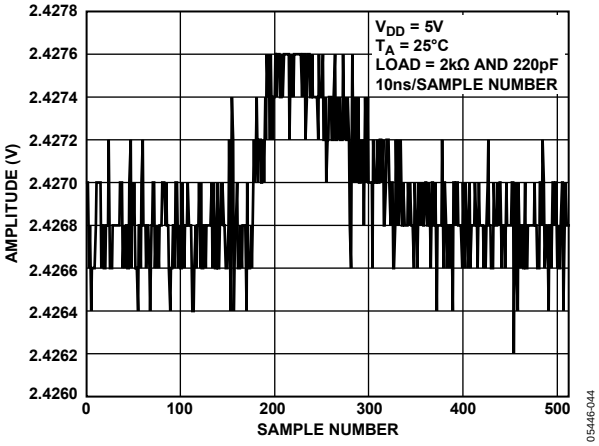

Figure 34. Digital Feedthrough

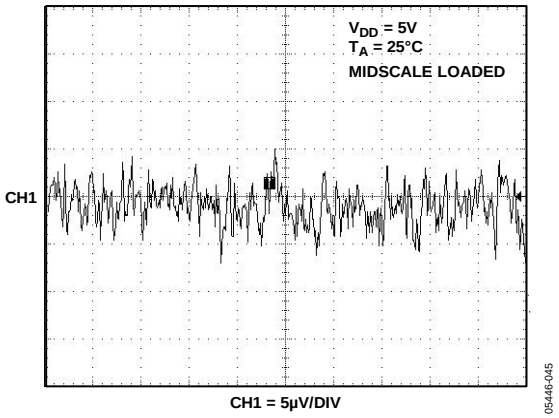

Figure 35. 1/f Noise, 0.1 Hz to 10 Hz Bandwidth

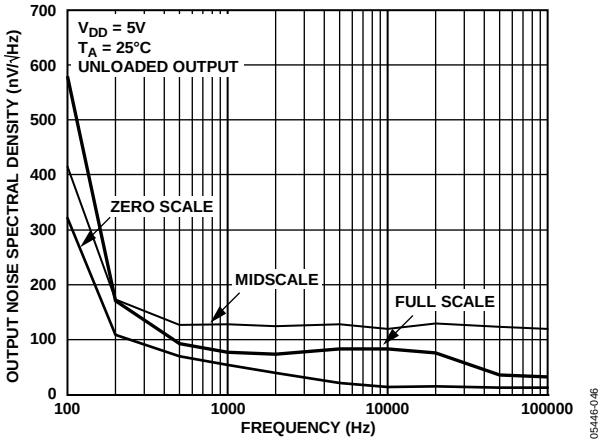

Figure 36. Output Noise Spectral Density

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in least significant bits (LSB), from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 5.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 6.

Zero Code Error
Zero code error is due to a combination of the offset errors in the DAC and output amplifier; it is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive in the AD5602/AD5612/AD5622 because the output of the DAC cannot go below 0 V. Zero code error is expressed in mV. A plot of zero code error vs. temperature can be seen in Figure 18.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register; it is expressed in percent of full-scale range. Ideally, the output is V_{DD} − 1 LSB. A plot of full-scale error vs. temperature can be seen in Figure 18.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 11.

Zero Code Error Drift
Zero code error drift is a measure of the change in zero code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 33).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s, and vice versa (see Figure 34).

THEORY OF OPERATION

D/A SECTION

The AD5602/AD5612/AD5622 DACs are fabricated on a CMOS process. The architecture consists of a string DACs followed by an output buffer amplifier. Figure 37 shows a block diagram of the DAC architecture.

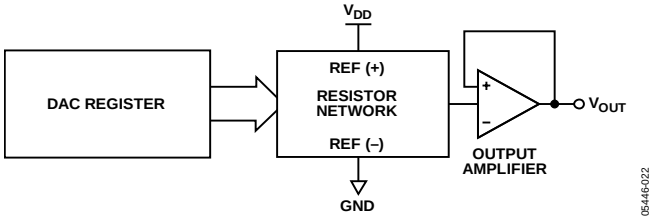

Figure 37. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{DD} \times \left(\frac{D}{2^n} \right)$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 255 (AD5602), 0 to 1023 (AD5612), or 0 to 4095 (AD5622).
n is the bit resolution of the DAC.

RESISTOR STRING

The resistor string structure is shown in Figure 38. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

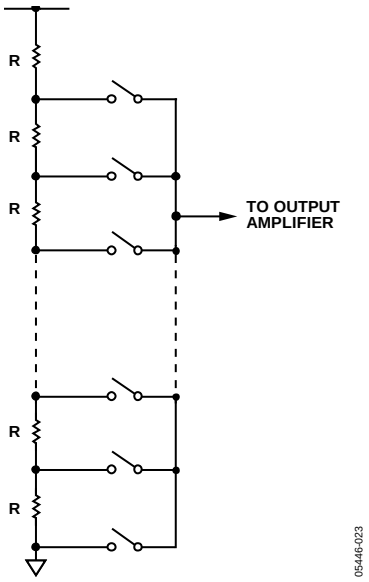

Figure 38. Resistor String Structure

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 27. The slew rate is 0.5 V/μs with a half scale settling time of 5 μs with the output unloaded.

SERIAL INTERFACE

The AD5602/AD5612/AD5622 have 2-wire I²C compatible serial interfaces (refer to *I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). The AD5602/AD5612/AD5622 can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 2 for a timing diagram of a typical write sequence.

The AD5602/AD5612/AD5622 support standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The AD5602/AD5612/AD5622 each have a 7-bit slave address. The five most significant bits (MSB) are 00011 and the two LSBs are determined by the state of the ADDR pin. The facility to make hardwired changes to ADDR allows the user to incorporate up to three of these devices on one bus as outlined in Table 7.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. If a stop condition is generated between the 7th and 8th clock pulse of the I²C address frame, a power cycle is required to recover the device. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

Table 7. Device Address Selection

ADDR	A1	A0
GND	1	1
V_{DD}	0	0
NC (No Connection)	1	0

INPUT REGISTER

The input register is 16 bits wide. Figure 39, Figure 40, and Figure 41 illustrate the contents of the input register for each device. Data is loaded into the device as a 16-bit word under the control of an SCL input. The timing diagram for this operation is shown in Figure 2. The 16-bit word consists of four control bits followed by 8, 10, or 12 bits of data, depending on the device type. MSB (DB15) is loaded first. The first two bits are reserved bits that must be set to zero; the next two bits are control bits that select the mode of operation of the device (normal mode or any one of three power-down modes). See the Power-Down Modes section for a complete description. The remaining bits are left justified DAC data bits, starting with the MSB and ending with the LSB.

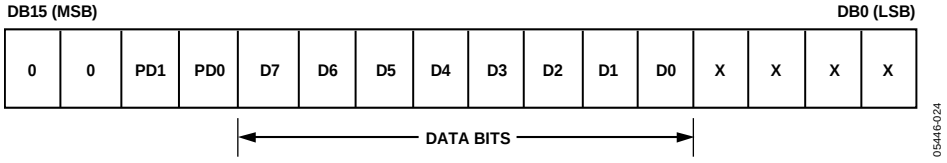

Figure 39. AD5602 Input Register Contents

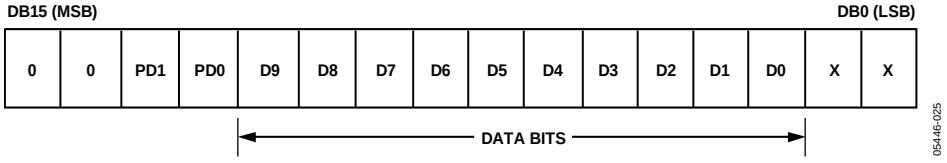

Figure 40. AD5612 Input Register Contents

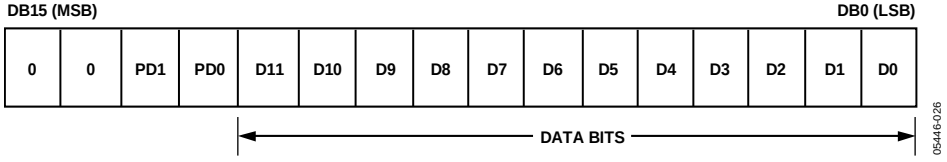

Figure 41. AD5622 Input Register Contents

POWER-ON RESET

The AD5602/AD5612/AD5622 each contain a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is 0 V where it remains until a valid write sequence is made to the DAC. This is useful in applications in which it is important to know the state of the DAC output while it is in the process of powering up.

POWER-DOWN MODES

The AD5602/AD5612/AD5622 each contain four separate modes of operation. These modes are software programmable by setting Bit PD1 and Bit PD0 in the control register. Table 8 shows how the state of the bits corresponds to the mode of operation of the device.

Table 8. Modes of Operation

PD1	PD0	Operating Mode
0	0	Normal operation
0	1	Power-down (1 kΩ load to GND)
1	0	Power-down (100 kΩ load to GND)
1	1	Power-down (Three-state output)

When both bits are set to 0, the device works normally with its usual power consumption of 100 μA maximum at 5 V. However, for the three power-down modes, the supply current falls to <150 nA (at 3 V). Not only does the supply current fall, but the output stage is internally switched from the output of the amplifier to a resistor network of known values. This gives the advantage of knowing the output impedance of the device while the device is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open circuited (three-state). Figure 42 shows the output stage.

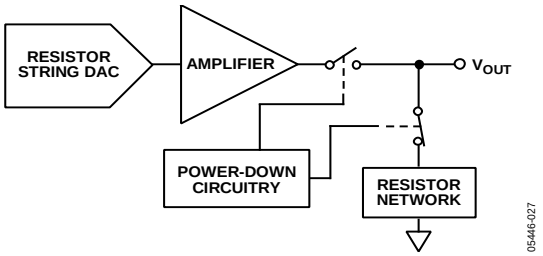

Figure 42. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 14 μs for V_{DD} = 5 V and 17 μs for V_{DD} = 3 V (see Figure 29).

WRITE OPERATION

When writing to the AD5602/AD5612/AD5622, the user must begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the DAC, the most significant byte followed by the least significant byte as shown in Figure 40; both of these data bytes are acknowledged by the AD5602/AD5612/AD5622. A stop condition follows. The write operations for the three DACs are shown in Figure 43, Figure 44, and Figure 45.

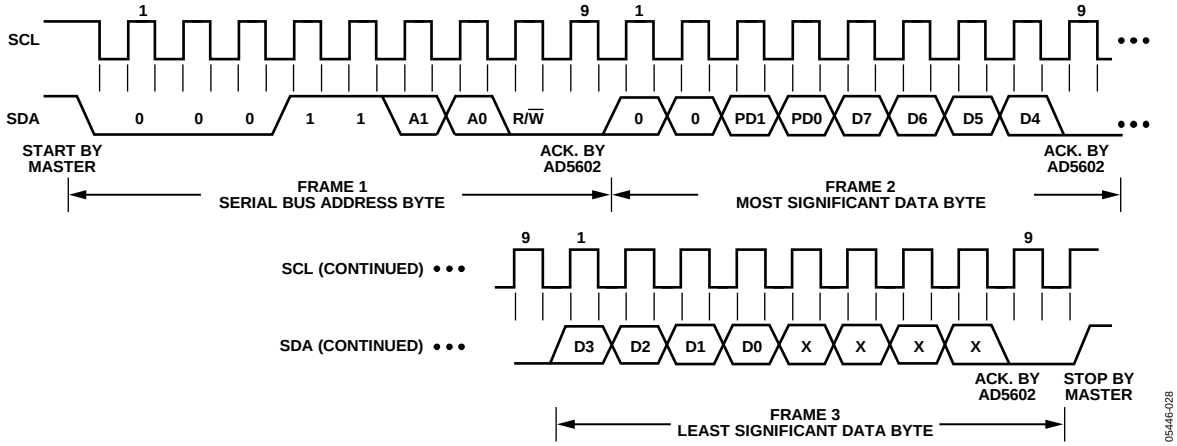

Figure 43. AD5602 Write Sequence

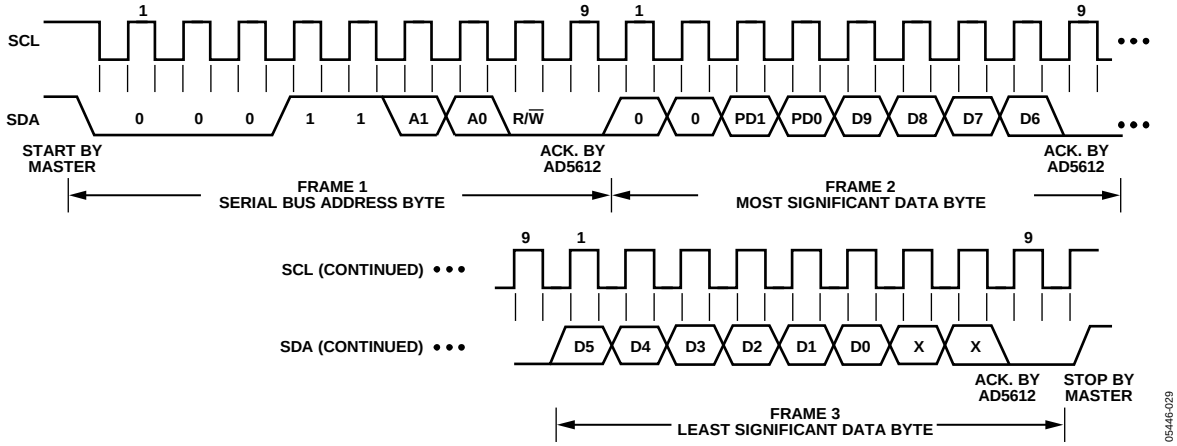

Figure 44. AD5612 Write Sequence

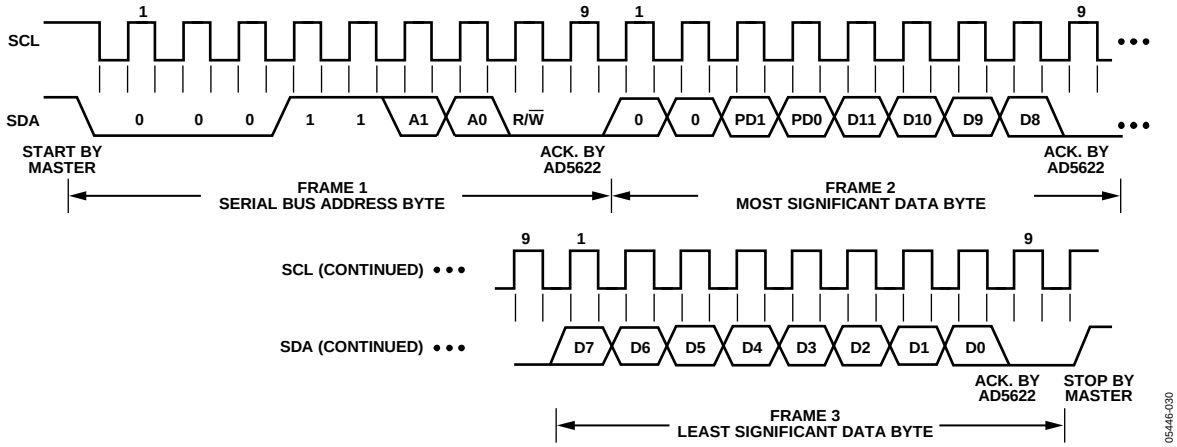

Figure 45. AD5622 Write Sequence

READ OPERATION

When reading data back from the AD5602/AD5612/AD5622, the user begins with a start command followed by an address byte (R/$\overline{W}$ = 1), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low.

The DAC then shifts out two bytes of data, both acknowledged by the master as shown in Figure 46, Figure 47, and Figure 48. A stop condition follows. When a read operation is performed, the DAC shifts out the last transferred command. If a second readback operation is executed, the device shifts out 0x00

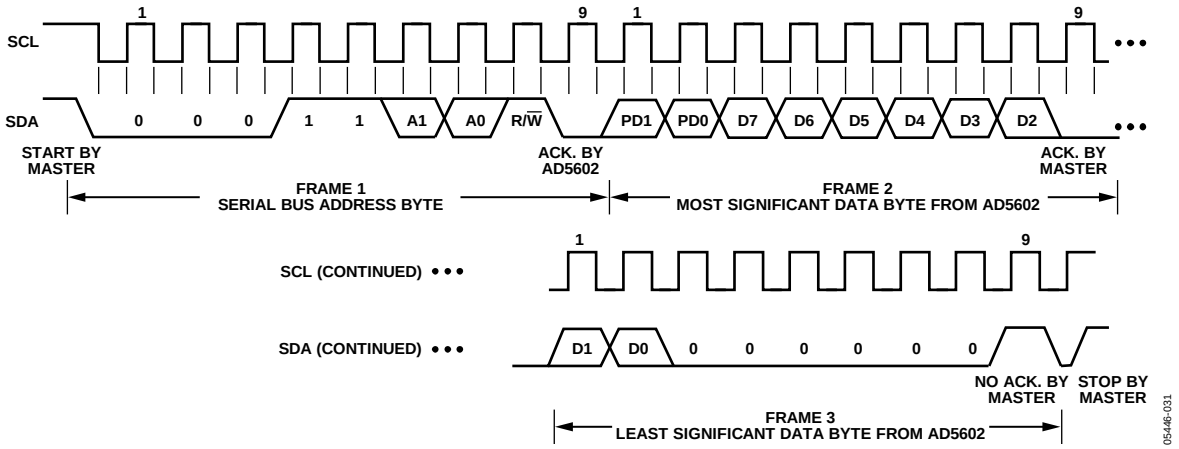

Figure 46. AD5602 Read Sequence

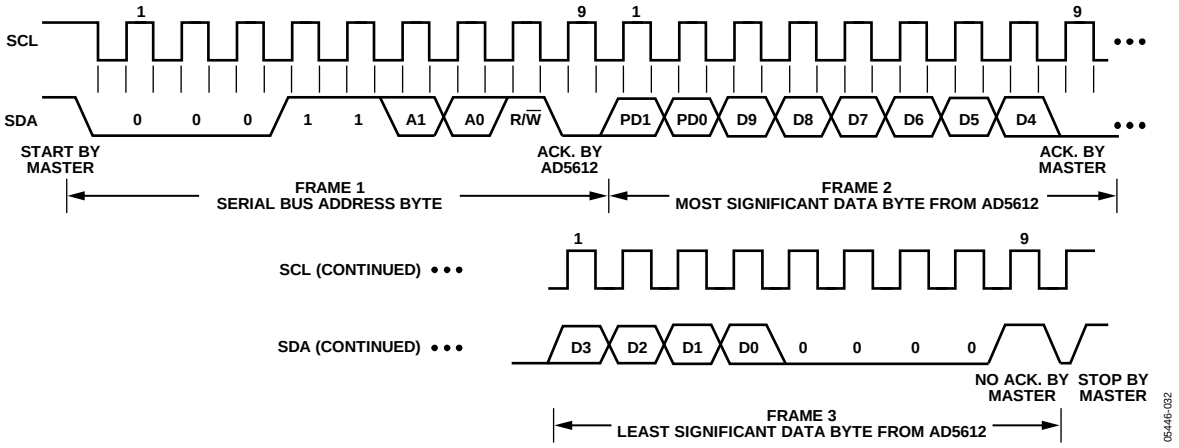

Figure 47. AD5612 Read Sequence

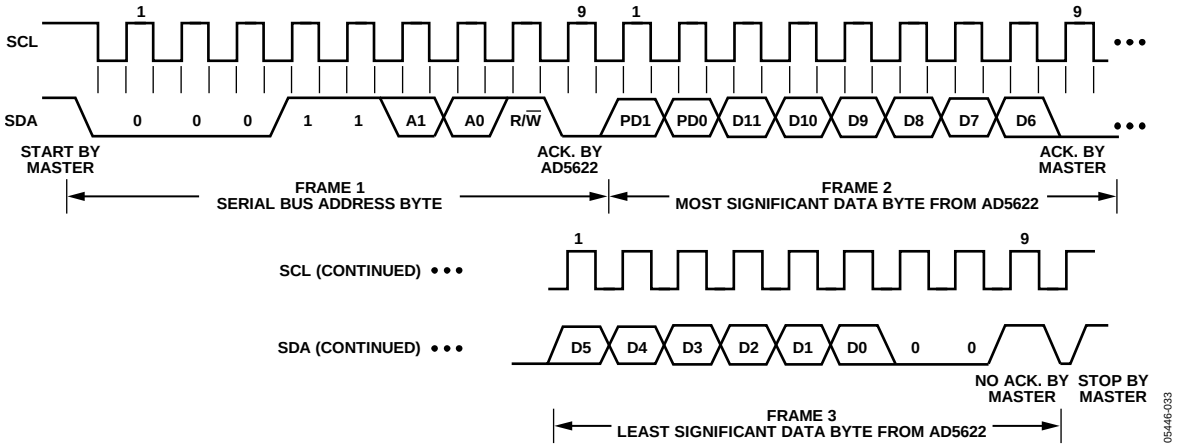

Figure 48. AD5622 Read Sequence

HIGH SPEED MODE

High speed mode communication commences after the master addresses all devices connected to the bus with the Master Code 00001XXX to indicate that a high speed mode transfer is to begin. No device connected to the bus is permitted to acknowledge the high speed master code, therefore, the code is followed by a no acknowledge.

The master must then issue a repeated start followed by the device address. The selected device then acknowledges the address. All devices continue to operate in high speed mode until the master issues a stop condition. When the stop condition is issued, the devices return to standard/fast mode.

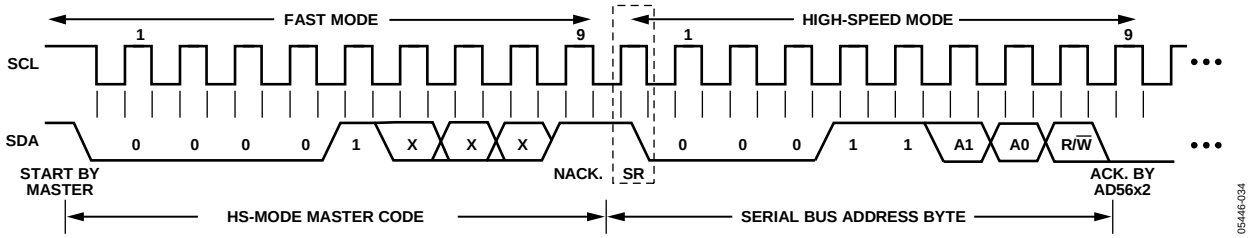

Figure 49. Placing the AD5602/AD5612/AD5622 into High Speed Mode

APPLICATIONS INFORMATION

CHOOSING A REFERENCE AS POWER SUPPLY

The AD5602/AD5612/AD5622 come in tiny LFCSP and SC70 packages with less than 100 µA supply current, thereby making the choice of reference dependent upon the application requirement. For space-saving applications, the ADR425 is available in an SC70 package with excellent drift at 3ppm/°C. It also provides very good noise performance at 3.4 µV p-p in the 0.1 Hz to 10 Hz range.

Because the supply current required by the AD5602/AD5612/AD5622 DACs is extremely low, they are ideal for low supply applications. The ADR293 voltage reference is recommended in this case. This requires 15 µA of quiescent current and can therefore drive multiple DACs in the one system, if required.

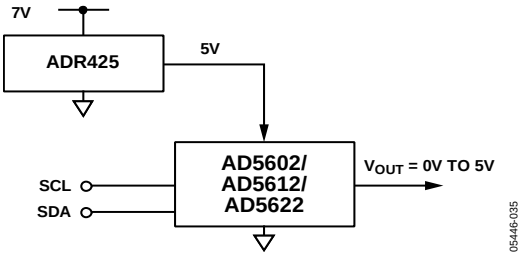

Figure 50. ADR425 as Power Supply

Examples of some recommended precision references for use as supplies to the AD5602/AD5612/AD5622 are shown in Table 9.

Table 9. Recommended Precision References

Device No.	Initial Accuracy (mV max)	Temperature Drift (ppm/°C max)	0.1 Hz to 10 Hz Noise (µV p-p typ)
ADR435	±6	3	3.4
ADR425	±6	3	3.4
ADR02	±5	3	15
ADR395	±6	25	5

BIPOLAR OPERATION

The AD5602/AD5612/AD5622 are designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 51. The circuit in Figure 51 gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as

$$V_O = \left[V_{DD} \times \left(\frac{D}{2^n} \right) \times \left(\frac{R1+R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where:
D represents the input code in decimal.
n represents the bit resolution of the DAC.

With V_{DD} = 5 V, R1 = R2 = 10 kΩ.

$$V_O = \left(\frac{10 \times D}{2^n} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V with 0x000 corresponding to a −5 V output, and 0xFFF corresponding to a +5 V output.

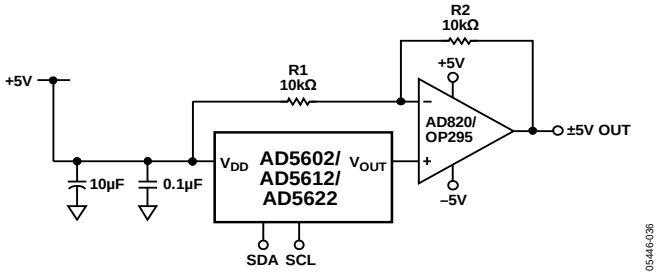

Figure 51. Bipolar Operation with the AD5602/AD5612/AD5622

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5602/AD5612/AD5622 has separate analog and digital sections, each having its own area of the board. If theAD5602, AD5612, or AD5622 is in a system in which other devices require an AGND to DGND connection, the connection is made at one point only. This ground point must be as close as possible to the AD5602/AD5612/AD5622.

The power supply to the AD5602/AD5612/AD5622 is bypassed with 10 µF and 0.1 µF capacitors. The capacitors must be physically as close as possible to the device with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), such as common ceramic types. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line has as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals must be shielded from other devices of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, the microstrip technique is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

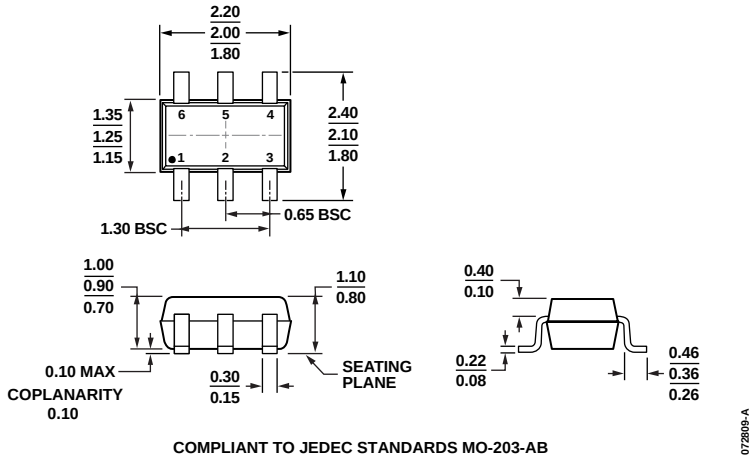

Figure 52. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

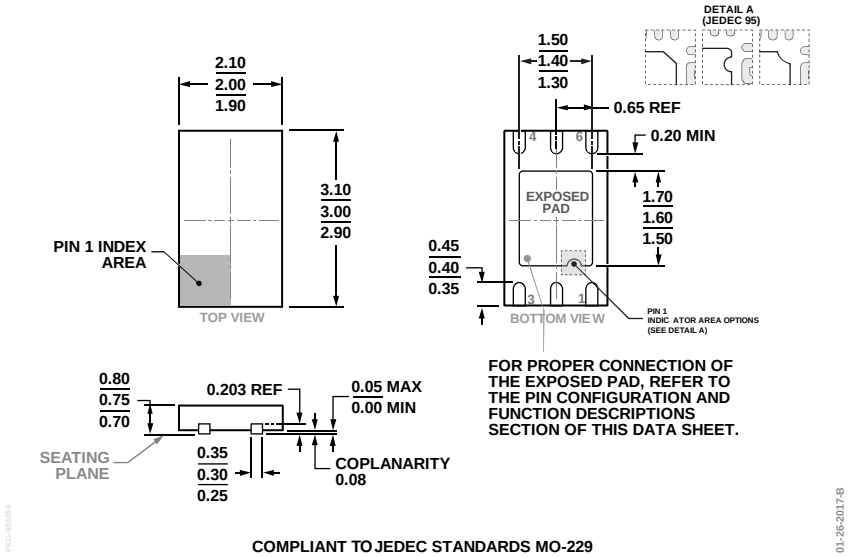

Figure 53. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2.00 mm × 3.00 mm Body and 0.75 mm Package Height
(CP-6-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	INL (max)	I²C Interface Modes Supported	Temperature Range	Power Supply Range	Package Description	Package Option	Marking Code
AD5602YKSZ-1500RL7	±0.5 LSB	Standard, fast and high speed	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5W
AD5602YKSZ-1REEL7	±0.5 LSB	Standard, fast and high speed	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5W
AD5602BKSZ-2500RL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5X
AD5602BKSZ-2REEL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5X
AD5602YKSZ-2500RL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5Y
AD5602YKSZ-2REEL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5Y
AD5612YKSZ-1500RL7	±0.5 LSB	Standard, fast, and high speed	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5T
AD5612BKSZ-2500RL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5U
AD5612AKSZ-2500RL7	±4 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D60
AD5612AKSZ-2REEL7	±4 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D60
AD5612ACPZ-2-RL7	±4 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead LFCSP	CP-6-5	D2
AD5612YKSZ-2500RL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5S
AD5612YKSZ-2REEL7	±0.5 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5S
AD5622YKSZ-1500RL7	±2 LSB	Standard, fast, and high speed	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5M
AD5622YKSZ-1REEL7	±2 LSB	Standard, fast, and high speed	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5M
AD5622BKSZ-2500RL7	±2 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5N
AD5622BKSZ-2REEL7	±2 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5N
AD5622YKSZ-2500RL7	±2 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5P
AD5622YKSZ-2REEL7	±2 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5P
AD5622WKSZ-1500RL7	±6 LSB	Standard, fast, and high speed	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5Q
AD5622AKSZ-2500RL7	±6 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5R
AD5622AKSZ-2REEL7	±6 LSB	Standard, fast	−40°C to +125°C	2.7 V to 5.5 V	6-Lead SC70	KS-6	D5R

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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