



**THE DATASHEET OF  
CY8C4247FNI-BL493T**



# PSoC™ 4 MCU with AIROC™ Bluetooth® LE

## Based on Arm® Cortex®-M0

### General description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE product family, based on this platform, is a combination of a microcontroller with an integrated Bluetooth® Low Energy, also known as Bluetooth® smart, radio and subsystem (BLESS). The other features include digital programmable logic, high-performance analog-to-digital conversion (ADC), opamps with Comparator mode, and standard communication and timing peripherals. The programmable analog and digital subsystems allow flexibility and in-field tuning of the design.

### Features

- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0 CPU with single-cycle multiply and DMA
  - Up to 256 KB of flash with read accelerator
  - Up to 32 KB of SRAM
- Bluetooth® LE radio and subsystem
  - Bluetooth® LE 4.2 support
  - 2.4-GHz RF transceiver with 50-Ω antenna drive
  - Digital PHY
  - Link-layer engine supporting master and slave modes
  - RF output power: -18 dBm to +3 dBm
  - RX sensitivity: -89 dBm
  - RX current: 18.7 mA
  - TX current: 15.6 mA at 0 dBm
  - Received Signal Strength Indication (RSSI): 1-dB resolution
- Programmable analog
  - Four opamps with reconfigurable high-drive external and high-bandwidth internal drive, Comparator modes, and ADC input buffering capability. Can operate in Deep Sleep mode.
  - 12-bit, 1-Msps SAR ADC with differential and single-ended modes; Channel Sequencer with signal averaging
  - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in Deep Sleep mode
- Programmable digital
  - Four programmable logic blocks called universal digital blocks, (UDBs), each with eight macrocells and data path
  - Infineon-provided peripheral component library, user-defined state machines, and Verilog input
- Power management
  - Active mode: 1.7 mA at 3-MHz flash program execution
  - Deep Sleep mode: 1.5 μA with watch crystal oscillator (WCO) on
  - Hibernate mode: 150 nA with RAM retention
  - Stop mode: 60 nA
- Capacitive sensing
  - Capacitive sigma-delta (CSD) provides best-in-class SNR (>5:1) and liquid tolerance
  - Infineon-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning algorithm (SmartSense)

## Features

- Segment LCD drive
  - LCD drive supported on all pins (common or segment)
  - Operates in Deep Sleep mode with four bits per pin memory
- Serial communication
  - Two independent run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I<sup>2</sup>C, SPI, or UART functionality
- Timing and pulse-width modulation
  - Four 16-bit timer/counter pulse-width modulator (TCPWM) blocks
  - Center-aligned, Edge, and Pseudo-random modes
  - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications
- Up to 36 programmable GPIOs
  - 7 mm × 7 mm 56-pin QFN package
  - 76-ball CSP package
  - 68-ball CSP package
  - Any GPIO pin can be CAPSENSE™, LCD, analog, or digital
  - Two overvoltage-tolerant (OVT) pins; drive modes, strengths, and slew rates are programmable
- PSoC™ Creator design environment
  - Integrated Design Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
  - API components for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
  - After schematic entry, development can be done with Arm®-based industry-standard development tools

More information

## More information

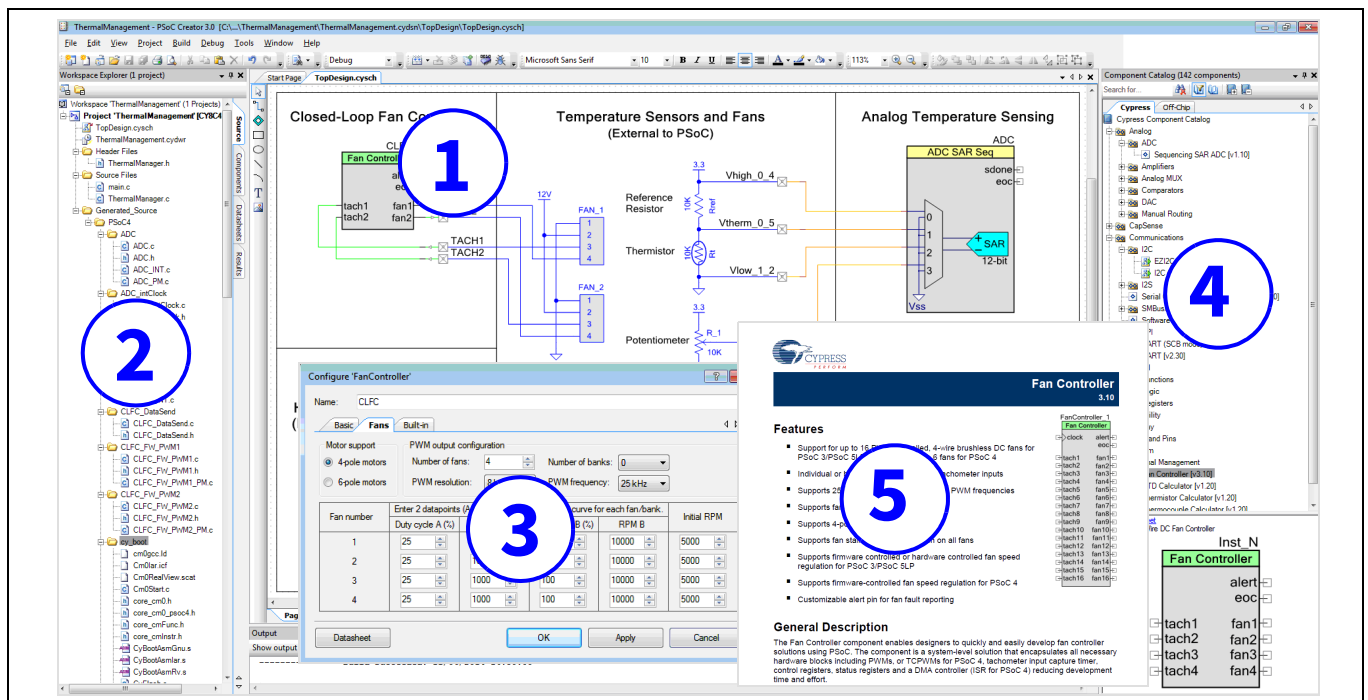
There is a wealth of data at [www.infineon.com](http://www.infineon.com) to help you to select the right PSoC™ device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for [Bluetooth® Low Energy products](#). Following is an abbreviated list for PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE:

- Overview: [PSoC™ portfolio](#)
- Product selectors: [PSoC™ 1](#), [PSoC™ 3](#), [PSoC™ 4](#), [PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE](#), [PSoC™ 5LP](#). In addition, PSoC™ Creator includes a device selection tool.
- Application notes: There are a large number of PSoC™ application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE are:
  - [AN91267](#): Getting started with PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE
  - [AN97060](#): PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE and PRoC-BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) guide
  - [AN91184](#): PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE - Designing Bluetooth® LE applications
  - [AN91162](#): Creating a Bluetooth® LE Custom Profile
  - [AN91445](#): Antenna design and RF layout guidelines
  - [AN96841](#): Getting started With EZ-BLE module
  - [AN85951](#): PSoC™ 4 CAPSENSE™ design guide
  - [AN95089](#): PSoC™ 4/PRoC-Bluetooth® LE crystal oscillator selection and tuning techniques
  - [AN92584](#): Designing for low power and estimating battery life for Bluetooth® LE applications
- Technical reference manual (TRM) is in two documents:
  - [Architecture TRM](#) details each PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE functional block.
  - [Registers TRM](#) describes each of the PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE registers.
- Development kits:
  - [CY8CKIT-042-BLE-A](#) Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth® LE development kit for PSoC™ 4 with AIROC™ Bluetooth® LE.
  - [CY8CKIT-142](#), PSoC™ 4 with AIROC™ Bluetooth® LE Module, features a PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE device, two crystals for the antenna matching network, a PCB antenna, and other passives, while providing access to all GPIOs of the device.
  - [CY8CKIT-143](#), PSoC™ 4 with AIROC™ Bluetooth® LE 256 KB module, features a PSoC™ 4 CY8C4xxx-BL MCU with AIROC™ Bluetooth® LE 256 KB device, two crystals for the antenna matching network, a PCB antenna, and other passives, while providing access to all GPIOs of the device.
  - The [MiniProg3](#) device provides an interface for flash programming and debug.

## PSoC™ Creator

**PSoC™ Creator** is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, and PSoC™ 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC™ Components; see the [list of component datasheets](#). With PSoC™ Creator, you can

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC™ hardware, using the PSoC™ Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets



**Figure 1 Multiple-sensor example project in PSoC™ Creator contents**

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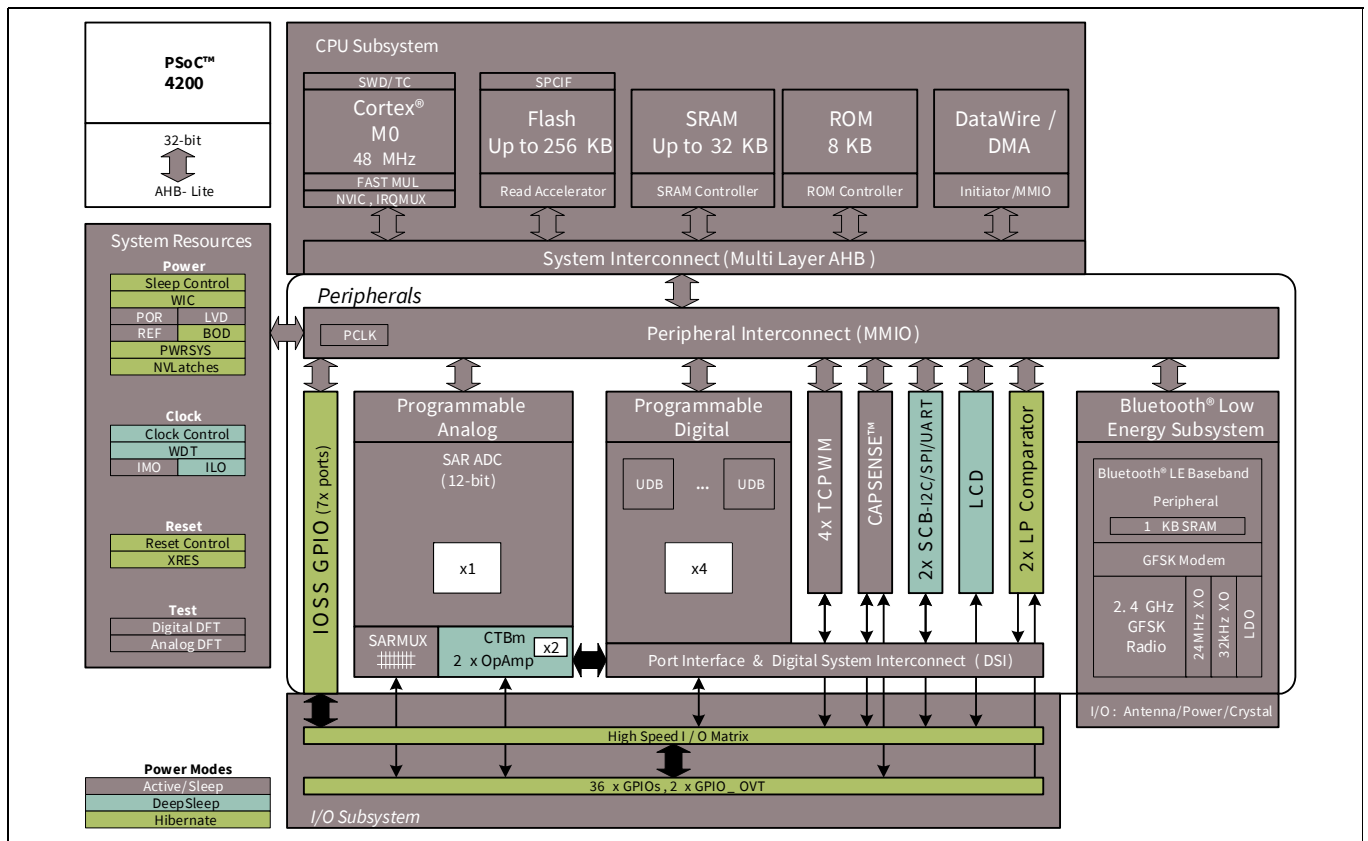
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Block diagram

## Block diagram



The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® SWD interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debugging.

The PSoC™ Creator IDE provides fully integrated programming and debugging support for the PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE devices. The SWD interface is fully compatible with industry-standard third-party tools. With the ability to disable debug features, very robust flash protection, and allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

Debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with the new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE allows the customer to make.

## **1 Functional definition**

### **1.1 CPU and memory subsystem**

#### **1.1.1 CPU**

The Cortex®-M0 CPU in PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher-performance processors such as Cortex®-M3 and M4. The implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to the main processor to be switched off when the chip is in the Deep Sleep mode. The Cortex®-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes an SWD interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE has four break-point (address) comparators and two watchpoint (data) comparators.

#### **1.1.2 Flash**

The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE device has a flash module with 256 KB of flash memory, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required. Maximum erase and program time is 20 ms per row (256 bytes). This also applies to the emulated EEPROM.

#### **1.1.3 SRAM**

SRAM memory is retained during Hibernate.

#### **1.1.4 SRAM**

The 8-KB supervisory ROM contains a library of executable functions for flash programming. These functions are accessed through supervisory calls (SVC) and enable in-system programming of the flash memory.

#### **1.1.5 DMA**

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

### **1.2 System Resources**

#### **1.2.1 Power System**

The power system is described in detail in the section **“Power”** on page 27. It provides an assurance that the voltage levels are as required for the respective modes, and can either delay the mode entry (on power-on reset (POR), for example) until voltage levels are as required or generate resets (brownout detect (BOD)) or interrupts when the power supply reaches a particular programmable level between 1.8 and 4.5 V (low voltage detect (LVD)). PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE operates with a single external supply (1.71 to 5.5 V without radio, and 1.9 V to 5.5 V with radio). The device has five different power modes; transitions between these modes are managed by the power system. PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes. Refer to the *Technical Reference Manual* for more details.

### **1.2.2 Clock system**

The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE consists of the internal main oscillator (IMO), the internal low-speed oscillator (ILO), the 24-MHz external crystal oscillator (ECO) and the 32-kHz watch crystal oscillator (WCO). In addition, an external clock may be supplied from a pin.

### **1.2.3 IMO clock source**

The IMO is the primary source of internal clocking in PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. The IMO tolerance with Infineon-provided calibration settings is  $\pm 2\%$ .

### **1.2.4 ILO clock source**

The ILO is a very low-power oscillator, which is primarily used to generate clocks for the peripheral operation in the Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. A software component is provided, which does the calibration.

### **1.2.5 External crystal oscillator (ECO)**

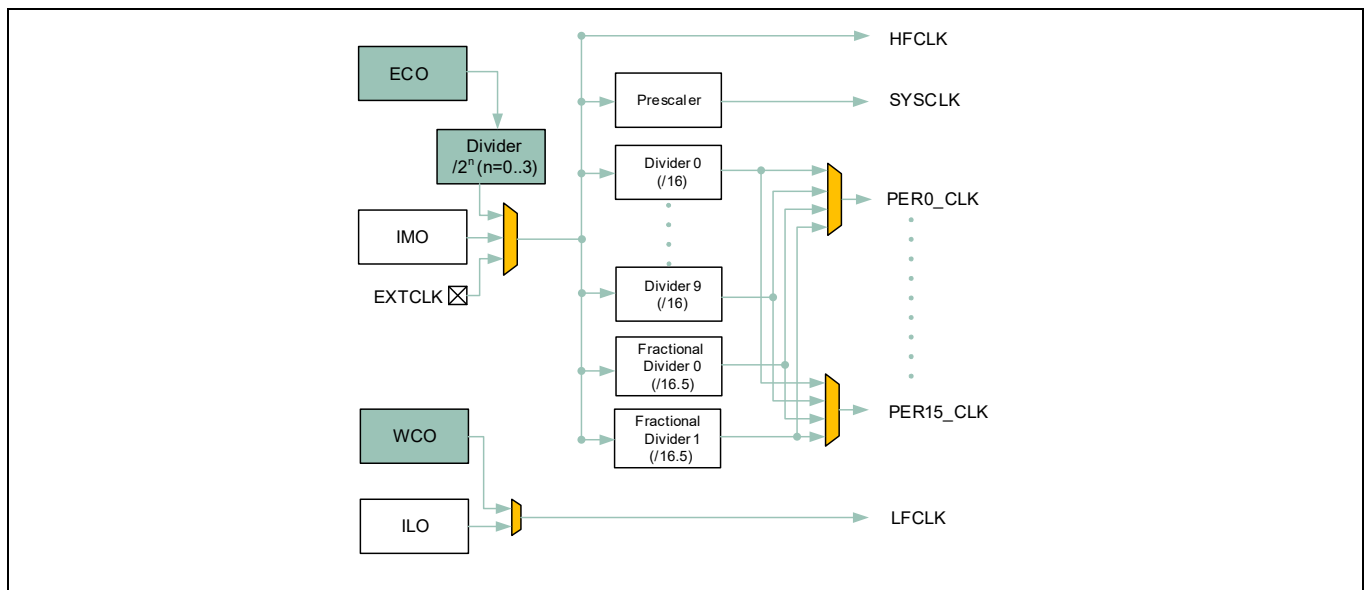
The ECO is used as the active clock for the Bluetooth® LE subsystem to meet the  $\pm 50$ -ppm clock accuracy of the Bluetooth® 4.2 Specification. PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE includes a tunable load capacitor to tune the crystal clock frequency by measuring the actual clock frequency. The high-accuracy ECO clock can also be used as a system clock.

### **1.2.6 Watch crystal oscillator (WCO)**

The WCO is used as the sleep clock for the Bluetooth® LE subsystem to meet the  $\pm 500$ -ppm clock accuracy for the Bluetooth® 4.2 Specification. The sleep clock provides an accurate sleep timing and enables wakeup at the specified advertisement and connection intervals. The WCO output can be used to realize the real-time clock (RTC) function in firmware.

### **1.2.7 Watchdog timer**

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows the watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register. With the WCO and firmware, an accurate real-time clock (within the bounds of the 32-kHz crystal accuracy) can be realized.



**Figure 2 PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE MCU clocking architecture**

The HFCLK signal can be divided down (see [Figure 2](#)) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC™ Creator.

### 1.2.8 Reset

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

### 1.2.9 Voltage Reference

The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a REF pin or use an external reference for the SAR. See [Table 21](#) for details.

### **1.3 Bluetooth® LE radio and subsystem**

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE incorporates a Bluetooth® Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth® Smart Bluetooth® Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth® smart radio and subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band, and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE secure connections (Bluetooth® 4.2 feature)
- Link layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE ping
  - LE data packet length extension (Bluetooth® 4.2 feature)
  - Link layer privacy (with extended scanning filter policy, Bluetooth® 4.2 feature)
- Supports all SIG-adopted Bluetooth® LE profiles

## 1.4 Analog blocks

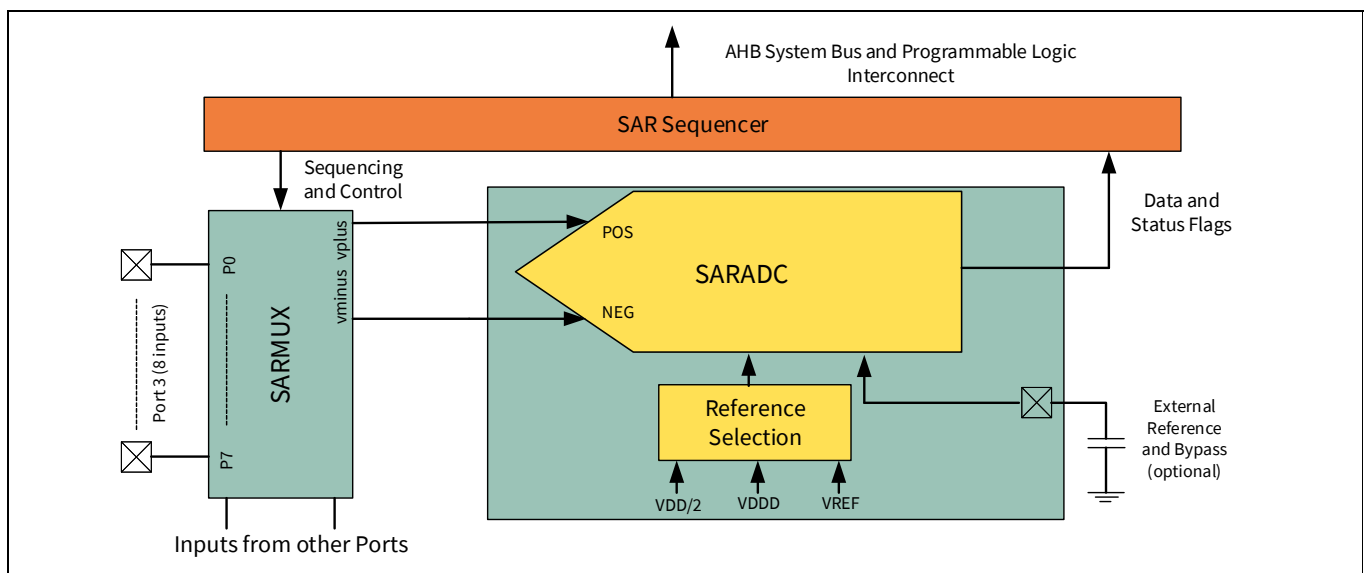
### 1.4.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm 1\%$ ) and by providing the choice of three internal voltage references,  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{REF}$  (nominally 1.024 V), as well as an external reference through a REF pin. The sample-and-hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Mpsps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.



**Figure 3 SAR ADC system diagram**

### 1.4.2 Opamps (CTBm block)

PSoC™ CY8C42x8\_BLE has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip, eliminating external components. PGAs, voltage buffers, filters, transimpedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

### 1.4.3 Temperature sensor

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using an Infineon-supplied software that includes calibration and linearization.

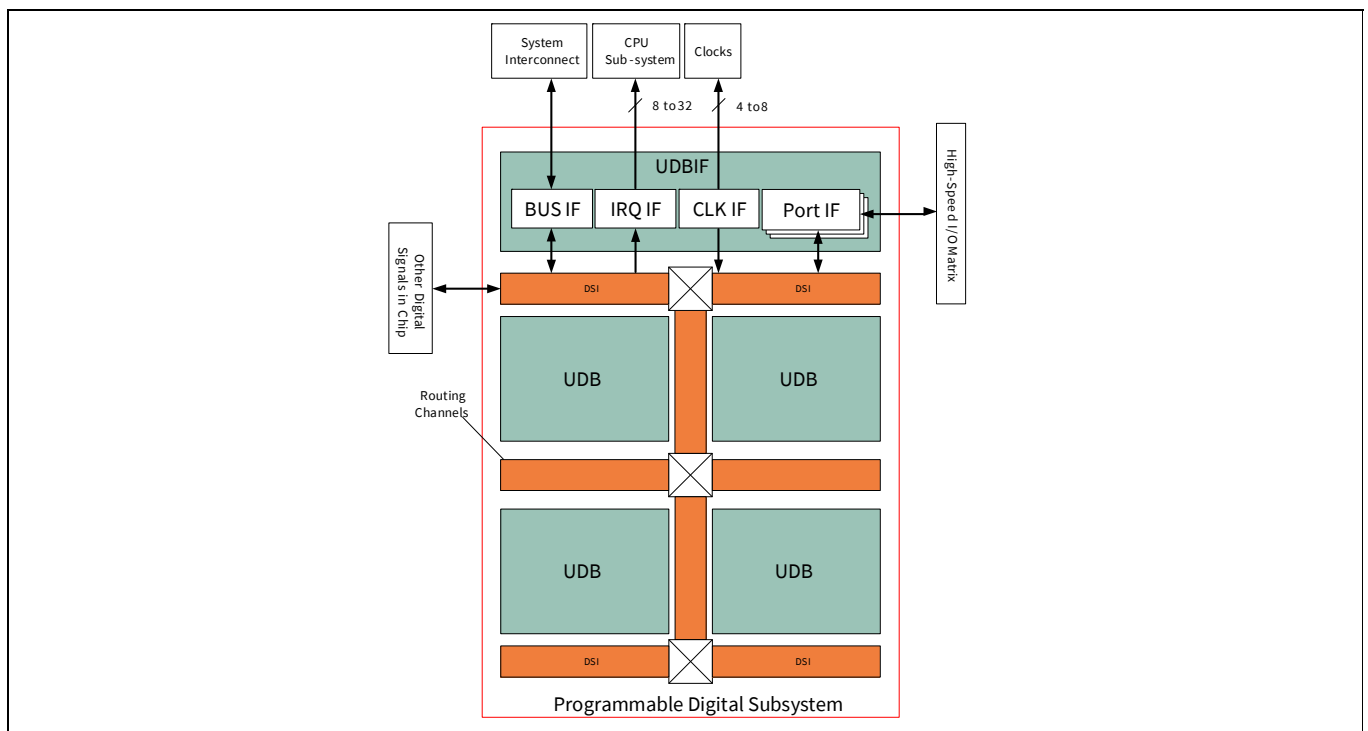
### 1.4.4 Low-power comparators

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

## 1.5 Programmable digital

### 1.5.1 Universal digital blocks (UDBs) and port interfaces

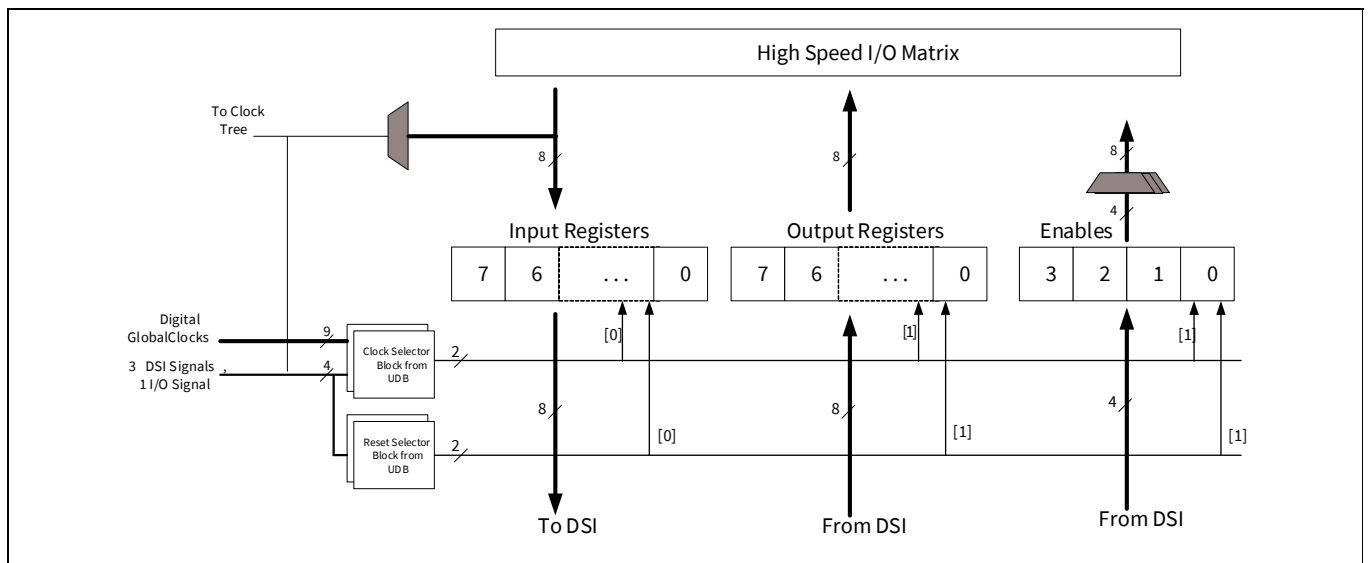
The PSoC™ 4XX8 BLE 4.2 has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.



**Figure 4** UDB array

UDBs can be clocked from a clock-divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows a faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs (see [Figure 5](#)).



**Figure 5** Port interface

UDBs can generate interrupts (one UDB at a time) to the interrupt controller. UDBs retain the ability to connect to any pin on the chip through the DSI.

## 1.6 Fixed-function digital

### 1.6.1 Timer/counter/PWM block

The timer/counter/PWM block consists of four 16-bit counters with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

### 1.6.2 Serial Communication Blocks (SCB)

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE has two SCBs, each of which can implement an I<sup>2</sup>C, UART, or SPI interface.

**I<sup>2</sup>C mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI<sup>2</sup>C that creates a mailbox address range in the memory of PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE and effectively reduces the I<sup>2</sup>C communication to reading from and writing to an array in the memory. In addition, the block supports an 8-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I<sup>2</sup>C peripheral is compatible with I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

SCB1 is fully compliant with Standard mode (100 kHz), Fast mode (400 kHz), and Fast-Mode Plus (1 MHz) I<sup>2</sup>C signaling specifications when routed to GPIO pins P5[0] and P5[1], except for hot-swap capability during I<sup>2</sup>C active communication. The remaining GPIOs do not meet the hot-swap specification ( $V_{DD}$  off; draw < 10- $\mu$ A current) for Fast mode and Fast-Mode Plus,  $I_{OL}$  Spec (20 mA) for Fast-Mode Plus, hysteresis spec (0.05  $V_{DD}$ ) for Fast mode and Fast-Mode Plus, and minimum fall time spec for Fast mode and Fast-Mode Plus.

Functional definition

- GPIO cells, including P5.0 and P5.1, cannot be hot-swapped or powered up independent of the rest of the I<sup>2</sup>C system.
- The GPIO pins P5.0 and P5.1 are over-voltage tolerant but cannot be hot-swapped or powered up independent of the rest of the I<sup>2</sup>C system
- Fast-Mode Plus has an I<sub>OL</sub> specification of 20 mA at a V<sub>OL</sub> of 0.4 V. The GPIO cells can sink a maximum of 8 mA I<sub>OL</sub> with a V<sub>OL</sub> maximum of 0.6 V.
- Fast-mode and Fast-Mode Plus specify minimum Fall times, which are not met with the GPIO cell; the Slow-Strong mode can help meet this spec depending on the bus load.

**UART mode:** This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated. Note that hardware handshaking is not supported. This is not commonly used and can be implemented with a UDB-based UART in the system, if required.

**SPI mode:** The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codex), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO for transmit and receive.

## 1.7 GPIO

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Pins 0 and 1 of Port 5 are overvoltage-tolerant pins
- Individual control of input and output buffer enabling/disabling in addition to drive-strength modes
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin-state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE).

## **1.8 Special-function peripherals**

### **1.8.1 LCD segment drive**

PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE has an LCD controller, which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

The digital correlation method modulates the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

The PWM method drives the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep mode, refreshing a small display buffer (four bits; one 32-bit register per port).

### **1.8.2 CAPSENSE™**

CAPSENSE™ is supported on all pins in PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE through a CAPSENSE™ Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CAPSENSE™ function can thus be provided on any pin or group of pins in a system under software control. A Component is provided for the CAPSENSE™ block to make it easy for the user.

The shield voltage can be driven on another mux bus to provide liquid-tolerance capability. Liquid tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CAPSENSE™ block has two IDACs which can be used for general purposes if CAPSENSE™ is not being used (both IDACs are available in that case) or if CAPSENSE™ is used without liquid tolerance (one IDAC is available).

## 2 Pinouts

**Table 1**, **Table 2**, and **Table 3** show pin list for 56-pin QFN, 68-ball WLCSP, and 76-ball WLCSP packages of PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE respectively. Port 3 consists of the high-speed analog inputs for the SAR mux. All pins support CSD CAPSENSE™ and analog mux bus connections.

**Table 1 PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list (56-pin QFN package)**

Pin	Name	Type	Description
1	VDDD	POWER	1.71-V to 5.5-V digital supply
2	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
3	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
4	XRES	RESET	Reset, active LOW
5	P4.0	GPIO	Port 4 Pin 0, lcd, csd
6	P4.1	GPIO	Port 4 Pin 1, lcd, csd
7	P5.0	GPIO	Port 5 Pin 0, lcd, csd
8	P5.1	GPIO	Port 5 Pin 1, lcd, csd
9	VSSD	GROUND	Digital ground
10	VDDR	POWER	1.9-V to 5.5-V radio supply
11	GANT1	GROUND	Antenna shielding ground
12	ANT	ANTENNA	Antenna pin
13	GANT2	GROUND	Antenna shielding ground
14	VDDR	POWER	1.9-V to 5.5-V radio supply
15	VDDR	POWER	1.9-V to 5.5-V radio supply
16	XTAL24I	CLOCK	24-MHz crystal or external clock input
17	XTAL24O	CLOCK	24-MHz crystal
18	VDDR	POWER	1.9-V to 5.5-V radio supply
19	P0.0	GPIO	Port 0 Pin 0, lcd, csd
20	P0.1	GPIO	Port 0 Pin 1, lcd, csd
21	P0.2	GPIO	Port 0 Pin 2, lcd, csd
22	P0.3	GPIO	Port 0 Pin 3, lcd, csd
23	VDDD	POWER	1.71-V to 5.5-V digital supply
24	P0.4	GPIO	Port 0 Pin 4, lcd, csd
25	P0.5	GPIO	Port 0 Pin 5, lcd, csd
26	P0.6	GPIO	Port 0 Pin 6, lcd, csd
27	P0.7	GPIO	Port 0 Pin 7, lcd, csd
28	P1.0	GPIO	Port 1 Pin 0, lcd, csd
29	P1.1	GPIO	Port 1 Pin 1, lcd, csd
30	P1.2	GPIO	Port 1 Pin 2, lcd, csd
31	P1.3	GPIO	Port 1 Pin 3, lcd, csd
32	P1.4	GPIO	Port 1 Pin 4, lcd, csd
33	P1.5	GPIO	Port 1 Pin 5, lcd, csd
34	P1.6	GPIO	Port 1 Pin 6, lcd, csd
35	P1.7	GPIO	Port 1 Pin 7, lcd, csd

Pinouts

**Table 1**      **PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list**  
**(56-pin QFN package) (continued)**

Pin	Name	Type	Description
36	VDDA	POWER	1.71-V to 5.5-V analog supply
37	P2.0	GPIO	Port 2 Pin 0, lcd, csd
38	P2.1	GPIO	Port 2 Pin 1, lcd, csd
39	P2.2	GPIO	Port 2 Pin 2, lcd, csd
40	P2.3	GPIO	Port 2 Pin 3, lcd, csd
41	P2.4	GPIO	Port 2 Pin 4, lcd, csd
42	P2.5	GPIO	Port 2 Pin 5, lcd, csd
43	P2.6	GPIO	Port 2 Pin 6, lcd, csd
44	P2.7	GPIO	Port 2 Pin 7, lcd, csd
45	VREF	REF	External reference input or bypass capacitor
46	VDDA	POWER	1.71-V to 5.5-V analog supply
47	P3.0	GPIO	Port 3 Pin 0, lcd, csd
48	P3.1	GPIO	Port 3 Pin 1, lcd, csd
49	P3.2	GPIO	Port 3 Pin 2, lcd, csd
50	P3.3	GPIO	Port 3 Pin 3, lcd, csd
51	P3.4	GPIO	Port 3 Pin 4, lcd, csd
52	P3.5	GPIO	Port 3 Pin 5, lcd, csd
53	P3.6	GPIO	Port 3 Pin 6, lcd, csd
54	P3.7	GPIO	Port 3 Pin 7, lcd, csd
55	VSSA	GROUND	Analog ground
56	VCCD	POWER	Regulated 1.8-V supply, connect to 1.3-μF capacitor.
57	EPAD	GROUND	Ground paddle for the QFN package

**Table 2**      **PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list**  
**(68-ball WLCSP package)**

Pin	Name	Type	Pin description
A1	VREF	REF	External reference input or bypass capacitor
A2	VSSA	GROUND	Analog ground
A3	P3.3	GPIO	Port 3 Pin 3, lcd, csd
A4	P3.7	GPIO	Port 3 Pin 7, lcd, csd
A5	VSSD	GROUND	Digital ground
A6	VSSA	GROUND	Analog ground
A7	VCCD	POWER	Regulated 1.8-V supply, connect to 1-μF capacitor
A8	VDDD	POWER	1.71-V to 5.5-V radio supply
B1	P2.3	GPI	Port 2 Pin 3, lcd, csd
B2	VSSA	GROUND	Analog ground
B3	P2.7	GPIO	Port 2 Pin 7, lcd, csd
B4	P3.4	GPIO	Port 3 Pin 4, lcd, csd

Pinouts

**Table 2**      **PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list**  
**(68-ball WLCSP package)** *(continued)*

Pin	Name	Type	Pin description
B5	P3.5	GPIO	Port 3 Pin 5, lcd, csd
B6	P3.6	GPIO	Port 3 Pin 6, lcd, csd
B7	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B8	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
C1	VSSA	GROUND	Analog ground
C2	P2.2	GPIO	Port 2 Pin 2, lcd, csd
C3	P2.6	GPIO	Port 2 Pin 6, lcd, csd
C4	P3.0	GPIO	Port 3 Pin 0, lcd, csd
C5	P3.1	GPIO	Port 3 Pin 1, lcd, csd
C6	P3.2	GPIO	Port 3 Pin 2, lcd, csd
C7	XRES	RESET	Reset, active LOW
C8	P4.0	GPIO	Port 4 Pin 0, lcd, csd
D1	P1.7	GPIO	Port 1 Pin 7, lcd, csd
D2	VDDA	POWER	1.71-V to 5.5-V analog supply
D3	P2.0	GPIO	Port 2 Pin 0, lcd, csd
D4	P2.1	GPIO	Port 2 Pin 1, lcd, csd
D5	P2.5	GPIO	Port 2 Pin 5, lcd, csd
D6	VSSD	GROUND	Digital ground
D7	P4.1	GPIO	Port 4 Pin 1, lcd, csd
D8	P5.0	GPIO	Port 5 Pin 0, lcd, csd
E1	P1.2	GPIO	Port 1 Pin 2, lcd, csd
E2	P1.3	GPIO	Port 1 Pin 3, lcd, csd
E3	P1.4	GPIO	Port 1 Pin 4, lcd, csd
E4	P1.5	GPIO	Port 1 Pin 5, lcd, csd
E5	P1.6	GPIO	Port 1 Pin 6, lcd, csd
E6	P2.4	GPIO	Port 2 Pin 4, lcd, csd
E7	P5.1	GPIO	Port 5 Pin 1, lcd, csd
E8	VSSD	GROUND	Digital ground
F1	VSSD	GROUND	Digital ground
F2	P0.7	GPIO	Port 0 Pin 7, lcd, csd
F3	P0.3	GPIO	Port 0 Pin 3, lcd, csd
F4	P1.0	GPIO	Port 1 Pin 0, lcd, csd
F5	P1.1	GPIO	Port 1 Pin 1, lcd, csd
F6	VSSR	GROUND	Radio ground
F7	VSSR	GROUND	Radio ground
F8	VDDR	POWER	1.9-V to 5.5-V radio supply
G1	P0.6	GPIO	Port 0 Pin 6, lcd, csd
G2	VDDD	POWER	1.71-V to 5.5-V digital supply
G3	P0.2	GPIO	Port 0 Pin 2, lcd, csd

Pinouts

**Table 2 PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list (68-ball WLCSP package) (continued)**

Pin	Name	Type	Pin description
G4	VSSD	GROUND	Digital ground
G5	VSSR	GROUND	Radio ground
G6	VSSR	GROUND	Radio ground
G7	GANT	GROUND	Antenna shielding ground
G8	VSSR	GROUND	Radio ground
H1	P0.5	GPIO	Port 0 Pin 5, lcd, csd
H2	P0.1	GPIO	Port 0 Pin 1, lcd, csd
H3	XTAL24O	CLOCK	24-MHz crystal
H4	XTAL24I	CLOCK	24-MHz crystal or external clock input
H5	VSSR	GROUND	Radio ground
H6	VSSR	GROUND	Radio ground
H7	ANT	ANTENNA	Antenna pin
J1	P0.4	GPIO	Port 0 Pin 4, lcd, csd
J2	P0.0	GPIO	Port 0 Pin 0, lcd, csd
J3	VDDR	POWER	1.9-V to 5.5-V radio supply
J6	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	No Connect	-	-

**Table 3 PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list (76-ball WLCSP package)**

Pin	Name	Type	Description
A1	NC	NC	Do not connect
A2	VREF	REF	External reference input or bypass capacitor
A3	VSSA	GROUND	Analog ground
A4	P3.3	GPIO	Port 3 Pin 3, analog/digital/lcd/csd
A5	P3.7	GPIO	Port 3 Pin 7, analog/digital/lcd/csd
A6	VSSD	GROUND	Digital ground
A7	VSSA	GROUND	Analog ground
A8	VCCD	POWER	Regulated 1.8-V supply, connect to 1-μF capacitor
A9	VDDD	POWER	1.71-V to 5.5-V digital supply
B1	NB	NO BALL	No Ball
B2	P2.3	GPIO	Port 2 Pin 3, analog/digital/lcd/csd
B3	VSSA	GROUND	Analog ground
B4	P2.7	GPIO	Port 2 Pin 7, analog/digital/lcd/csd
B5	P3.4	GPIO	Port 3 Pin 4, analog/digital/lcd/csd
B6	P3.5	GPIO	Port 3 Pin 5, analog/digital/lcd/csd
B7	P3.6	GPIO	Port 3 Pin 6, analog/digital/lcd/csd
B8	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B9	XTAL32O/P6.0	CLOCK	32.768-kHz crystal

Pinouts

**Table 3**      **PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list**  
**(76-ball WLCSP package)** *(continued)*

Pin	Name	Type	Description
C1	NC	NC	Do not connect
C2	VSSA	GROUND	Analog ground
C3	P2.2	GPIO	Port 2 Pin 2, analog/digital/lcd/csd
C4	P2.6	GPIO	Port 2 Pin 6, analog/digital/lcd/csd
C5	P3.0	GPIO	Port 3 Pin 0, analog/digital/lcd/csd
C6	P3.1	GPIO	Port 3 Pin 1, analog/digital/lcd/csd
C7	P3.2	GPIO	Port 3 Pin 2, analog/digital/lcd/csd
C8	XRES	RESET	Reset, active LOW
C9	P4.0	GPIO	Port 4 Pin 0, analog/digital/lcd/csd
D1	NC	NC	Do not connect
D2	P1.7	GPIO	Port 1 Pin 7, analog/digital/lcd/csd
D3	VDDA	POWER	1.71-V to 5.5-V analog supply
D4	P2.0	GPIO	Port 2 Pin 0, analog/digital/lcd/csd
D5	P2.1	GPIO	Port 2 Pin 1, analog/digital/lcd/csd
D6	P2.5	GPIO	Port 2 Pin 5, analog/digital/lcd/csd
D7	VSSD	GROUND	Digital ground
D8	P4.1	GPIO	Port 4 Pin 1, analog/digital/lcd/csd
D9	P5.0	GPIO	Port 5 Pin 0, analog/digital/lcd/csd
E1	NC	NC	Do not connect
E2	P1.2	GPIO	Port 1 Pin 2, analog/digital/lcd/csd
E3	P1.3	GPIO	Port 1 Pin 3, analog/digital/lcd/csd
E4	P1.4	GPIO	Port 1 Pin 4, analog/digital/lcd/csd
E5	P1.5	GPIO	Port 1 Pin 5, analog/digital/lcd/csd
E6	P1.6	GPIO	Port 1 Pin 6, analog/digital/lcd/csd
E7	P2.4	GPIO	Port 2 Pin 4, analog/digital/lcd/csd
E8	P5.1	GPIO	Port 5 Pin 1, analog/digital/lcd/csd
E9	VSSD	GROUND	Digital ground
F1	NC	NC	Do not connect
F2	VSSD	GROUND	Digital ground
F3	P0.7	GPIO	Port 0 Pin 7, analog/digital/lcd/csd
F4	P0.3	GPIO	Port 0 Pin 3, analog/digital/lcd/csd
F5	P1.0	GPIO	Port 1 Pin 0, analog/digital/lcd/csd
F6	P1.1	GPIO	Port 1 Pin 1, analog/digital/lcd/csd
F7	VSSR	GROUND	Radio ground
F8	VSSR	GROUND	Radio ground
F9	VDDR	POWER	1.9-V to 5.5-V radio supply
G1	NC	NC	Do not connect
G2	P0.6	GPIO	Port 0 Pin 6, analog/digital/lcd/csd
G3	VDDD	POWER	1.71-V to 5.5-V digital supply

Pinouts

**Table 3**      **PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE pin list**  
**(76-ball WLCSP package)** *(continued)*

<b>Pin</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
G4	P0.2	GPIO	Port 0 Pin 2, analog/digital/lcd/csd
G5	VSSD	GROUND	Digital ground
G6	VSSR	GROUND	Radio ground
G7	VSSR	GROUND	Radio ground
G8	GANT	GROUND	Antenna shielding ground
G9	VSSR	GROUND	Radio ground
H1	NC	NC	Do not connect
H2	P0.5	GPIO	Port 0 Pin 5, analog/digital/lcd/csd
H3	P0.1	GPIO	Port 0 Pin 1, analog/digital/lcd/csd
H4	XTAL24O	CLOCK	24-MHz crystal
H5	XTAL24I	CLOCK	24-MHz crystal or external clock input
H6	VSSR	GROUND	Radio ground
H7	VSSR	GROUND	Radio ground
H8	ANT	ANTENNA	Antenna pin
J1	NC	NC	Do not connect
J2	P0.4	GPIO	Port 0 Pin 4, analog/digital/lcd/csd
J3	P0.0	GPIO	Port 0 Pin 0, analog/digital/lcd/csd
J4	VDDR	POWER	1.9-V to 5.5-V radio supply
J7	VDDR	POWER	1.9-V to 5.5-V radio supply
J8	NO CONNECT	–	–

Pinouts

High-speed I/O matrix (HSIOM) is a group of high-speed switches that routes GPIOs to the resources inside the device. These resources include CAPSENSE™, TCPWMs, I<sup>2</sup>C, SPI, UART, and LCD. HSIOM\_PORT\_SELx are 32-bit-wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing as shown in [Table 4](#).

**Table 4 HSIOM port settings**

Value	Description
0	Firmware-controlled GPIO
1	Output is firmware-controlled, but Output Enable (OE) is controlled from DSI.
2	Both output and OE are controlled from DSI.
3	Output is controlled from DSI, but OE is firmware-controlled.
4	Pin is a CSD sense pin
5	Pin is a CSD shield pin
6	Pin is connected to AMUXA
7	Pin is connected to AMUXB
8	Pin-specific Active function #0
9	Pin-specific Active function #1
10	Pin-specific Active function #2
11	Reserved
12	Pin is an LCD common pin
13	Pin is an LCD segment pin
14	Pin-specific Deep-Sleep function #0
15	Pin-specific Deep-Sleep function #1

The selection of peripheral function for different GPIO pins is given in [Table 5](#).

**Table 5** Port pin connections

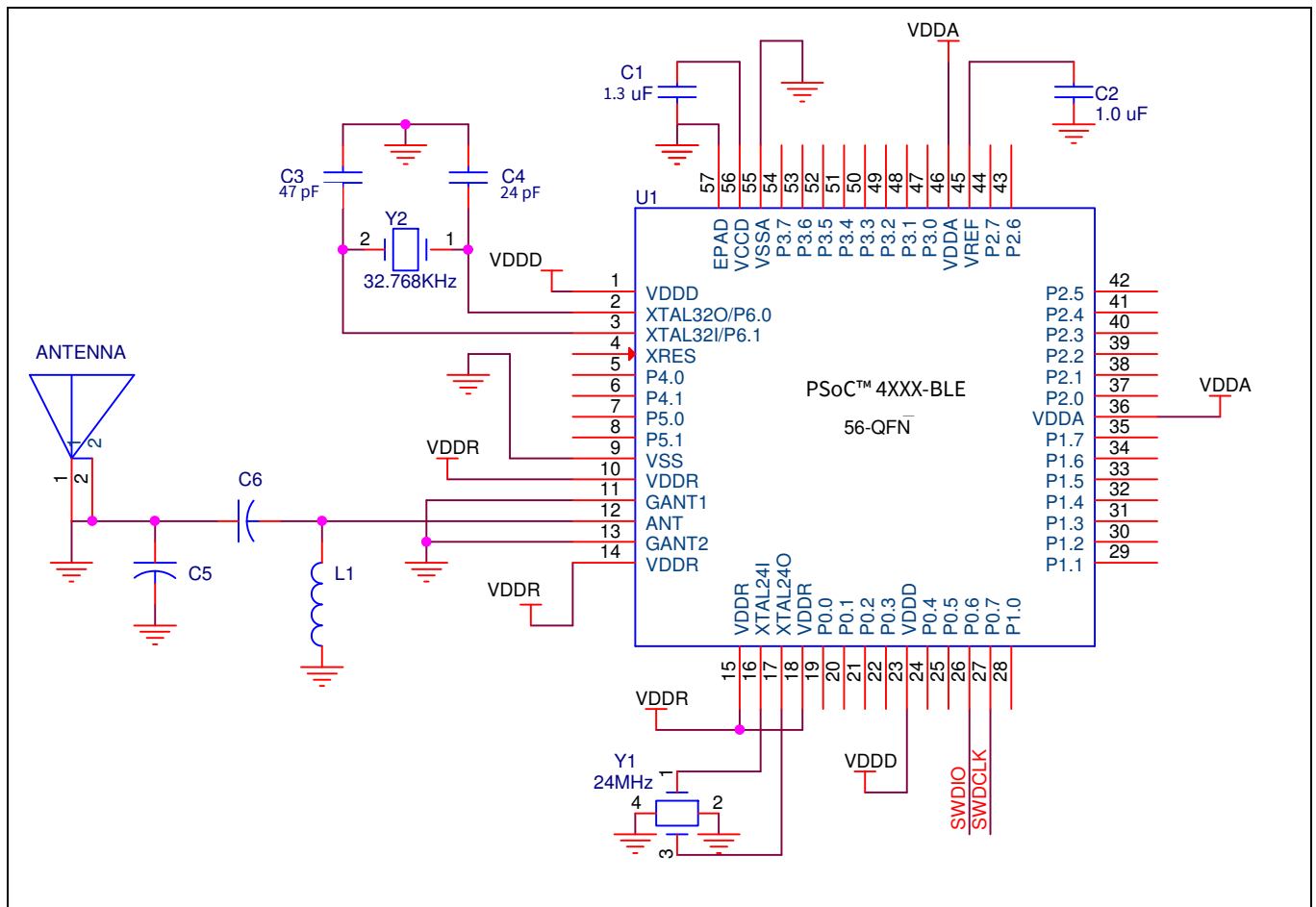
Name	Analog	Digital				
		GPIO	Active #0	Active #1	Active #2	Deep Sleep
P0.0	COMP0_INP	GPIO	TCPWM0_P[3]	SCB1_UART_RX[1]	-	SCB1_I2C_SD
P0.1	COMP0_INN	GPIO	TCPWM0_N[3]	SCB1_UART_TX[1]	-	SCB1_I2C_SC
P0.2	-	GPIO	TCPWM1_P[3]	SCB1_UART_RTS[1]	-	COMP0_OUT[0]
P0.3	-	GPIO	TCPWM1_N[3]	SCB1_UART_CTS[1]	-	COMP1_OUT[0]
P0.4	COMP1_INP	GPIO	TCPWM1_P[0]	SCB0_UART_RX[1]	EXT_CLK[0]/ ECO_OUT[0]	SCB0_I2C_SD
P0.5	COMP1_INN	GPIO	TCPWM1_N[0]	SCB0_UART_TX[1]	-	SCB0_I2C_SC
P0.6	-	GPIO	TCPWM2_P[0]	SCB0_UART_RTS[1]	-	SWDIO[0]
P0.7	-	GPIO	TCPWM2_N[0]	SCB0_UART_CTS[1]	-	SWDCLK[0]
P1.0	CTBm1_OA0_INP	GPIO	TCPWM0_P[1]	-	-	COMP0_OUT[0]
P1.1	CTBm1_OA0_INN	GPIO	TCPWM0_N[1]	-	-	COMP1_OUT[0]
P1.2	CTBm1_OA0_OUT	GPIO	TCPWM1_P[1]	-	-	-
P1.3	CTBm1_OA1_OUT	GPIO	TCPWM1_N[1]	-	-	-
P1.4	CTBm1_OA1_INN	GPIO	TCPWM2_P[1]	SCB0_UART_RX[0]	-	SCB0_I2C_SD
P1.5	CTBm1_OA1_INP	GPIO	TCPWM2_N[1]	SCB0_UART_TX[0]	-	SCB0_I2C_SC
P1.6	CTBm1_OA0_INP	GPIO	TCPWM3_P[1]	SCB0_UART_RTS[0]	-	-
P1.7	CTBm1_OA1_INP	GPIO	TCPWM3_N[1]	SCB0_UART_CTS[0]	-	-
P2.0	CTBm0_OA0_INP	GPIO	-	-	-	-
P2.1	CTBm0_OA0_INN	GPIO	-	-	-	-
P2.2	CTBm0_OA0_OUT	GPIO	-	-	-	WAKEUP
P2.3	CTBm0_OA1_OUT	GPIO	-	-	-	-
P2.4	CTBm0_OA1_INN	GPIO	-	-	-	-
P2.5	CTBm0_OA1_INP	GPIO	-	-	-	-
P2.6	CTBm0_OA0_INP	GPIO	-	-	-	-
P2.7	CTBm0_OA1_INP	GPIO	-	-	EXT_CLK[1]/ECO_OUT[1]	-
P3.0	SARMUX_0	GPIO	TCPWM0_P[2]	SCB0_UART_RX[2]	-	SCB0_I2C_SD
P3.1	SARMUX_1	GPIO	TCPWM0_N[2]	SCB0_UART_TX[2]	-	SCB0_I2C_SC
P3.2	SARMUX_2	GPIO	TCPWM1_P[2]	SCB0_UART_RTS[2]	-	-
P3.3	SARMUX_3	GPIO	TCPWM1_N[2]	SCB0_UART_CTS[2]	-	-

**Table 5** Port pin connections (continued)

Name	Analog	Digital					
		GPIO	Active #0	Active #1	Active #2	Deep Sle	
P3.4	SARMUX_4	GPIO	TCPWM2_P[2]	SCB1_UART_RX[2]	-	SCB1_I2C_SD	
P3.5	SARMUX_5	GPIO	TCPWM2_N[2]	SCB1_UART_TX[2]	-	SCB1_I2C_SC	
P3.6	SARMUX_6	GPIO	TCPWM3_P[2]	SCB1_UART_RTS[2]	-	-	
P3.7	SARMUX_7	GPIO	TCPWM3_N[2]	SCB1_UART_CTS[2]	-	-	
P4.0	CMOD	GPIO	TCPWM0_P[0]	SCB1_UART_RTS[0]	-	-	
P4.1	CTANK	GPIO	TCPWM0_N[0]	SCB1_UART_CTS[0]	-	-	
P5.0	-	GPIO	TCPWM3_P[0]	SCB1_UART_RX[0]	EXTPA_EN	SCB1_I2C_SD	
P5.1	-	GPIO	TCPWM3_N[0]	SCB1_UART_TX[0]	EXT_CLK[2]/ECO_OUT[2]	SCB1_I2C_SC	
P6.0_XTAL32 O	-	GPIO	-	-	-	-	
P6.1_XTAL32I	-	GPIO	-	-	-	-	

Pinouts

The possible pin connections are shown for all analog and digital peripherals (except the radio, LCD, and CSD blocks, which were shown in **Table 1**). A typical system application connection diagram is shown in **Figure 6**.



**Figure 6** System application connection diagram

### 3 Power

The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE device can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (VDDD), analog supply (VDDA), and radio supply (VDDR) pins. Internal LDOs in the device regulate the supply voltage to the required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. Analog circuits run directly from the analog supply (VDDA) input. The device uses separate regulators for Deep Sleep and Hibernate (lowered power supply and retention) modes to minimize the power consumption. The radio stops working below 1.9 V, but the device continues to function down to 1.71 V without RF.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu$ F range in parallel with a smaller capacitor (for example, 0.1  $\mu$ F). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

**Table 6 Power supply**

<b>Power supply</b>	<b>Bypass capacitors</b>
VDDD	The internal bandgap may be bypassed with a 1- $\mu$ F to 10- $\mu$ F.
VDDA	0.1- $\mu$ F ceramic at each pin plus bulk capacitor 1- $\mu$ F to 10- $\mu$ F.
VDDR	0.1- $\mu$ F ceramic at each pin plus bulk capacitor 1- $\mu$ F to 10- $\mu$ F.
VCCD	1.3- $\mu$ F ceramic capacitor at the VCCD pin.
VREF (optional)	The internal bandgap may be bypassed with a 1- $\mu$ F to 10- $\mu$ F capacitor.

## 4 Development support

The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE family has a rich set of documentation, development tools, and online resources to assist you during your development process. See [PSoC™ 4 MCU with AIROC™ Bluetooth® LE](#) to find out more.

### 4.1 Documentation

A suite of documentation supports the PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software user guide:** A step-by-step guide for using PSoC™ Creator. The software user guide shows you how the PSoC™ Creator build process works in detail, how to use source control with PSoC™ Creator, and much more.

**Component datasheets:** The flexibility of PSoC™ allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application notes:** PSoC™ application notes discuss a particular application of PSoC™ in depth; examples include creating standard and custom Bluetooth® LE profiles. Application notes often include example projects in addition to the application note document.

**Technical reference manual (TRM):** The TRM contains all the technical detail you need to use a PSoC™ device, including a complete description of all PSoC™ registers. The TRM is available in the Documentation section at [PSoC™ 4 MCU](#).

### 4.2 Online

In addition to print documentation, the PSoC™ forums connect you with fellow PSoC™ users and experts in PSoC™ from around the world, 24 hours a day, 7 days a week.

### 4.3 Tools

With industry standard cores, programming, and debugging interfaces, the PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE family is part of a development tool ecosystem. See the [PSoC™ Creator](#) for the latest information on the revolutionary, easy to use PSoC™ Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

## 5 Electrical specifications

### 5.1 Absolute maximum ratings

**Table 7** Absolute maximum ratings<sup>[1]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID1	V <sub>DDD_ABS</sub>	Analog, digital, or radio supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )	-0.5	-	6	V	Absolute max
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	-0.5	-	1.95	V	Absolute max
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	-	V <sub>DD</sub> +0.5	V	Absolute max
SID4	I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	Absolute max
SID5	I <sub>GPIO_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	-	0.5	mA	Absolute max, current injected per pin
BID57	ESD_HBM	Electrostatic discharge human body model	2200	-	-	V	-
BID58	ESD_CDM	Electrostatic discharge charged device model	500	-	-	V	-
BID61	LU	Pin current for latch-up	-200	-	200	mA	-

#### Note

- Usage above the absolute maximum conditions listed in [Table 7](#) may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

## 5.2 Device-level specifications

All specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $T_J \leq 100^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 8 DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID6	$V_{DD}$	Power supply input voltage ( $V_{DDA} = V_{DDD} = V_{DD}$ )	1.8	–	5.5	V	With regulator enabled
SID7	$V_{DD}$	Power supply input voltage unregulated ( $V_{DDA} = V_{DDD} = V_{DD}$ )	1.71	1.8	1.89	V	Internally unregulated Supply
SID8	$V_{DDR}$	Radio supply voltage (Radio ON)	1.9	–	5.5	V	–
SID8A	$V_{DDR}$	Radio supply voltage (Radio OFF)	1.71	–	5.5	V	–
SID9	$V_{CCD}$	Digital regulator output voltage (for core logic)	–	1.8	–	V	–
SID10	$C_{VCCD}$	Digital regulator output bypass capacitor	1	1.3	1.6	$\mu\text{F}$	X5R ceramic or better

### Active mode, $V_{DD} = 1.71\text{ V to }5.5\text{ V}$

SID13	$I_{DD3}$	Execute from flash; CPU at 3 MHz	–	2.1	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$
SID14	$I_{DD4}$	Execute from flash; CPU at 3 MHz	–	–	–	mA	$T = -40^{\circ}\text{C to }85^{\circ}\text{C}$
SID15	$I_{DD5}$	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$
SID16	$I_{DD6}$	Execute from flash; CPU at 6 MHz	–	–	–	mA	$T = -40^{\circ}\text{C to }85^{\circ}\text{C}$
SID17	$I_{DD7}$	Execute from flash; CPU at 12 MHz	–	4	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$
SID18	$I_{DD8}$	Execute from flash; CPU at 12 MHz	–	–	–	mA	$T = -40^{\circ}\text{C to }85^{\circ}\text{C}$
SID19	$I_{DD9}$	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$
SID20	$I_{DD10}$	Execute from flash; CPU at 24 MHz	–	–	–	mA	$T = -40^{\circ}\text{C to }85^{\circ}\text{C}$
SID21	$I_{DD11}$	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$
SID22	$I_{DD12}$	Execute from flash; CPU at 48 MHz	–	–	–	mA	$T = -40^{\circ}\text{C to }85^{\circ}\text{C}$

### Sleep mode, $V_{DD} = 1.8\text{ to }5.5\text{ V}$

SID23	$I_{DD13}$	IMO on	–	–	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$ , $\text{SYSCLK} = 3\text{ MHz}$
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### Sleep mode, $V_{DD}$ and $V_{DDR} = 1.9\text{ to }5.5\text{ V}$

SID24	$I_{DD14}$	ECO on	–	–	–	mA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$ , $\text{SYSCLK} = 3\text{ MHz}$
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### Deep Sleep mode, $V_{DD} = 1.8\text{ to }3.6\text{ V}$

SID25	$I_{DD15}$	WDT with WCO on	–	1.5	–	$\mu\text{A}$	$T = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$
SID26	$I_{DD16}$	WDT with WCO on	–	–	–	$\mu\text{A}$	$T = -40^{\circ}\text{C to }85^{\circ}\text{C}$

Electrical specifications

**Table 8** DC specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
<b>Deep Sleep mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>							
SID27	I <sub>DD17</sub>	WDT with WCO on	-	-	-	μA	T = 25°C, V <sub>DD</sub> = 5 V
SID28	I <sub>DD18</sub>	WDT with WCO on	-	-	-	μA	T = -40°C to 85°C
<b>Deep Sleep mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator bypassed)</b>							
SID29	I <sub>DD19</sub>	WDT with WCO on	-	-	-	μA	T = 25°C
SID30	I <sub>DD20</sub>	WDT with WCO on	-	-	-	μA	T = -40°C to 85°C
<b>Deep Sleep mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>							
SID31	I <sub>DD21</sub>	Opamp on	-	-	-	μA	T = 25°C, V <sub>DD</sub> = 3.3 V
SID32	I <sub>DD22</sub>	Opamp on	-	-	-	μA	T = -40°C to 85°C
<b>Deep Sleep mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>							
SID33	I <sub>DD23</sub>	Opamp on	-	-	-	μA	T = 25°C, V <sub>DD</sub> = 5 V
SID34	I <sub>DD24</sub>	Opamp on	-	-	-	μA	T = -40°C to 85°C
<b>Deep Sleep mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator bypassed)</b>							
SID35	I <sub>DD25</sub>	Opamp on	-	-	-	μA	T = 25°C
SID36	I <sub>DD26</sub>	Opamp on	-	-	-	μA	T = -40°C to 85°C
<b>Hibernate mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>							
SID37	I <sub>DD27</sub>	GPIO and reset active	-	150	-	nA	T = 25°C, V <sub>DD</sub> = 3.3 V
SID38	I <sub>DD28</sub>	GPIO and reset active	-	-	-	nA	T = -40°C to 85°C
<b>Hibernate mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>							
SID39	I <sub>DD29</sub>	GPIO and reset active	-	-	-	nA	T = 25°C, V <sub>DD</sub> = 5 V
SID40	I <sub>DD30</sub>	GPIO and reset active	-	-	-	nA	T = -40°C to 85°C
<b>Hibernate mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator bypassed)</b>							
SID41	I <sub>DD31</sub>	GPIO and reset active	-	-	-	nA	T = 25°C
SID42	I <sub>DD32</sub>	GPIO and reset active	-	-	-	nA	T = -40°C to 85°C
<b>Stop mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>							
SID43	I <sub>DD33</sub>	Stop mode current (V <sub>DD</sub> )	-	20	-	nA	T = 25°C, V <sub>DD</sub> = 3.3 V
SID44	I <sub>DD34</sub>	Stop mode current (V <sub>DDR</sub> )	-	40	--	nA	T = 25°C, V <sub>DDR</sub> = 3.3 V
SID45	I <sub>DD35</sub>	Stop mode current (V <sub>DD</sub> )	-	-	-	nA	T = -40°C to 85°C
SID46	I <sub>DD36</sub>	Stop mode current (V <sub>DDR</sub> )	-	-	-	nA	T = -40°C to 85°C, V <sub>DDR</sub> = 1.9 V to 3.6 V

Electrical specifications

**Table 8 DC specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
<b>Stop mode, <math>V_{DD} = 3.6</math> to <math>5.5</math> V</b>							
SID47	$I_{DD37}$	Stop mode current ( $V_{DD}$ )	-	-	-	nA	$T = 25^{\circ}\text{C}$ , $V_{DD} = 5$ V
SID48	$I_{DD38}$	Stop mode current ( $V_{DDR}$ )	-	-	-	nA	$T = 25^{\circ}\text{C}$ , $V_{DDR} = 5$ V
SID49	$I_{DD39}$	Stop mode current ( $V_{DD}$ )	-	-	-	nA	$T = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$
SID50	$I_{DD40}$	Stop mode current ( $V_{DDR}$ )	-	-	-	nA	$T = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$
<b>Stop mode, <math>V_{DD} = 1.71</math> to <math>1.89</math> V (Regulator bypassed)</b>							
SID51	$I_{DD41}$	Stop mode current ( $V_{DD}$ )	-	-	-	nA	$T = 25^{\circ}\text{C}$
SID52	$I_{DD42}$	Stop mode current ( $V_{DD}$ )	-	-	-	nA	$T = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$

**Table 9 AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID53	$F_{\text{CPU}}$	CPU frequency	DC	-	48	MHz	$1.71$ V $\leq$ $V_{DD}$ $\leq$ $5.5$ V
SID54	$T_{\text{SLEEP}}$	Wakeup from Sleep mode	-	0	-	$\mu\text{s}$	Guaranteed by characterization
SID55	$T_{\text{DEEPSLEEP}}$	Wakeup from Deep Sleep mode	-	-	25	$\mu\text{s}$	24-MHz IMO. Guaranteed by characterization.
SID56	$T_{\text{HIBERNATE}}$	Wakeup from Hibernate mode	-	-	0.7	ms	Guaranteed by characterization
SID57	$T_{\text{STOP}}$	Wakeup from Stop mode	-	-	2.2	ms	Guaranteed by characterization

## 5.2.1 GPIO

**Table 10 GPIO DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID58	$V_{IH}$	Input voltage HIGH threshold	$0.7 \times V_{DD}$	-	-	V	CMOS input
SID59	$V_{IL}$	Input voltage LOW threshold	-	-	$0.3 \times V_{DD}$	V	CMOS input
SID60	$V_{IH}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	-	-	V	-
SID61	$V_{IL}$	LVTTL input, $V_{DD} < 2.7$ V	-	-	$0.3 \times V_{DD}$	V	-
SID62	$V_{IH}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	-	-	V	-
SID63	$V_{IL}$	LVTTL input, $V_{DD} \geq 2.7$ V	-	-	0.8	V	-
SID64	$V_{OH}$	Output voltage HIGH level	$V_{DD} - 0.6$	-	-	V	$I_{OH} = 4\text{-mA}$ at $3.3\text{-V } V_{DD}$
SID65	$V_{OH}$	Output voltage HIGH level	$V_{DD} - 0.5$	-	-	V	$I_{OH} = 1\text{-mA}$ at $1.8\text{-V } V_{DD}$
SID66	$V_{OL}$	Output voltage LOW level	-	-	0.6	V	$I_{OL} = 8\text{-mA}$ at $3.3\text{-V } V_{DD}$
SID67	$V_{OL}$	Output voltage LOW level	-	-	0.6	V	$I_{OL} = 4\text{-mA}$ at $1.8\text{-V } V_{DD}$
SID68	$V_{OL}$	Output voltage LOW level	-	-	0.4	V	$I_{OL} = 3\text{-mA}$ at $3.3\text{-V } V_{DD}$
SID69	Rpullup	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	-
SID70	Rpulldown	Pull-down resistor	3.5	5.6	8.5	k $\Omega$	-
SID71	$I_{IL}$	Input leakage current (absolute value)	-	-	2	nA	25°C, $V_{DD} = 3.3$ V
SID72	$I_{IL\_CTBM}$	Input leakage on CTBm input pins	-	-	4	nA	-
SID73	$C_{IN}$	Input capacitance	-	-	7	pF	-
SID74	Vhystttl	Input hysteresis LVTTL	25	40	-	mV	$V_{DD} > 2.7$ V
SID75	Vhyscmos	Input hysteresis CMOS	$0.05 \times V_{DD}$	-	-	mV	-
SID76	Iiode	Current through protection diode to $V_{DD}/V_{SS}$	-	-	100	$\mu$ A	-
SID77	$I_{TOT\_GPIO}$	Maximum total source or sink chip current	-	-	200	mA	-

**Note**

2.  $V_{IH}$  must not exceed  $V_{DD} + 0.2$  V.

Electrical specifications

**Table 11 GPIO AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID78	T <sub>RISEF</sub>	Rise time in Fast-Strong mode	2	-	12	ns	3.3-V V <sub>DDD</sub> , C <sub>LOAD</sub> = 25-pF
SID79	T <sub>FALLF</sub>	Fall time in Fast-Strong mode	2	-	12	ns	3.3-V V <sub>DDD</sub> , C <sub>LOAD</sub> = 25-pF
SID80	T <sub>RISES</sub>	Rise time in Slow-Strong mode	10	-	60	-	3.3-V V <sub>DDD</sub> , C <sub>LOAD</sub> = 25-pF
SID81	T <sub>FALLS</sub>	Fall time in Slow-Strong mode	10	-	60	-	3.3-V V <sub>DDD</sub> , C <sub>LOAD</sub> = 25-pF
SID82	F <sub>GPIOUT1</sub>	GPIO Fout; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V. Fast-Strong mode	-	-	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83	F <sub>GPIOUT2</sub>	GPIO Fout; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V. Fast-Strong mode	-	-	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID84	F <sub>GPIOUT3</sub>	GPIO Fout; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V. Slow-Strong mode	-	-	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID85	F <sub>GPIOUT4</sub>	GPIO Fout; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V. Slow-Strong mode	-	-	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID86	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V	-	-	48	MHz	90/10% V <sub>IO</sub>

**Table 12 OVT GPIO DC specifications (P5\_0 and P5\_1 Only)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID71A	I <sub>IL</sub>	Input leakage current (absolute value), V <sub>IH</sub> > V <sub>DD</sub>	-	-	10	μA	25°C, V <sub>DD</sub> = 0 V, V <sub>IH</sub> = 3.0 V
SID66A	V <sub>OL</sub>	Output voltage LOW level	-	-	0.4	V	I <sub>OL</sub> = 20-mA, V <sub>DD</sub> > 2.9-V

**Table 13 OVT GPIO AC specifications (P5\_0 and P5\_1 only)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID78A	T <sub>RISE_OVFS</sub>	Output rise time in Fast-Strong mode	1.5	-	12	ns	25-pF load, 10%-90%, V <sub>DD</sub> =3.3-V
SID79A	T <sub>FALL_OVFS</sub>	Output fall time in Fast-Strong mode	1.5	-	12	ns	25-pF load, 10%-90%, V <sub>DD</sub> =3.3-V
SID80A	T <sub>RISSS</sub>	Output rise time in Slow-Strong mode	10	-	60	ns	25-pF load, 10%-90%, V <sub>DD</sub> =3.3-V
SID81A	T <sub>FALLSS</sub>	Output fall time in Slow-Strong mode	10	-	60	ns	25-pF load, 10%-90%, V <sub>DD</sub> =3.3-V

Electrical specifications

**Table 13 OVT GPIO AC specifications (P5\_0 and P5\_1 only) (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID82A	F <sub>GPIOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID83A	F <sub>GPIOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25-pF load, 60/40 duty cycle

## 5.2.2 XRES

**Table 14 XRES DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID87	V <sub>IH</sub>	Input voltage HIGH threshold	0.7 × V <sub>DDD</sub>	–	–	V	CMOS input
SID88	V <sub>IL</sub>	Input voltage LOW threshold	–	–	0.3 × V <sub>DDD</sub>	V	CMOS input
SID89	R <sub>pullup</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID90	C <sub>IN</sub>	Input capacitance	–	3	–	pF	–
SID91	V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	–
SID92	I <sub>DIODE</sub>	Current through protection diode to V <sub>DDD</sub> /V <sub>SS</sub>	–	–	100	μA	–

**Table 15 XRES AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	T <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–

Electrical specifications

## 5.3 Analog peripherals

### 5.3.1 Opamp

**Table 16 Opamp specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>I<sub>DD</sub> (Opamp block current. V<sub>DD</sub> = 1.8 V. No load)</b>							
SID94	I <sub>DD_HI</sub>	Power = high	–	1000	1850	μA	–
SID95	I <sub>DD_MED</sub>	Power = medium	–	500	950	μA	–
SID96	I <sub>DD_LOW</sub>	Power = low	–	250	350	μA	–
<b>GBW (Load = 20 pF, 0.1 mA. V<sub>DDA</sub> = 2.7 V)</b>							
SID97	GBW_HI	Power = high	6	–	–	MHz	–
SID98	GBW_MED	Power = medium	4	–	–	MHz	–
SID99	GBW_LO	Power = low	–	1	–	MHz	–
<b>I<sub>OUT_MAX</sub> (V<sub>DDA</sub> ≥ 2.7 V, 500 mV from rail)</b>							
SID100	I <sub>OUT_MAX_HI</sub>	Power = high	10	–	–	mA	–
SID101	I <sub>OUT_MAX_MID</sub>	Power = medium	10	–	–	mA	–
SID102	I <sub>OUT_MAX_LO</sub>	Power = low	–	5	–	mA	–
<b>I<sub>OUT</sub> (V<sub>DDA</sub> = 1.71 V, 500 mV from rail)</b>							
SID103	I <sub>OUT_MAX_HI</sub>	Power = high	4	–	–	mA	–
SID104	I <sub>OUT_MAX_MID</sub>	Power = medium	4	–	–	mA	–
SID105	I <sub>OUT_MAX_LO</sub>	Power = low	–	2	–	mA	–
SID106	V <sub>IN</sub>	Charge pump on, V <sub>DDA</sub> ≥ 2.7 V	–0.05	–	V <sub>DDA</sub> – 0.2	V	–
SID107	V <sub>CM</sub>	Charge pump on, V <sub>DDA</sub> ≥ 2.7 V	–0.05	–	V <sub>DDA</sub> – 0.2	V	–
<b>V<sub>OUT</sub> (V<sub>DDA</sub> ≥ 2.7 V)</b>							
SID108	V <sub>OUT_1</sub>	Power = high, I <sub>LOAD</sub> =10 mA	0.5	–	V <sub>DDA</sub> – 0.5	V	–
SID109	V <sub>OUT_2</sub>	Power = high, I <sub>LOAD</sub> =1 mA	0.2	–	V <sub>DDA</sub> – 0.2	V	–
SID110	V <sub>OUT_3</sub>	Power = medium, I <sub>LOAD</sub> =1 mA	0.2	–	V <sub>DDA</sub> – 0.2	V	–
SID111	V <sub>OUT_4</sub>	Power = low, I <sub>LOAD</sub> =0.1 mA	0.2	–	V <sub>DDA</sub> – 0.2	V	–
SID112	V <sub>OS_TR</sub>	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID113	V <sub>OS_TR</sub>	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID114	V <sub>OS_TR</sub>	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID115	V <sub>OS_DR_TR</sub>	Offset voltage drift, trimmed	–10	±3	10	μV/C	High mode
SID116	V <sub>OS_DR_TR</sub>	Offset voltage drift, trimmed	–	±10	–	μV/C	Medium mode
SID117	V <sub>OS_DR_TR</sub>	Offset voltage drift, trimmed	–	±10	–	μV/C	Low mode
SID118	CMRR	DC	70	80	–	dB	V <sub>DD</sub> = 3.6-V
SID119	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V <sub>DD</sub> = 3.6-V

Electrical specifications

**Table 16 Opamp specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>Noise</b>							
SID120	V <sub>N1</sub>	Input referred, 1 Hz–1 GHz, power = high	–	94	–	μVrms	–
SID121	V <sub>N2</sub>	Input referred, 1-kHz, power = high	–	72	–	nV/rtHz	–
SID122	V <sub>N3</sub>	Input referred, 10-kHz, power = high	–	28	–	nV/rtHz	–
SID123	V <sub>N4</sub>	Input referred, 100-kHz, power = high	–	15	–	nV/rtHz	–
SID124	C <sub>LOAD</sub>	Stable up to maximum load. Performance specs at 50 pF	–	–	125	pF	–
SID125	Slew_rate	Clload = 50 pF, Power = High, V <sub>DDA</sub> ≥ 2.7 V	6	–	–	V/μsec	–
SID126	T <sub>op_wake</sub>	From disable to enable, no external RC dominating	–	300	–	μsec	–
<b>Comp_mode (Comparator mode; 50-mV drive, T<sub>RISE</sub> = T<sub>FALL</sub> (approx.))</b>							
SID127	T <sub>PD1</sub>	Response time; power = high	–	150	–	nsec	–
SID128	T <sub>PD2</sub>	Response time; power = medium	–	400	–	nsec	–
SID129	T <sub>PD3</sub>	Response time; power = low	–	2000	–	nsec	–
SID130	V <sub>hyst_op</sub>	Hysteresis	–	10	–	mV	–
<b>Deep Sleep (Deep Sleep mode operation is only guaranteed for V<sub>DDA</sub> &gt; 2.5 V)</b>							
SID131	GBW_DS	Gain bandwidth product	–	50	–	kHz	–
SID132	IDD_DS	Current	–	15	–	μA	–
SID133	V <sub>os_DS</sub>	Offset voltage	–	5	–	mV	–
SID134	V <sub>os_dr_DS</sub>	Offset voltage drift	–	20	–	μV/°C	–
SID135	V <sub>out_DS</sub>	Output voltage	0.2	–	V <sub>DD</sub> –0.2	V	–
SID136	V <sub>cm_DS</sub>	Common mode voltage	0.2	–	V <sub>DD</sub> –1.8	V	–

**Table 17 Comparator DC specifications<sup>[3]</sup>**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID140	V <sub>OFFSET1</sub>	Input offset voltage, Factory trim	–	–	±10	mV	–
SID141	V <sub>OFFSET2</sub>	Input offset voltage, Custom trim	–	–	±6	mV	–
SID141A	V <sub>OFFSET3</sub>	Input offset voltage, ultra-low-power mode	–	±12	–	mV	V <sub>DDD</sub> ≥ 2.6 V for Temp < 0°C, V <sub>DDD</sub> ≥ 1.8 V for Temp > 0°C
SID142	V <sub>HYST</sub>	Hysteresis when enabled. Common Mode voltage range from 0 to VDD –1	–	10	35	mV	–

**Note**

3. ULP LCOMP operating conditions:  
 - V<sub>DDD</sub> 2.6 V–5.5 V for datasheet temp range < 0°C  
 - V<sub>DDD</sub> 1.8 V–5.5 V for datasheet temp range ≥ 0°C

Electrical specifications

**Table 17** Comparator DC specifications<sup>[3]</sup> (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID143	V <sub>ICM1</sub>	Input common mode voltage in normal mode	0	–	V <sub>DDD</sub> – 0.1	V	Modes 1 and 2
SID144	V <sub>ICM2</sub>	Input common mode voltage in low power mode	0	–	V <sub>DDD</sub>	V	–
SID145	V <sub>ICM3</sub>	Input common mode voltage in ultra low power mode	0	–	V <sub>DDD</sub> – 1.15	V	V <sub>DDD</sub> ≥ 2.6 V for Temp < 0°C, V <sub>DDD</sub> ≥ 1.8 V for Temp > 0°C
SID146	CMRR	Common mode rejection ratio	50	–	–	dB	V <sub>DDD</sub> ≥ 2.7 V
SID147	CMRR	Common mode rejection ratio	42	–	–	dB	V <sub>DDD</sub> ≤ 2.7 V
SID148	I <sub>CMP1</sub>	Block current, normal mode	–	–	400	μA	–
SID149	I <sub>CMP2</sub>	Block current, low power mode	–	–	100	μA	–
SID150	I <sub>CMP3</sub>	Block current in ultra low-power mode	–	6	–	μA	V <sub>DDD</sub> ≥ 2.6 V for Temp < 0°C, V <sub>DDD</sub> ≥ 1.8 V for Temp > 0°C
SID151	Z <sub>CMP</sub>	DC input impedance of comparator	35	–	–	MΩ	–

**Note**

3. ULP LCOMP operating conditions:  
 - V<sub>DDD</sub> 2.6 V-5.5 V for datasheet temp range < 0°C  
 - V<sub>DDD</sub> 1.8 V-5.5 V for datasheet temp range ≥ 0°C

**Table 18** Comparator AC specifications<sup>[3]</sup>

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID152	T <sub>RESP1</sub>	Response time, normal mode, 50-mV overdrive	–	38	–	ns	50-mV overdrive
SID153	T <sub>RESP2</sub>	Response time, low power mode, 50-mV overdrive	–	70	–	ns	50-mV overdrive
SID154	T <sub>RESP3</sub>	Response time, ultra-low-power mode, 50-mV overdrive	–	2.3	–	μs	200-mV overdrive. V <sub>DDD</sub> ≥ 2.6 V for Temp < 0°C, V <sub>DDD</sub> ≥ 1.8 V for Temp > 0°C

**5.3.2 Temperature sensor**

**Table 19** Temperature sensor specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID155	T <sub>SENSACC</sub>	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85°C

Electrical specifications

### 5.3.3 SAR ADC

**Table 20 SAR ADC DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID156	A_RES	Resolution	-	-	12	bits	-
SID157	A_CHNIS_S	Number of channels - single-ended	-	-	16	-	8 full-speed
SID158	A-CHNKS_D	Number of channels - differential	-	-	8	-	Diff inputs use neighboring I/O
SID159	A-MONO	Monotonicity	-	-	-	-	Yes
SID160	A_GAINERR	Gain error	-	-	±0.1	%	With external reference.
SID161	A_OFFSET	Input offset voltage	-	-	2	mV	Measured with 1-V V <sub>REF</sub>
SID162	A_ISAR	Current consumption	-	-	1	mA	-
SID163	A_VINS	Input voltage range - single-ended	V <sub>SS</sub>	-	V <sub>DDA</sub>	V	-
SID164	A_VIND	Input voltage range - differential	V <sub>SS</sub>	-	V <sub>DDA</sub>	V	-
SID165	A_INRES	Input resistance	-	-	2.2	kΩ	-
SID166	A_INCAP	Input capacitance	-	-	10	pF	-
SID312	VREFSAR	Trimmed internal reference to SAR	-1	-	1	%	Percentage of V <sub>bg</sub> (1.024-V)

**Table 21 SAR ADC AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID167	A_psrr	Power supply rejection ratio	70	-	-	dB	Measured at 1-V reference
SID168	A_cmrr	Common mode rejection ratio	66	-	-	dB	-
SID169	A_samp	Sample rate	-	-	1	Msp/s	-
SID313	Fsarintref	SAR operating speed without external ref. bypass	-	-	100	Ksps	12-bit resolution
SID170	A_snr	Signal-to-noise ratio (SNR)	65	-	-	dB	F <sub>in</sub> = 10 kHz
SID171	A_bw	Input bandwidth without aliasing	-	-	A <sub>samp</sub> /2	kHz	-
SID172	A_inl	Integral non linearity. V <sub>DD</sub> = 1.71 to 5.5 V, 1 Msps	-1.7	-	2	LSB	V <sub>ref</sub> = 1 V to V <sub>DD</sub>
SID173	A_INL	Integral non linearity. V <sub>DDD</sub> = 1.71 to 3.6 V, 1 Msps	-1.5	-	1.7	LSB	V <sub>ref</sub> = 1.71 V to V <sub>DD</sub>
SID174	A_INL	Integral non linearity. V <sub>DD</sub> = 1.71 to 5.5 V, 500 Ksps	-1.5	-	1.7	LSB	V <sub>ref</sub> = 1 V to V <sub>DD</sub>
SID175	A_dnl	Differential non linearity. V <sub>DD</sub> = 1.71 to 5.5 V, 1 Msps	-1	-	2.2	LSB	V <sub>ref</sub> = 1 V to V <sub>DD</sub>
SID176	A_DNL	Differential non linearity. V <sub>DD</sub> = 1.71 to 3.6 V, 1 Msps	-1	-	2	LSB	V <sub>ref</sub> = 1.71 V to V <sub>DD</sub>

Electrical specifications

**Table 21 SAR ADC AC specifications (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID177	A_DNL	Differential non linearity. $V_{DD} = 1.71$ to $5.5$ V, 500 Ksps	-1	-	2.2	LSB	$V_{ref} = 1$ V to $V_{DD}$
SID178	A_thd	Total harmonic distortion	-	-	-65	dB	$F_{in} = 10$ kHz

### 5.3.4 CSD

**Table 22 CSD block specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID179	$V_{CSD}$	Voltage range of operation	1.71	-	5.5	V	-
SID180	IDAC1	DNL for 8-bit resolution	-1	-	1	LSB	-
SID181	IDAC1	INL for 8-bit resolution	-3	-	3	LSB	-
SID182	IDAC2	DNL for 7-bit resolution	-1	-	1	LSB	-
SID183	IDAC2	INL for 7-bit resolution	-3	-	3	LSB	-
SID184	SNR	Ratio of counts of finger to noise	5	-	-	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity. Radio is not operating during the scan
SID185	$I_{DAC1\_CRT1}$	Output current of IDAC1 (8 bits) in High range	-	612	-	$\mu$ A	-
SID186	$I_{DAC1\_CRT2}$	Output current of IDAC1 (8 bits) in Low range	-	306	-	$\mu$ A	-
SID187	$I_{DAC2\_CRT1}$	Output current of IDAC2 (7 bits) in High range	-	305	-	$\mu$ A	-
SID188	$I_{DAC2\_CRT2}$	Output current of IDAC2 (7 bits) in Low range	-	153	-	$\mu$ A	-

Electrical specifications

## 5.4 Digital peripherals

### 5.4.1 Timer

**Table 23 Timer DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID189	$I_{TIM1}$	Block current consumption at 3 MHz	–	–	50	µA	16-bit timer
SID190	$I_{TIM2}$	Block current consumption at 12 MHz	–	–	175	µA	16-bit timer
SID191	$I_{TIM3}$	Block current consumption at 48 MHz	–	–	712	µA	16-bit timer

**Table 24 Timer AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID192	$T_{TIMFREQ}$	Operating frequency	$F_{CLK}$	–	48	MHz	–
SID193	$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID194	$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID195	$T_{TIMRES}$	Timer resolution	$T_{CLK}$	–	–	ns	–
SID196	$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID197	$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID198	$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID199	$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Electrical specifications

## 5.4.2 Counter

**Table 25 Counter DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID200	I <sub>CTR1</sub>	Block current consumption at 3 MHz	–	–	50	µA	16-bit counter
SID201	I <sub>CTR2</sub>	Block current consumption at 12 MHz	–	–	175	µA	16-bit counter
SID202	I <sub>CTR3</sub>	Block current consumption at 48 MHz	–	–	712	µA	16-bit counter

**Table 26 Counter AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID203	T <sub>CTRFREQ</sub>	Operating frequency	F <sub>CLK</sub>	–	48	MHz	–
SID204	T <sub>CTRPWINT</sub>	Capture pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
SID205	T <sub>CTRPWEXT</sub>	Capture pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
SID206	T <sub>CTRES</sub>	Counter Resolution	T <sub>CLK</sub>	–	–	ns	–
SID207	T <sub>CENWIDINT</sub>	Enable pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
SID208	T <sub>CENWIDEXT</sub>	Enable pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
SID209	T <sub>CTRRE-SWINT</sub>	Reset pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
SID210	T <sub>CTRRE-SWEXT</sub>	Reset pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–

Electrical specifications

### 5.4.3 Pulse width modulation (PWM)

**Table 27 PWM DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID211	$I_{P_{PWM1}}$	Block current consumption at 3 MHz	–	–	50	μA	16-bit PWM
SID212	$I_{P_{PWM2}}$	Block current consumption at 12 MHz	–	–	175	μA	16-bit PWM
SID213	$I_{P_{PWM3}}$	Block current consumption at 48 MHz	–	–	741	μA	16-bit PWM

**Table 28 PWM AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID214	$T_{P_{PWFREQ}}$	Operating frequency	$F_{CLK}$	–	48	MHz	–
SID215	$T_{P_{PWMPWINT}}$	Pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID216	$T_{P_{PWXEXT}}$	Pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID217	$T_{P_{PWKILLINT}}$	Kill pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID218	$T_{P_{PWKILLEXT}}$	Kill pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID219	$T_{P_{PWMEINT}}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID220	$T_{P_{PWMEEXT}}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID221	$T_{P_{PWRRESWINT}}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID222	$T_{P_{PWRRESWEXT}}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

### 5.4.4 I<sup>2</sup>C

**Table 29 Fixed I<sup>2</sup>C DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID223	$I_{I2C1}$	Block current consumption at 100 kHz	–	–	50	μA	–
SID224	$I_{I2C2}$	Block current consumption at 400 kHz	–	–	155	μA	–
SID225	$I_{I2C3}$	Block current consumption at 1 Mbps	–	–	390	μA	–
SID226	$I_{I2C4}$	I <sup>2</sup> C enabled in Deep Sleep mode	–	–	1.4	μA	–

**Table 30 Fixed I<sup>2</sup>C AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID227	$F_{I2C1}$	Bit rate	–	–	1	Mbps	–

Electrical specifications

### 5.4.5 LCD direct drive

**Table 31 LCD direct drive DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID228	$I_{LCDLOW}$	Operating current in low-power mode	-	17.5	-	$\mu A$	16 × 4 small segment display at 50 Hz
SID229	$C_{LCDCAP}$	LCD capacitance per segment/common driver	-	500	5000	pF	-
SID230	$LCD_{OFFSET}$	Long-term segment offset	-	20	-	mV	-
SID231	$I_{LCDOP1}$	LCD system operating current $V_{BIAS} = 5 V$ .	-	2	-	mA	32 × 4 segments. 50 Hz at 25°C
SID232	$I_{LCDOP2}$	LCD system operating current. $V_{BIAS} = 3.3 V$	-	2	-	mA	32 × 4 segments 50 Hz at 25°C

**Table 32 LCD direct drive AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID233	$F_{LCD}$	LCD frame rate	10	50	150	Hz	-

**Table 33 Fixed UART DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID234	$I_{UART1}$	Block current consumption at 100 kbps	-	-	55	$\mu A$	-
SID235	$I_{UART2}$	Block current consumption at 1000 kbps	-	-	360	$\mu A$	-

**Table 34 Fixed UART AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID236	$F_{UART}$	Bit rate	-	-	1	Mbps	-

Electrical specifications

## 5.4.6 SPI specifications

**Table 35 Fixed SPI DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID237	I <sub>SPI1</sub>	Block current consumption at 1 Mbps	-	-	360	µA	-
SID238	I <sub>SPI2</sub>	Block current consumption at 4 Mbps	-	-	560	µA	-
SID239	I <sub>SPI3</sub>	Block current consumption at 8 Mbps	-	-	600	µA	-

**Table 36 Fixed SPI AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID240	F <sub>SPI</sub>	SPI operating frequency (master; 6X oversampling)	-	-	8	MHz	-

**Table 37 Fixed SPI Master mode AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID241	T <sub>DMO</sub>	MOSI valid after Sclock driving edge	-	-	18	ns	-
SID242	T <sub>DSI</sub>	MISO valid before Sclock capturing edge. Full clock, late MISO sampling used	20	-	-	ns	Full clock, late MISO sampling
SID243	T <sub>HMO</sub>	Previous MOSI data hold time	0	-	-	ns	Referred to Slave capturing edge

**Table 38 Fixed SPI Slave mode AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID244	T <sub>DMI</sub>	MOSI valid before Sclock capturing edge	40	-	-	ns	-
SID245	T <sub>DSO</sub>	MISO valid after Sclock driving edge	-	-	42 + 3 × T <sub>CPU</sub>	ns	-
SID246	T <sub>DSO_ext</sub>	MISO valid after Sclock driving edge in external clock mode	-	-	53	ns	V <sub>DD</sub> < 3.0 V
SID247	T <sub>HSO</sub>	Previous MISO data hold time	0	-	-	ns	-
SID248	T <sub>SSELSCK</sub>	SSEL valid to first SCK valid edge	100	-	-	ns	-

## 5.5 Memory

**Table 39 Flash DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID249	V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	–
SID309	T <sub>WS48</sub>	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
SID310	T <sub>WS32</sub>	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
SID311	T <sub>WS16</sub>	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

**Table 40 Flash AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID250	T <sub>ROWWRITE</sub> <sup>[4]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes for 128 KB flash devices Row (block) = 256 bytes for 256 KB flash devices
SID251	T <sub>ROWERASE</sub> <sup>[4]</sup>	Row erase time	–	–	13	ms	–
SID252	T <sub>ROWPROGRAM</sub> <sup>[4]</sup>	Row program time after erase	–	–	7	ms	–
SID253	T <sub>BULKERASE</sub> <sup>[4]</sup>	Bulk erase time (256 KB)	–	–	35	ms	–
SID254	T <sub>DEVPROG</sub> <sup>[4]</sup>	Total device program time	–	–	50	seconds	256 KB
SID254A			–	–	25		128 KB
SID255	F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	–
SID256	F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55°C, 100 K P/E cycles	20	–	–	years	–
SID257	F <sub>RET2</sub>	Flash retention. T <sub>A</sub> ≤ 85°C, 10 K P/E cycles	10	–	–	years	–

**Note**

4. It can take as much as 20 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

Electrical specifications

## 5.6 System resources

### 5.6.1 Power-on reset (POR)

**Table 41** POR DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID258	V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	–	1.45	V	–
SID259	V <sub>FALLIPOR</sub>	Falling trip voltage	0.75	–	1.40	V	–
SID260	V <sub>IPORHYST</sub>	Hysteresis	15	–	200	mV	–

**Table 42** POR AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID264	T <sub>PPOR_TR</sub>	PPOR response time in Active and Sleep modes	–	–	1	μs	–

**Table 43** Brown-out detect

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID261	V <sub>FALLPPOR</sub>	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
SID262	V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep mode	1.4	–	–	V	–

**Table 44** Hibernate reset

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID263	V <sub>HBRTRIP</sub>	BOD trip voltage in Hibernate mode	1.1	–	–	V	–

## 5.6.2 Voltage monitors

**Table 45 Voltage monitor DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID265	V <sub>LVI1</sub>	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	-
SID266	V <sub>LVI2</sub>	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	-
SID267	V <sub>LVI3</sub>	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	-
SID268	V <sub>LVI4</sub>	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	-
SID269	V <sub>LVI5</sub>	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	-
SID270	V <sub>LVI6</sub>	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	-
SID271	V <sub>LVI7</sub>	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	-
SID272	V <sub>LVI8</sub>	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	-
SID273	V <sub>LVI9</sub>	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	-
SID274	V <sub>LVI10</sub>	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	-
SID2705	V <sub>LVI11</sub>	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	-
SID276	V <sub>LVI12</sub>	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	-
SID277	V <sub>LVI13</sub>	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	-
SID278	V <sub>LVI14</sub>	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	-
SID279	V <sub>LVI15</sub>	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	-
SID280	V <sub>LVI16</sub>	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	-
SID281	LVI_IDD	Block current	-	-	100	μA	-

**Table 46 Voltage monitor AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID282	T <sub>MONTRIP</sub>	Voltage monitor trip time	-	-	1	μs	-

## 5.6.3 SWD interface

**Table 47 SWD interface specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID283	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-	-	14	MHz	SWDCCLK ≤ 1/3 CPU clock frequency
SID284	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	-	-	7	MHz	SWDCCLK ≤ 1/3 CPU clock frequency
SID285	T_SWDI_SETUP	$T = 1/f\text{ SWDCCLK}$	$0.25 \times T$	-	-	ns	-
SID286	T_SWDI_HOLD	$T = 1/f\text{ SWDCCLK}$	$0.25 \times T$	-	-	ns	-
SID287	T_SWDO_VALID	$T = 1/f\text{ SWDCCLK}$	-	-	$0.5 \times T$	ns	-
SID288	T_SWDO_HOLD	$T = 1/f\text{ SWDCCLK}$	1	-	-	ns	-

Electrical specifications

## 5.6.4 Internal main oscillator

**Table 48** IMO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID289	I <sub>IMO1</sub>	IMO operating current at 48 MHz	–	–	1000	µA	–
SID290	I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	325	µA	–
SID291	I <sub>IMO3</sub>	IMO operating current at 12 MHz	–	–	225	µA	–
SID292	I <sub>IMO4</sub>	IMO operating current at 6 MHz	–	–	180	µA	–
SID293	I <sub>IMO5</sub>	IMO operating current at 3 MHz	–	–	150	µA	–

**Table 49** IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID296	F <sub>IMOTOL3</sub>	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	F <sub>IMOTOL3</sub>	IMO startup time	–	–	12	µs	–

## 5.6.5 Internal low-speed oscillator

**Table 50** ILO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID298	I <sub>ILO2</sub>	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

**Table 51** ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID299	T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	–
SID300	F <sub>ILOTRIM1</sub>	32-kHz trimmed frequency	15	32	50	kHz	–

**Table 52** External clock specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	–	55	%	CMOS input level only

Electrical specifications

**Table 53 UDB AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
<b>Data path performance</b>							
SID303	F <sub>MAX-TIMER</sub>	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID304	F <sub>MAX-ADDER</sub>	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID305	F <sub>MAX_CRC</sub>	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
<b>PLD performance in UDB</b>							
SID306	F <sub>MAX_PLD</sub>	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
<b>Clock to output performance</b>							
SID307	T <sub>CLK_OUT_UDB1</sub>	Prop. delay for clock in to data out at 25°C, Typical	–	15	–	ns	–
SID308	T <sub>CLK_OUT_UDB2</sub>	Prop. delay for clock in to data out, Worst case	–	25	–	ns	–

Electrical specifications

**Table 54 Bluetooth® LE subsystem**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
<b>RF receiver specification</b>							
SID340	RXS, IDLE	RX sensitivity with idle transmitter	-	-89	-	dBm	-
SID340A		RX sensitivity with idle transmitter excluding Balun loss	-	-91	-	dBm	Guaranteed by design simulation
SID341	RXS, DIRTY	RX sensitivity with dirty transmitter	-	-87	-70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID342	RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	-	-91	-	dBm	-
SID343	PRXMAX	Maximum input power	-10	-1	-	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID344	CI1	Co-channel interference, Wanted signal at -67 dBm and Interferer at FRX	-	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID345	CI2	Adjacent channel interference Wanted signal at -67 dBm and Interferer at FRX ±1 MHz	-	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID346	CI3	Adjacent channel interference Wanted signal at -67 dBm and Interferer at FRX ±2 MHz	-	-29	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID347	CI4	Adjacent channel interference Wanted signal at -67 dBm and Interferer at ≥FRX ±3 MHz	-	-39	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID348	CI5	Adjacent channel interference Wanted Signal at -67 dBm and Interferer at Image frequency ( $F_{IMAGE}$ )	-	-20	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID349	CI6	Adjacent channel interference Wanted signal at -67 dBm and Interferer at Image frequency ( $F_{IMAGE} \pm 1$ MHz)	-	-30	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID350	OBB1	Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 30–2000 MHz	-30	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID351	OBB2	Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 2003–2399 MHz	-35	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID352	OBB3	Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 2484–2997 MHz	-35	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID353	OBB4	Out-of-band blocking, Wanted signal a -67 dBm and Interferer at F = 3000–12750 MHz	-30	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)

Electrical specifications

**Table 54 Bluetooth® LE subsystem (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID354	IMD	Intermodulation performance Wanted signal at -64 dBm and 1-Mbps Bluetooth® LE, third, fourth, and fifth offset channel	-50	-	-	dBm	RF-PHY Specification (RCV-LE/CA/05/C)
SID355	RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	-	-	-57	dBm	100-kHz measurement bandwidth ETSI EN300 328 V1.8.1
SID356	RXSE2	Receiver spurious emission 1.0 GHz to 12.75 GHz	-	-	-47	dBm	1-MHz measurement bandwidth ETSI EN300 328 V1.8.1
<b>RF transmitter specifications</b>							
SID357	TXP, ACC	RF power accuracy	-	±1	-	dB	-
SID358	TXP, RANGE	RF power control range	-	20	-	dB	-
SID359	TXP, 0dBm	Output power, 0-dB Gain setting (PA7)	-	0	-	dBm	-
SID360	TXP, MAX	Output power, maximum power setting (PA10)	-	3	-	dBm	-
SID361	TXP, MIN	Output power, minimum power setting (PA1)	-	-18	-	dBm	-
SID362	F2AVG	Average frequency deviation for 10101010 pattern	185	-	-	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID363	F1AVG	Average frequency deviation for 11110000 pattern	225	250	275	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID364	EO	Eye opening = $\Delta F_{2AVG}/\Delta F_{1AVG}$	0.8	-	-		RF-PHY Specification (TRM-LE/CA/05/C)
SID365	FTX, ACC	Frequency accuracy	-150	-	150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID366	FTX, MAXDR	Maximum frequency drift	-50	-	50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID367	FTX, INITDR	Initial frequency drift	-20	-	20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID368	FTX, DR	Maximum drift rate	-20	-	20	kHz/ 50 $\mu$ s	RF-PHY Specification (TRM-LE/CA/06/C)
SID369	IBSE1	In-band spurious emission at 2-MHz offset	-	-	-20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)

Electrical specifications

**Table 54 Bluetooth® LE subsystem (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID370	IBSE2	In-band spurious emission at $\geq 3$ -MHz offset	-	-	-30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID371	TXSE1	Transmitter spurious emissions (average), <1.0 GHz	-	-	-55.5	dBm	FCC-15.247
SID372	TXSE2	Transmitter spurious emissions (average), >1.0 GHz	-	-	-41.5	dBm	FCC-15.247

**RF current specifications**

SID373	IRX	Receive current in normal mode	-	18.7	-	mA	-
SID373A	IRX_RF	Radio receive current in normal mode	-	16.4	-	mA	Measured at $V_{DDR}$
SID374	IRX, HIGHGAIN	Receive current in high-gain mode	-	21.5	-	mA	-
SID375	ITX, 3dBm	TX current at 3-dBm setting (PA10)	-	20	-	mA	-
SID376	ITX, 0dBm	TX current at 0-dBm setting (PA7)	-	16.5	-	mA	-
SID376A	ITX_RF, 0dBm	Radio TX current at 0 dBm setting (PA7)	-	15.6	-	mA	Measured at $V_{DDR}$
SID376B	ITX_RF, 0dBm	Radio TX current at 0 dBm excluding Balun loss	-	14.2	-	mA	Guaranteed by design simulation
SID377	ITX,-3dBm	TX current at -3-dBm setting (PA4)	-	15.5	-	mA	-
SID378	ITX,-6dBm	TX current at -6-dBm setting (PA3)	-	14.5	-	mA	-
SID379	ITX,-12dBm	TX current at -12-dBm setting (PA2)	-	13.2	-	mA	-
SID380	ITX,-18dBm	TX current at -18-dBm setting (PA1)	-	12.5	-	mA	-
SID380A	lavg_1sec, 0dBm	Average current at 1-second Bluetooth® LE connection interval	-	17.1	-	$\mu$ A	TXP: 0 dBm; $\pm 20$ -ppm master and slave clock accuracy.
SID380B	lavg_4sec, 0dBm	Average current at 4-second Bluetooth® LE connection interval	-	6.1	-	$\mu$ A	TXP: 0 dBm; $\pm 20$ -ppm master and slave clock accuracy.

**General RF specifications**

SID381	FREQ	RF operating frequency	2400	-	2482	MHz	-
SID382	CHBW	Channel spacing	-	2	-	MHz	-
SID383	DR	On-air data rate	-	1000	-	kbps	-
SID384	IDLE2TX	Bluetooth® LE.IDLE to Bluetooth® LE. TX transition time	-	120	140	$\mu$ s	-

Electrical specifications

**Table 54 Bluetooth® LE subsystem (continued)**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID385	IDLE2RX	Bluetooth® LE.IDLE to Bluetooth® LE. RX transition time	-	75	120	µs	-

**RSSI specifications**

SID386	RSSI, ACC	RSSI accuracy	-	±5	-	dB	-
SID387	RSSI, RES	RSSI resolution	-	1	-	dB	-
SID388	RSSI, PER	RSSI sample period	-	6	-	µs	-

**Table 55 ECO specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID389	F <sub>ECO</sub>	Crystal frequency	-	24	-	MHz	-
SID390	F <sub>TOL</sub>	Frequency tolerance	-50	-	50	ppm	-
SID391	ESR	Equivalent series resistance	-	-	60	Ω	-
SID392	PD	Drive level	-	-	100	µW	-
SID393	T <sub>START1</sub>	Startup time (Fast Charge on)	-	-	850	µs	-
SID394	T <sub>START2</sub>	Startup time (Fast Charge off)	-	-	3	ms	-
SID395	C <sub>L</sub>	Load capacitance	-	8	-	pF	-
SID396	C <sub>0</sub>	Shunt capacitance	-	1.1	-	pF	-
SID397	I <sub>ECO</sub>	Operating current	-	1400	-	µA	-

**Table 56 WCO specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID398	F <sub>WCO</sub>	Crystal frequency	-	32.768	-	kHz	-
SID399	FTOL	Frequency tolerance	-	50	-	ppm	-
SID400	ESR	Equivalent series resistance	-	50	-	kΩ	-
SID401	PD	Drive level	-	-	1	µW	-
SID402	T <sub>START</sub>	Startup time	-	-	500	ms	-
SID403	C <sub>L</sub>	Crystal load capacitance	6	-	12.5	pF	-
SID404	C <sub>0</sub>	Crystal shunt capacitance	-	1.35	-	pF	-
SID405	I <sub>WCO1</sub>	Operating current (High-Power mode)	-	-	8	µA	-
SID406	I <sub>WCO2</sub>	Operating current (Low-Power mode)	-	-	2.6	µA	-

## 6 Ordering information

The PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE part numbers and features are listed in [Table 57](#).

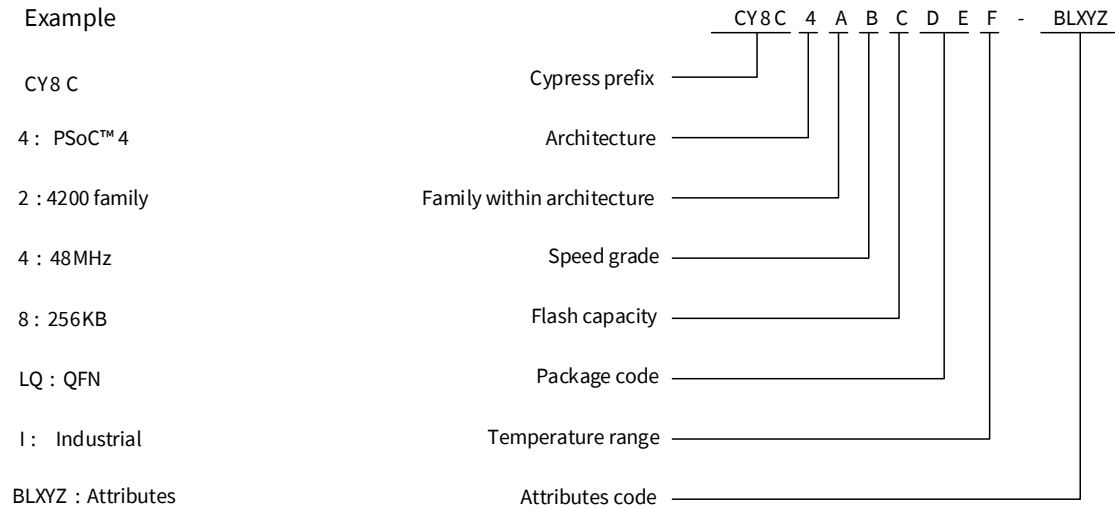
**Table 57 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE part numbers**

Product family	MPN	Max CPU speed (MHz)	Bluetooth® LE subsystem	Flash (KB)	SRAM (KB)	UDB	Opamp	CAPSENSE™	TMG (Gestures)	Direct LCD drive	12-bit SAR ADC	DMA	LP comparators	TCPWM blocks	SCB Blocks	GPIO	Package	Temperature range
PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE	CY8C4247LQI-BL473	48	4.1	128	16	4	4	-	-	-	1 Msps	-	2	4	2	36	QFN	85°C
	CY8C4247FNI-BL473	48	4.1	128	16	4	4	-	-	-	1 Msps	-	2	4	2	36	68-CSP	85°C
	CY8C4247LQI-BL453	48	4.1	128	16	4	4	1	-	-	1 Msps	-	2	4	2	36	QFN	85°C
	CY8C4247LQI-BL463	48	4.1	128	16	4	4	-	-	1	1 Msps	-	2	4	2	36	QFN	85°C
	CY8C4247LQI-BL483	48	4.1	128	16	4	4	1	-	1	1 Msps	-	2	4	2	36	QFN	85°C
	CY8C4247LQI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	-	2	4	2	36	QFN	85°C
	CY8C4247FNI-BL483	48	4.1	128	16	4	4	1	-	1	1 Msps	-	2	4	2	36	68-CSP	85°C
	CY8C4247FNI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	-	2	4	2	36	68-CSP	85°C
	CY8C4247FNQ-BL483	48	4.1	128	16	4	4	1	-	1	1 Msps	-	2	4	2	36	68-CSP	105°C
	CY8C4247LQQ-BL483	48	4.1	128	16	4	4	1	-	1	1 Msps	-	2	4	2	36	QFN	105°C
	CY8C4247FLI-BL493	48	4.1	128	16	4	4	1	1	1	1 Msps	-	2	4	2	36	Thin 68-CSP	85°C
	CY8C4248LQI-BL453	48	4.1	256	32	4	4	1	-	-	1 Msps	1	2	4	2	36	QFN	85°C
	CY8C4248LQI-BL483	48	4.1	256	32	4	4	1	-	1	1 Msps	1	2	4	2	36	QFN	85°C
	CY8C4248FNI-BL483	48	4.1	256	32	4	4	1	-	1	1 Msps	1	2	4	2	36	76-CSP	85°C
	CY8C4248LQI-BL543	48	4.2	256	32	-	2	-	-	-	1 Msps	1	-	4	2	36	QFN	85°C
	CY8C4248LQI-BL573	48	4.2	256	32	4	4	-	-	-	1 Msps	1	2	4	2	36	QFN	85°C
	CY8C4248FNI-BL573	48	4.2	256	32	4	4	-	-	-	1 Msps	1	2	4	2	36	76-CSP	85°C
	CY8C4248LQI-BL553	48	4.2	256	32	4	4	1	-	-	1 Msps	1	2	4	2	36	QFN	85°C
	CY8C4248FNI-BL553	48	4.2	256	32	4	4	1	-	-	1 Msps	1	2	4	2	36	76-CSP	85°C
	CY8C4248LQI-BL563	48	4.2	256	32	4	4	-	-	1	1 Msps	1	2	4	2	36	QFN	85°C
	CY8C4248LQI-BL583	48	4.2	256	32	4	4	1	-	1	1 Msps	1	2	4	2	36	QFN	85°C
	CY8C4248FNI-BL583	48	4.2	256	32	4	4	1	-	1	1 Msps	1	2	4	2	36	76-CSP	85°C
	CY8C4248LQQ-BL583	48	4.2	256	32	4	4	1	-	1	1 Msps	1	2	4	2	36	QFN	105°C
	CY8C4248LQI-BL593	48	4.2	256	32	4	4	1	1	1	1 Msps	1	2	4	2	36	QFN	85°C

PSoC™ 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, ..., 9, A,B, ..., Z) unless stated otherwise.

Ordering information

### 6.1 Ordering code definitions



The field values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC™ 4
A	Family within architecture	2	PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE family
B	CPU speed	4	48 MHz
C	Flash capacity	8, 7	256, 128 KB respectively
DE	Package code	FN	WLCSP
		LQ	QFN
		FL	Thin CSP
F	Temperature range	I	Industrial
BLXYZ	Attributes code	BL400-BL499	Bluetooth® 4.1 compliant
		BL500-BL599	Bluetooth® 4.2 compliant

Packaging

## 7 Packaging

**Table 58 Package characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
T <sub>A</sub>	Operating ambient temperature	–	–40	25.00	105	°C
T <sub>J</sub>	Operating junction temperature	–	–40	–	125	°C
T <sub>JA</sub>	Package θ <sub>JA</sub> (56-pin QFN)	–	–	16.9	–	°C/watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (56-pin QFN)	–	–	9.7	–	°C/watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (76-ball WLCSP)	–	–	20.1	–	°C/watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (76-ball WLCSP)	–	–	0.19	–	°C/watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (76-ball thin WLCSP)	–	–	20.9	–	°C/watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (76-ball thin WLCSP)	–	–	0.17	–	°C/watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (68-ball WLCSP)	–	–	16.6	–	°C/watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (68-ball WLCSP)	–	–	0.19	–	°C/watt
T <sub>JA</sub>	Package θ <sub>JA</sub> (68-ball thin WLCSP)	–	–	16.6	–	°C/watt
T <sub>JC</sub>	Package θ <sub>JC</sub> (68-ball thin WLCSP)	–	–	0.19	–	°C/watt

**Table 59 Solder reflow peak temperature**

Package	Maximum peak temperature	Maximum time at peak temperature
All packages	260°C	30 seconds

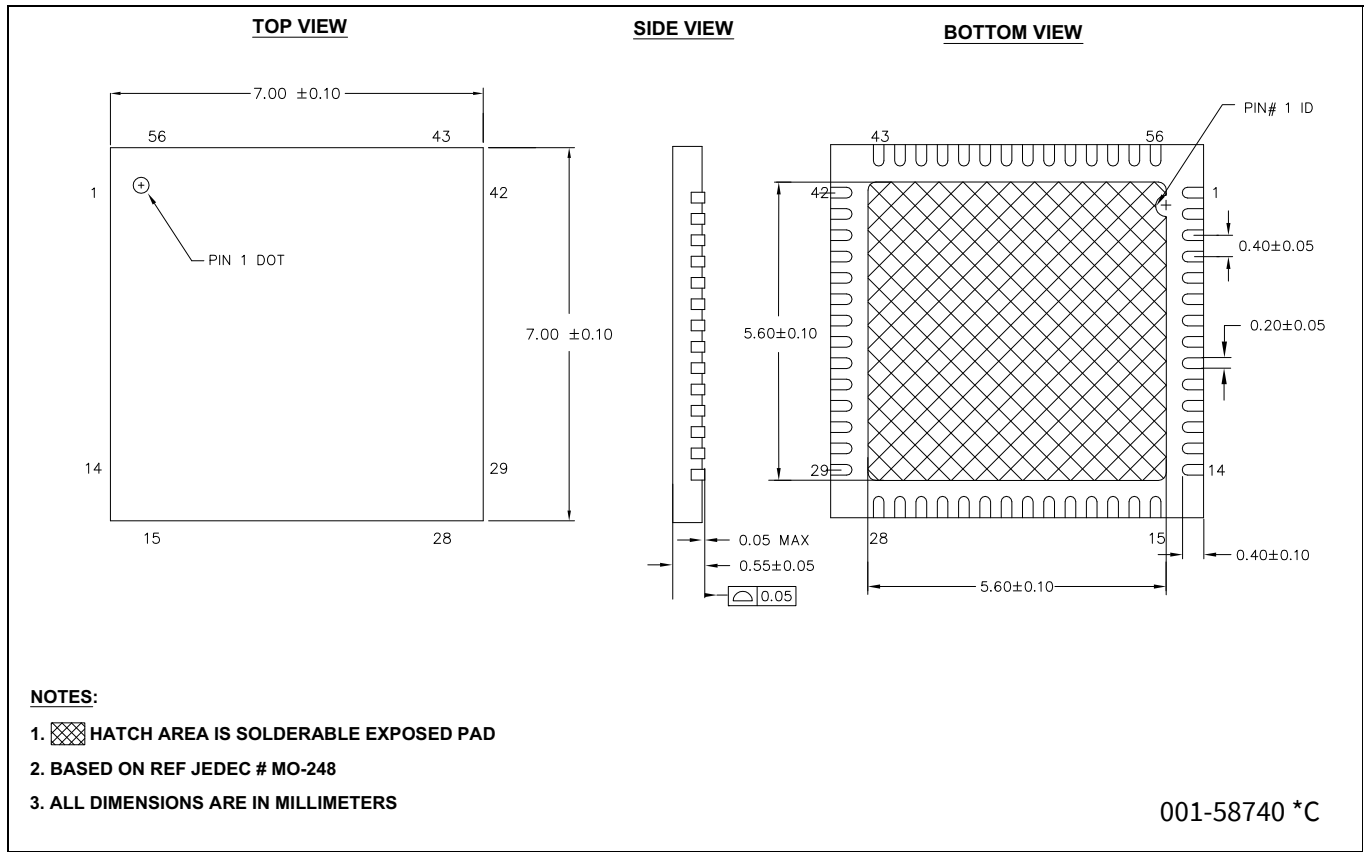
**Table 60 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
56-pin QFN	MSL 3
All WLCSP packages	MSL 1

**Table 61 Package details**

Spec ID	Package	Description
001-58740 Rev. *C	56-pin QFN	7.0 mm × 7.0 mm × 0.6 mm
001-96603 Rev. *B	76-ball WLCSP	4.04 mm × 3.87 mm × 0.55 mm
002-10658 Rev. **	76-ball thin WLCSP	4.04 mm × 3.87 mm × 0.4 mm
001-92343 Rev. *A	68-ball WLCSP	3.52 mm × 3.91 mm × 0.55 mm
001-99408 Rev. **	68-ball thin WLCSP	52 mm × 3.91 mm × 0.4 mm

Packaging



**Figure 7 56-pin QFN 7 × 7 × 0.6 mm**

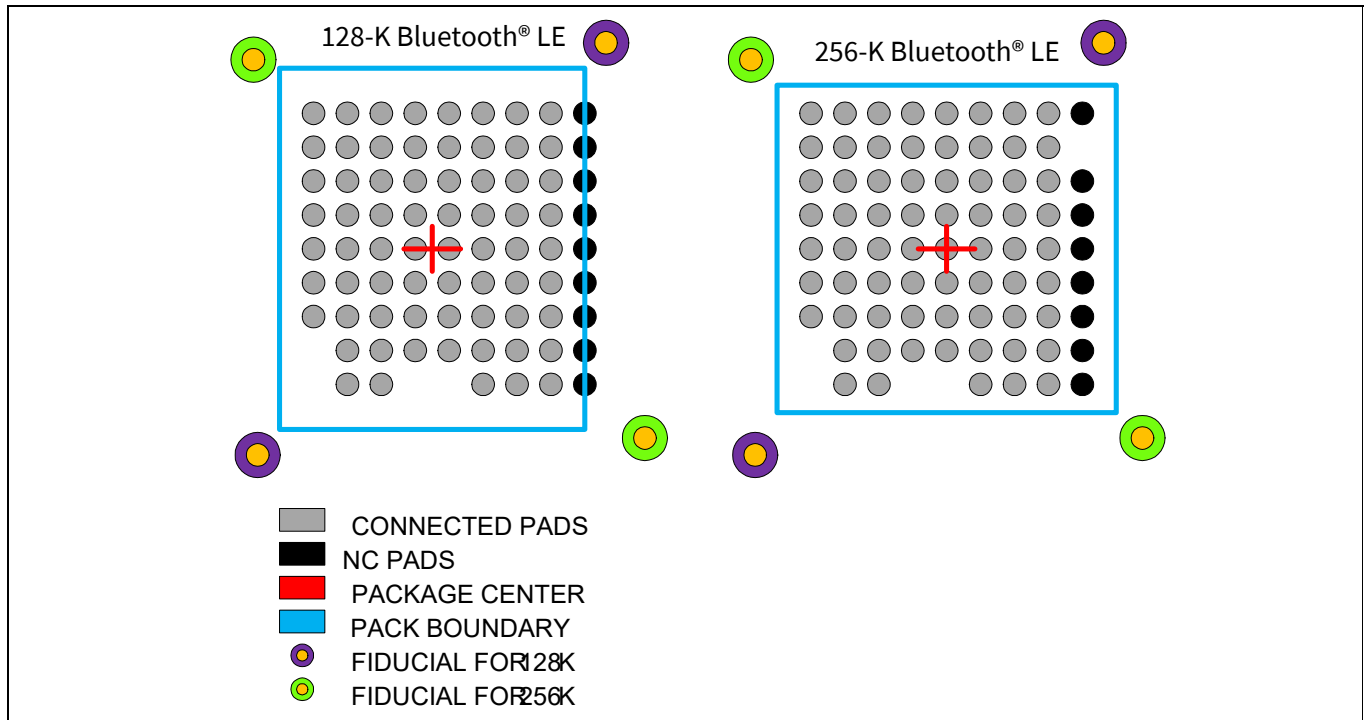
The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance.

## 7.1 WLCSP compatibility

The PSoC™ 4XXX-BLE family has products with 128 KB (16KB SRAM) and 256 KB (32KB SRAM) Flash. Package pin-outs and sizes are identical for the 56-pin QFN package but are different in one dimension for the 68-ball WLCSP.

The 256KB Flash product has an extra column of balls which are required for mechanical integrity purposes in the Chip-Scale package. With consideration for this difference, the land pattern on the PCB may be designed such that either product may be used with no change to the PCB design.

**Figure 8** shows the 128KB and 256 KB Flash CSP packages.

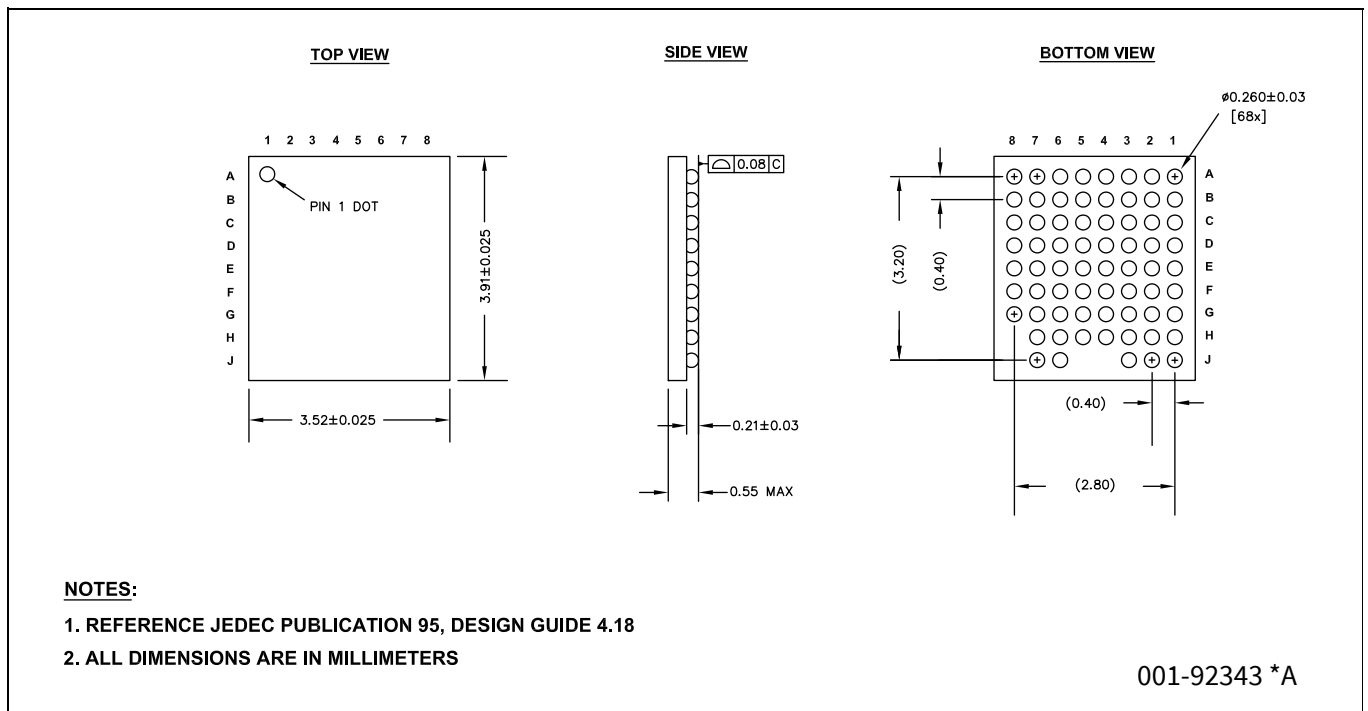


**Figure 8 128KB and 256 KB Flash CSP packages**

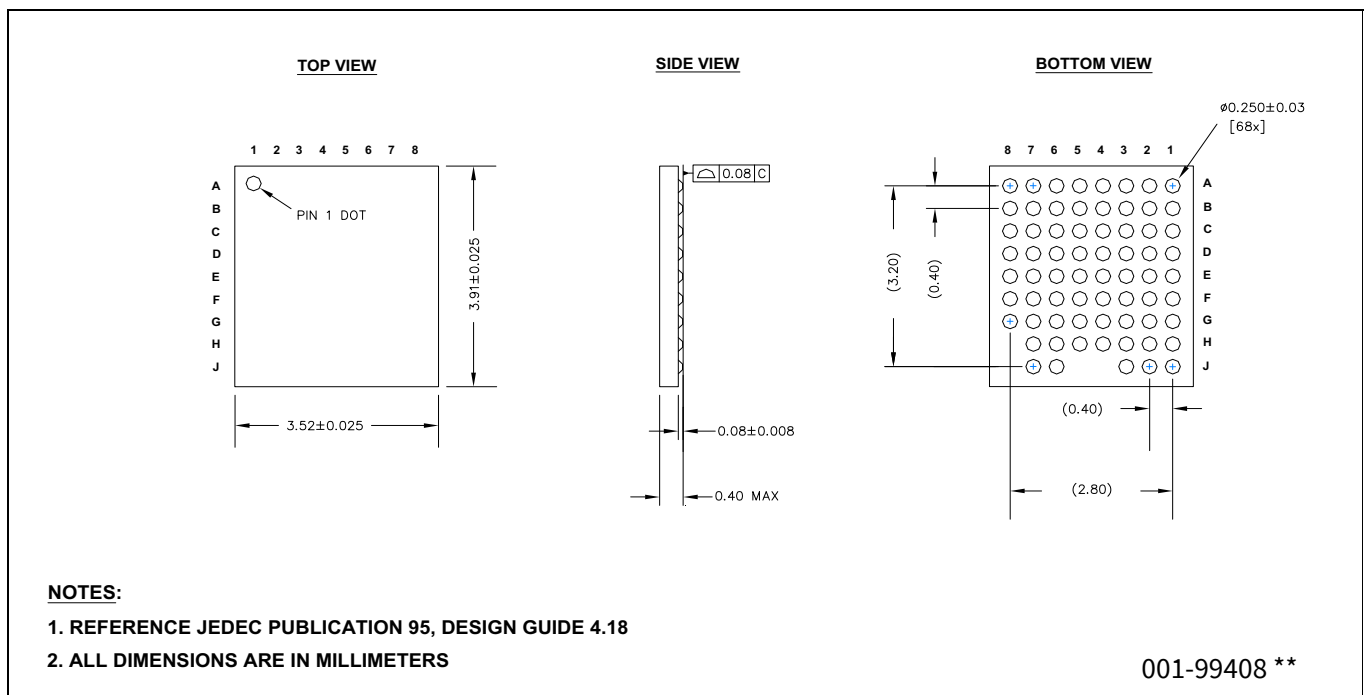
The rightmost column of (all NC, No Connect) balls in the 256K Bluetooth® LE WLCSP is for mechanical integrity purposes. The package is thus wider (3.2 mm versus 2.8 mm). All other dimensions are identical. Infineon will provide layout symbols for printed circuit board (PCB) layout.

The scheme in **Figure 8** is implemented to design the PCB for the 256K Bluetooth® LE package with the appropriate space requirements thus allowing use of either package at a later time without redesigning the PCB.

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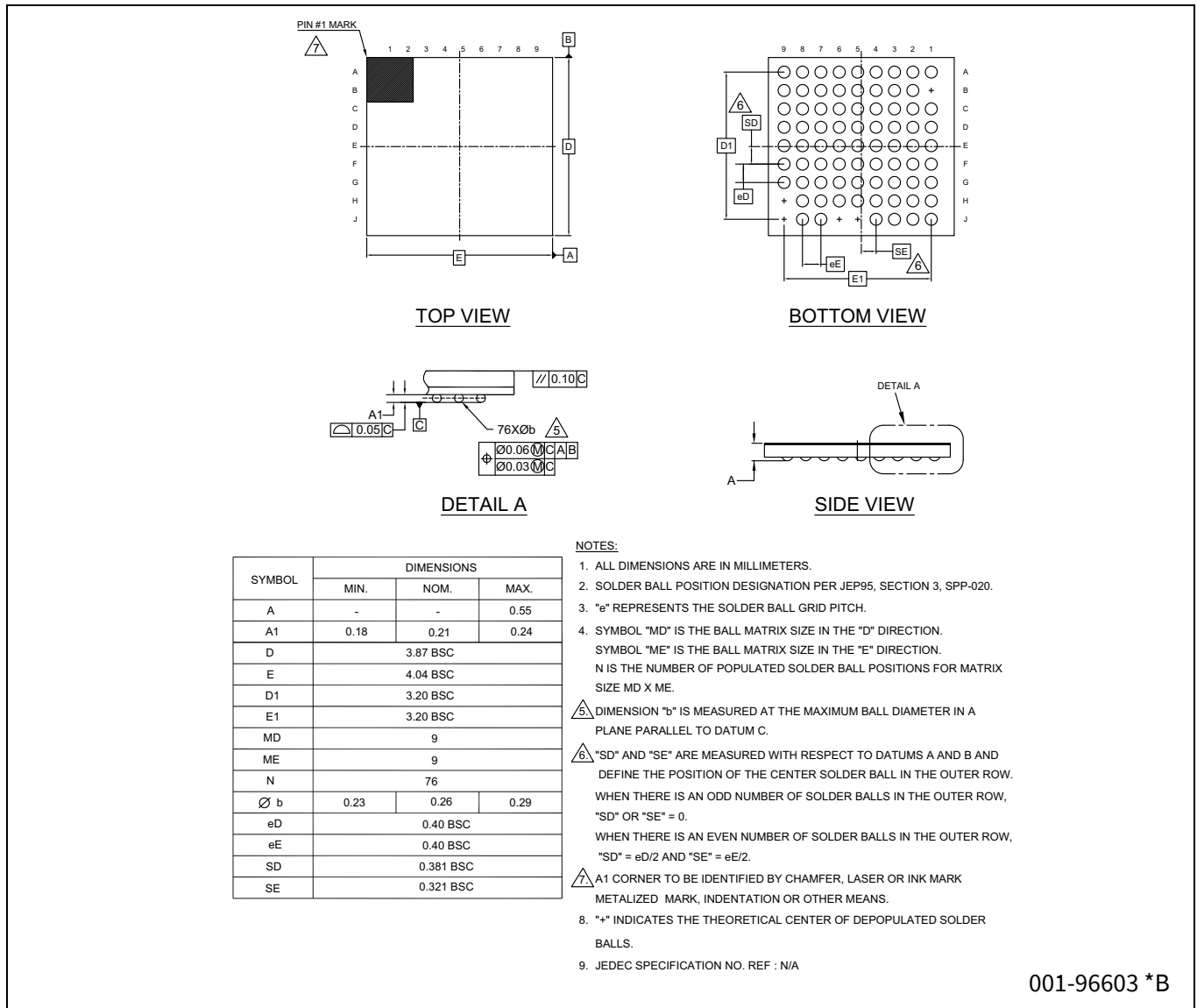


**Figure 9 68-ball WLCSP package outline**



**Figure 10 68-ball thin WLCSP**

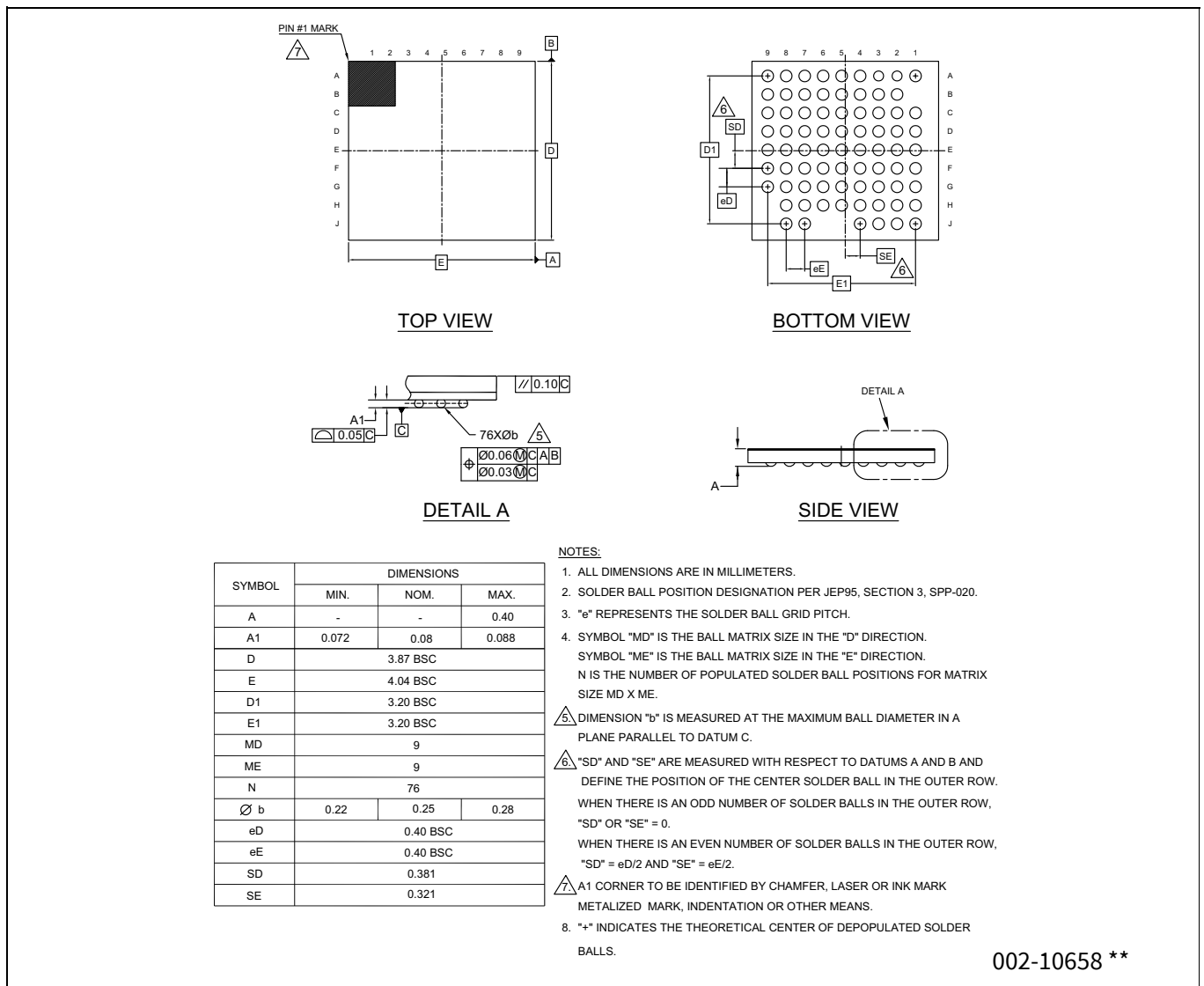
Packaging



001-96603 \*B

**Figure 11 76-ball WLCSP package outline**

Packaging



002-10658 \*\*

**Figure 12 76-ball thin WLCSP package outline**

## 8 Acronyms

**Table 62 Acronyms used in this document**

Acronym	Description
ABUS	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FET	field-effect transistor
FIR	finite impulse response, see also IIR

Acronyms

**Table 62** Acronyms used in this document *(continued)*

Acronym	Description
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HCI	host controller interface
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
Opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer

Acronyms

**Table 62** Acronyms used in this document *(continued)*

Acronym	Description
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC™	Programmable system on chip
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
STN	super twisted nematic
SWD	serial wire debug, a test protocol
SWV	single-wire viewer

Acronyms

**Table 62** Acronyms used in this document *(continued)*

<b>Acronym</b>	<b>Description</b>
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TN	twisted nematic
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## 9 Document conventions

### 9.1 Units of measure

**Table 63** Units of measure

Symbol	Units of measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

## Revision history

Document revision	Date	Description of changes
**	2018-02-22	New datasheet
*A	2021-06-16	Updated datasheet to IFX template. Changed title to “PSoC™ 4 CY8C42xx-BL MCU with AIROC™ Bluetooth® LE Family Datasheet”
*B	2023-03-29	Updated to the latest template Added <b>Table 2</b> for 68-ball WLCSP package Removed the following part numbers from <b>Table 57</b> : CY8C4248LQI-BL473, CY8C4248FLI-BL483, CY8C4248FNI-BL543, CY8C4248FNI-BL563, CY8C4248FLI-BL583, CY8C4248FNQ-BL583, and CY8C4248FNI-BL593

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