THE DATASHEET OF

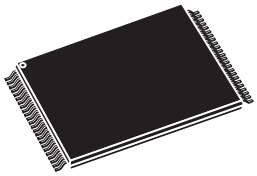
M29DW641F60ZE6E

M29DW641F

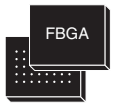
64 Mbit (4Mb x16, Multiple Bank, Page, Boot Block) 3V Supply Flash Memory

Features

- Supply voltage
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
  - $V_{PP}/\overline{WP}$=12V for Fast Program (optional)
- Asynchronous Page Read mode
  - Page Width 8 Words
  - Page Access 25, 30ns
  - Random Access: 60, 70ns
- Programming Time
  - 10µs per Word typical
  - 4 Words at-a-time Program
- Memory blocks
  - Quadruple Bank Memory Array: 8Mbit+24Mbit+24Mbit+8Mbit
  - Parameter Blocks (at Top and Bottom)
- Dual Operations
  - While Program or Erase in a group of banks (from 1 to 3), Read in any of the other banks
- Program/Erase Suspend and Resume modes
  - Read from any Block during Program Suspend
  - Read and Program another Block during Erase Suspend
- Unlock Bypass Program command
  - Faster Production/Batch Programming
- Common Flash Interface
  - 64 bit Security Code
- 100,000 Program/Erase cycles per block
- Low power consumption
  - Standby and Automatic Standby
- Extended Memory Block
  - Extra block used as security block or to store additional information



TSOP48 (N)
12 x 20mm



TFBGA48 (ZE)
6 x 8mm

- Hardware Block Protection
  - $V_{PP}/\overline{WP}$ Pin for fast program and write protect of the four outermost parameter blocks
- Software Block Protection
  - Standard Protection
  - Password Protection
- Electronic Signature
  - Manufacturer code: 0020h
  - Device code: 227Eh + 2203h + 2200h
- ECOPACK® packages

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1 Summary description

The M29DW641F is a 64 Mbit (4Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory default to its Read mode.

The device features an asymmetrical block architecture, with 16 parameter and 126 main blocks, divided into four Banks, A, B, C and D, providing Multiple Bank Operations. While programming or erasing is underway in one group of banks (from 1 to 3), reading can be conducted in any of the other banks. *Table 2* summarizes the bank architecture. Eight of the Parameter Blocks are at the top of the memory address space, and eight are at the bottom.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase Operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The Chip Enable, Output Enable and Write Enable signals control the Bus Operation of the memories. They allow simple connection to most microprocessors, often without additional logic.

The M29DW641F has one extra 128 Word block (Extended Block) that can be accessed using a dedicated command. The Extended Block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently, so it is possible to preserve valid data while old data is erased.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify). The software block protection features are available in 16 bit memory organization only:

- Hardware Protection:
  - The $V_{PP}/\overline{WP}$ provides a hardware protection of the four outermost parameter blocks (two at the top and two at the bottom of the address space).
  - The $\overline{RP}$ pin temporarily unprotects all the blocks previously protected using a High voltage Block Protection technique (see *Appendix D: High voltage Block Protection*).
- Software Protection
  - Standard Protection
  - Password Protection

The memory is offered in TSOP48 (12x20mm) and TFBGA48 (6x8mm, 0.8mm pitch) packages.

In order to meet environmental requirements, Numonyx offers the M29DW641F in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. The memory is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

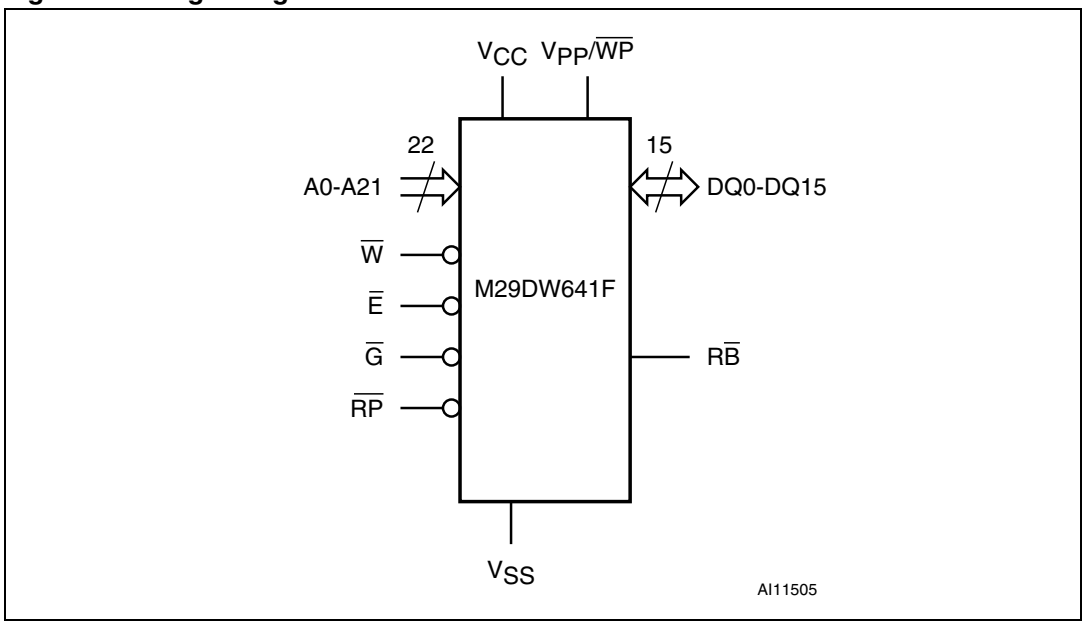


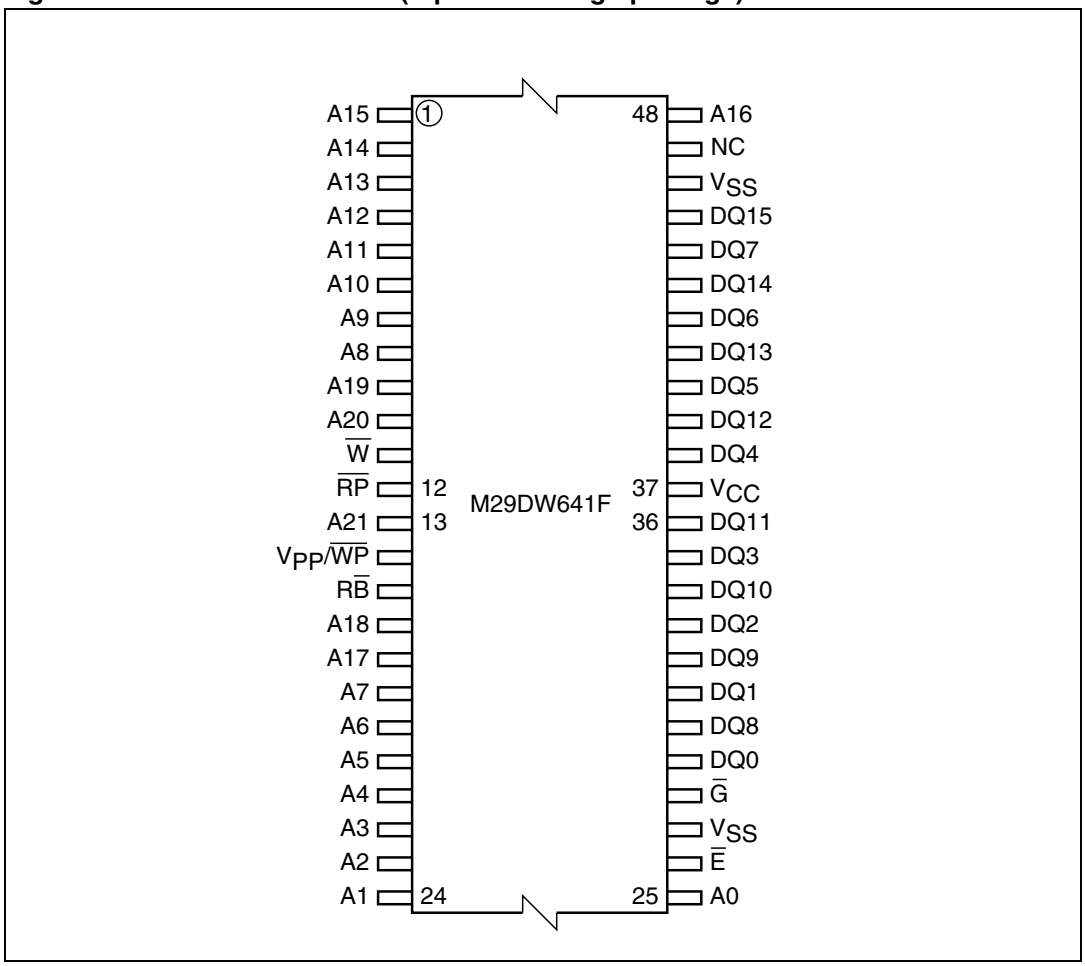
Table 1. Signal names

A0-A21	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
V_{CC}	Supply voltage
$V_{PP}/\overline{WP}$	V_{PP}/Write Protect
V_{SS}	Ground
NC	Not Connected Internally

Table 2. Bank architecture

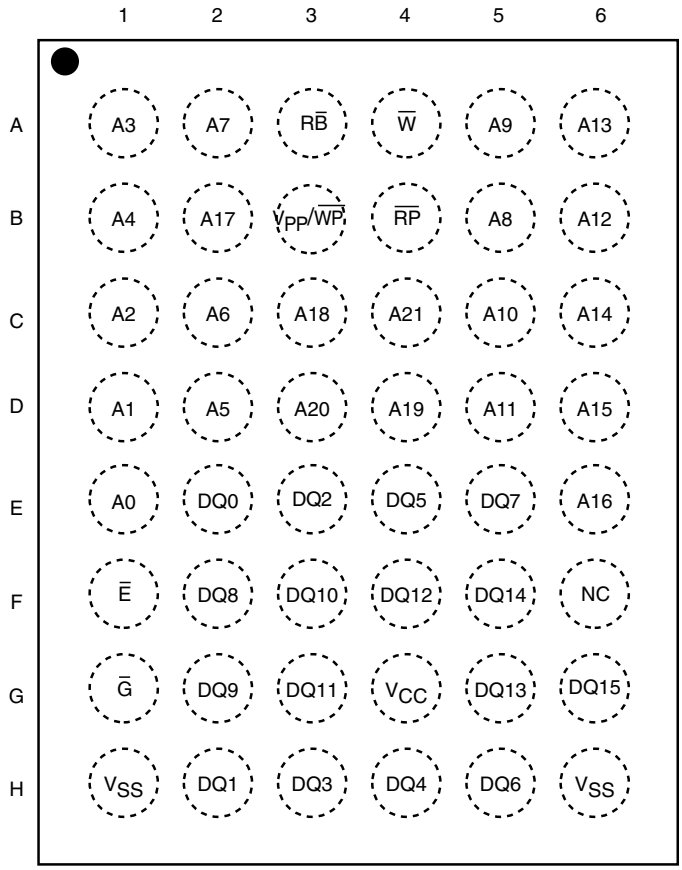
Bank	Bank size	Parameter Blocks		Main Blocks	
		No. of Blocks	Block size	No. of Blocks	Block size
A	8 Mbit	8	4 KWord	15	32 KWord
B	24 Mbit	—	—	48	32 KWord
C	24 Mbit	—	—	48	32 KWord
D	8 Mbit	8	4 KWord	15	32 KWord

Figure 2. TSOP connections (top view through package)



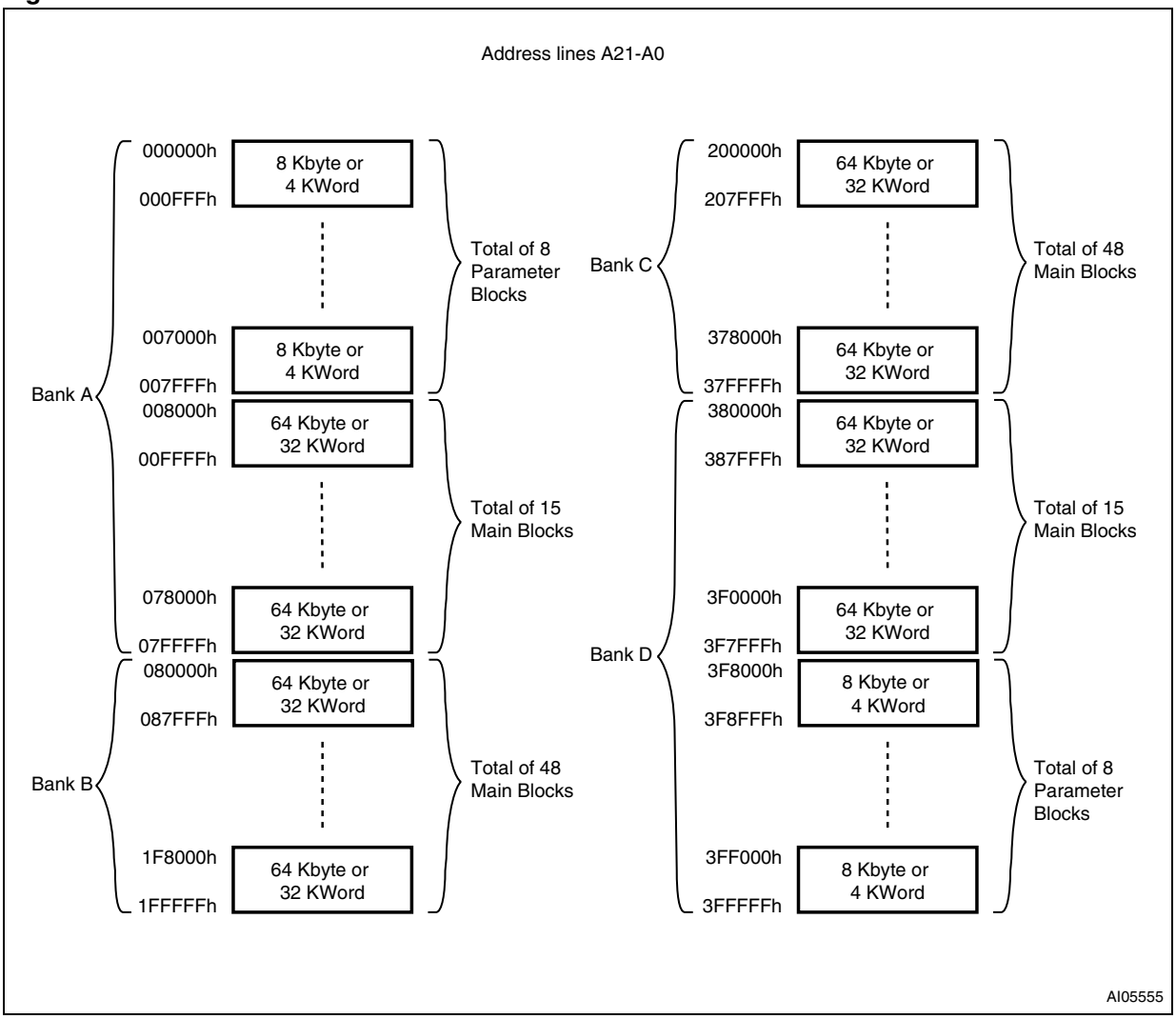
1. Balls are shorted together via the substrate but not connected to the die.

Figure 3. TFBGA48 connections (top view through package)



1. Balls are shorted together via the substrate but not connected to the die.

Figure 4. Block addresses



1. Also see *Appendix A*, *Table 28* for a full listing of the Block Addresses.

2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A21)

The Address Inputs select the cells in the memory array to access during Bus Read Operations. During Bus Write Operations they control the commands sent to the Command Interface of the internal state machine.

2.2 Data Inputs/Outputs (DQ0-DQ15)

The Data I/O output the data stored at the selected address during a Bus Read Operation. During Bus Write Operations they represent the commands sent to the Command Interface of the Program/Erase Controller.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write Operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.4 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, controls the Bus Read Operation of the memory.

2.5 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, controls the Bus Write Operation of the memory's Command Interface.

2.6 V_{PP}/Write Protect ($V_{PP}/\overline{WP}$)

The V_{PP}/Write Protect pin is both a power supply and a write protect pin. When V_{PP}/Write Protect is Low, V_{IL}, it is seen as a write protect pin protecting the four outermost parameter blocks (two at the top, and two at the bottom of the address space). Program and erase Operations in these blocks are ignored while V_{PP}/Write Protect is Low, even when $\overline{RP}$ is at V_{ID}.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection state of the four outermost parameter blocks. Program and Erase Operations can now modify the data in these blocks unless the blocks are protected using Block Protection.

Applying V_{PPH} to the $V_{PP}/\overline{WP}$ pin will temporarily unprotect any block previously protected (including the four outermost parameter blocks) using a High voltage Block Protection

technique (In-System or Programmer technique). See *Table 6: Hardware Protection* for details.

The V_{PP}/Write Protect pin must not be left floating or unconnected or the device may become unreliable. A 0.1µF capacitor should be connected between the V_{PP}/Write Protect pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

2.7 Reset/Block Temporary Unprotect ($\overline{RP}$)

The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all the blocks previously protected using a High voltage Block Protection technique (In-System or Programmer technique).

Note that if $V_{PP}/\overline{WP}$ is at V_{IL}, then the four outermost parameter blocks will remain protected even if $\overline{RP}$ is at V_{ID}.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}.

If $\overline{RP}$ is asserted during a Program or Erase Operation, the $R\overline{B}$ pin remains Low (busy), until the internal Reset Operation is completed, which requires a t_{PLYH} time (see *Figure 18: Reset/Block Temporary Unprotect during Program/Erase Operation AC waveforms*). The $R\overline{B}$ signal can be monitored by the system microprocessor to determine whether the Reset Operation is completed or not.

If $\overline{RP}$ is asserted when no Program or Erase Operation is ongoing, the $R\overline{B}$ pin remains high, V_{IH}. A t_{PHEL} or t_{PHGL} delay elapses before the Reset Operation is completed and $\overline{RP}$ returns to High, V_{IH}. After this delay, the memory is ready for Bus Read and Bus Write Operations.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect all the blocks previously protected using a High voltage Block Protection technique. Program and Erase Operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

See the Ready/Busy Output section, *Table 24: Reset/Block Temporary Unprotect AC characteristics* and *Figure 18: Reset/Block Temporary Unprotect during Program/Erase Operation AC waveforms* for more details.

2.8 Ready/Busy Output ($R\overline{B}$)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase Operation. During Program or Erase Operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write Operations cannot begin until Ready/Busy becomes high-impedance. See *Table 24* and *Figure 18: Reset/Block Temporary Unprotect during Program/Erase Operation AC waveforms*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.9 V_{CC} Supply voltage

V_{CC} provides the power supply for all operations (Read, Program and Erase).

The Command Interface is disabled when the V_{CC} Supply voltage is less than the Lockout voltage, V_{LKO}. This prevents Bus Write Operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Program and Erase Operations, I_{CC3}.

2.10 V_{SS} Ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins both of which must be connected to the system ground.

3 Bus Operations

There are five standard Bus Operations that control the device. These are Bus Read (Random and Page modes), Bus Write, Output Disable, Standby and Automatic Standby.

Dual Operations are possible in the M29DW641F, thanks to their multiple bank architecture. While programming or erasing in one banks, Read Operations are possible in any of the other banks. Write Operations are only allowed in one bank at a time.

See *Table 3: Bus Operations*, for a summary. Typically glitches of less than 5ns on Chip Enable, Write Enable, and Reset/Block Temporary Unprotect pins are ignored by the memory and do not affect Bus Operations.

3.1 Bus Read

Bus Read Operations read from the memory cells, or specific registers in the Command Interface. To speed up the Read Operation the memory array can be read in Page mode where data is internally read and stored in a page buffer. The Page has a size of 8 Words and is addressed by the address inputs A0-A2.

A valid Bus Read Operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see *Figure 11: Random Read AC waveforms*, *Figure 12: Page Read AC waveforms*, and *Table 20: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write Operations write to the Command Interface. A valid Bus Write Operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write Operation. See *Figure 13* and *Figure 14*, Write AC Waveforms, and *Table 21* and *Table 22*, Write AC Characteristics, for details of the timing requirements.

3.3 Output Disable

The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply current to the Standby Supply current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see *Table 19: DC characteristics*.

During program or Erase Operations the memory will continue to use the Program/Erase Supply current, I_{CC3}, for Program or Erase Operations until the operation completes.

3.5 Automatic Standby

If CMOS levels (V_{CC} ± 0.2V) are used to drive the bus and the bus is inactive for 300ns or more the memory enters Automatic Standby where the internal Supply current is reduced to the Standby Supply current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read Operation is in progress.

3.6 Special Bus Operations

Additional Bus Operations can be performed to read the Electronic Signature, verify the Protection status of the Extended Memory Block (second section), and apply or remove Block Protection. These Bus Operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

3.6.1 Read Electronic Signature

The memory has two codes, the Manufacturer code and the Device code used to identify the memory. These codes can accessed by performing Read Operations with control signals and addresses set as shown in *Table 3: Bus Operations*.

These codes can also be accessed by issuing an Auto Select command (see *Section 6: Command interface*, *Section 6.1.2: Auto Select command*).

3.6.2 Verify Extended Block Protection indicator

The Extended Block is divided in two sections of which one is Factory Locked and the second one is either Customer Lockable or Customer Locked.

The Protection status of the second section of the Extended Block (Customer Lockable or Customer Locked) can be accessed by reading the Extended Block Protection indicator. This is done by applying the signals listed in *Table 5: Block Protection*. The Protection status of the Extended Block is then output on bits DQ7 and DQ6 of the Data Input/Outputs. (see *Table 3: Bus Operations*).

The Protection status of the Extended Block can also be accessed by issuing an Auto Select command (see *Section 6: Command interface*, *Section 6.1.2: Auto Select command*).

3.6.3 Verify Block Protection status

The Protection status of a Block can be directly accessed by performing a Read Operation with control signals and addresses set as shown in *Table 5: Block Protection*.

If the Block is protected, then 0001h is output on Data Input/Outputs, otherwise 0000h is output.

3.6.4 Hardware Block Protect

The $V_{PP}/\overline{WP}$ pin can be used to protect the four outermost parameter blocks. When $V_{PP}/\overline{WP}$ is at V_{IL} the four outermost parameter blocks are protected and remain protected regardless of the Block Protection status or the Reset/Block Temporary Unprotect pin state.

3.6.5 Temporary Unprotection of High voltage Protected Blocks

The $\overline{RP}$ pin can be used to temporarily unprotect all the blocks previously protected using the In-System or the Programmer Protection technique (High voltage techniques).

Refer to *Section 2.7: Reset/Block Temporary Unprotect (RP)* in the *Section 2: Signal descriptions*.

Table 3. Bus Operations(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs	Data Inputs/Outputs
				A21-A0	DQ15-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.

Table 4. Read Electronic Signature(1)

Read cycle	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs									Data Inputs/Outputs
				A21-A10	A9	A8	A7-A6	A5-A4	A3	A2	A1	A0	DQ15-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0020h
Device code (Cycle 1)								V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (Cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	2203h
Device code (Cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	2200h (M29DW641F)

1. X = V_{IL} or V_{IH}.

Table 5. Block Protection(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address Inputs										Data Inputs/Outputs
						A21-A12	A11-A10	A9	A8	A7	A6	A5-A4	A3-A2	A1	A0	DQ15-DQ0
Verify Extended Block indicator (bits DQ6, DQ7)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	BA	X	V_{ID}	X	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	0080h (Customer Lockable) 00C0h (Customer Locked)(2)
Verify Block Protection status						BKA (3)				V_{IL}		V_{IL}			V_{IL}	0001h (protected) 0000h (unprotected)
Temporary Block Unprotect(4)	X	X	X	V_{ID}	X	Valid										Data Input

1. X = V_{IL} or V_{IH}.
2. This indicates the protection status of the second section of the Extended Block; the first section of the Extended Block being always Factory Locked.
3. BKA Bank Address, BA Any Address in the Block.
4. The $\overline{RP}$ pin unprotects all the blocks that have been previously protected using a High voltage Protection Technique.

4 Hardware Protection

The M29DW641F features hardware Protection/Unprotection. Refer to *Table 6* for details on Hardware Block Protection/unprotection using $V_{PP}/\overline{WP}$ and $\overline{RP}$ pins.

4.1 Write Protect

The $V_{PP}/\overline{WP}$ pin protects the four outermost parameter blocks (refer to *Section 2: Signal descriptions* for a detailed description of the signals).

4.2 Temporary Block Unprotect

When held at V_{ID}, the Reset/Block Temporary Unprotect pin, $\overline{RP}$, will temporarily unprotect all the blocks previously protected using a High voltage Block Protection technique.

Table 6. Hardware Protection(1)

$V_{PP}/\overline{WP}$	RP	Function
V_{IL}	V_{IH}	4 outermost parameter blocks protected from Program/Erase Operations
	V_{ID}	All blocks temporarily unprotected except the 4 outermost blocks
V_{IH} or V_{ID}	V_{ID}	All blocks temporarily unprotected
V_{PPH}	V_{IH} or V_{ID}	All blocks temporarily unprotected

1. The temporary unprotection is valid only for the blocks that have been protected using the High voltage Protection Technique (see *Appendix D: High voltage Block Protection*). The blocks protected using a Software Protection method (Standard or Password) do not follow this rules.

5 Software Protection

The M29DW641F has two different Software Protection modes: the Standard and Password Protection modes.

On first use all parts default to the Standard Protection mode and the customer is free to activate the Standard or the Password Protection mode.

The desired protection mode is activated by setting one of two one-time programmable bits, the Standard Protection mode Lock bit or the Password Protection mode Lock bit. Programming the Standard or the Password Protection mode Lock bit to '1' will permanently activate the Standard or the Password Protection mode, respectively. These two bits are one-time programmable and non-volatile, once the Protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected Protection mode. It is recommended to activate the desired Software Protection mode when first programming the device.

The device is shipped with all blocks unprotected. The Block Protection status can be read by issuing the Auto Select command (see *Table 7: Block Protection status*).

The Standard and Password Protection modes offer two levels of protection, a Block Lock/Unlock protection and a Non-volatile Protection.

For the four outermost parameter blocks, an even higher level of block protection can be achieved by locking the blocks using the Non-volatile Protection and then by holding the $V_{PP}/\overline{WP}$ pin Low.

5.1 Standard Protection mode

5.1.1 Block Lock/Unlock Protection

It is a flexible mechanism to protect/unprotect a block or a group of blocks from Program or Erase Operations.

A volatile Lock bit is assigned to each block or group of blocks. When the lock bit is set to '1' the associated block or group of blocks is protected from Program/Erase Operations, when the Lock bit is set to '0' the associated block or group of blocks is unprotected and can be programmed or erased.

The Lock bits can be set ('1') and cleared ('0') individually as often as required by issuing a Set Lock bit command and Clear Lock bit command, respectively.

After a Power-up or Hardware Reset, all the Lock bits are cleared to '0' (block unlocked). The device is shipped with all the Lock bits set to '0'.

5.1.2 Non-volatile Protection

A Non-Volatile Modify Protection bit is assigned to each block or group of blocks.

When a Non-Volatile Modify Protection bit is set to ‘1’, the associated block or group of blocks is protected, preventing any Program or Erase Operations in this block or group of blocks.

The Non-Volatile Modify Protection bits are set individually by issuing a Set Non-Volatile Modify Protection bit command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The Non-Volatile Modify Protection bits cannot be cleared individually, they can only be cleared all at the same time by issuing a Clear Non-Volatile Modify Protection bits command.

The device features a volatile Lock-Down bit which can be used to prevent changing the state of the Non-Volatile Modify Protection bits. When set to ‘1’, the Non-Volatile Modify Protection bits can no longer be modified; when set to ‘0’, the Non-Volatile Modify Protection bits can be set and reset using the Set Non-Volatile Modify Protection bit command and the Clear Non-Volatile Modify Protection bits command, respectively.

The Lock-Down bit is set by issuing the Set Lock-Down bit command. It is not cleared using a command, but through a hardware reset or a power-down/power-up sequence.

The part is shipped with the Non-Volatile Modify Protection bits set to ‘0’.

Locked blocks and Non-Volatile Locked blocks can co-exist in the same memory array.

Refer to *Table 7: Block Protection status* and *Figure 6: Software Protection scheme* for details on the block protection mechanism.

5.2 Password Protection mode

The Password Protection mode provides a more advanced level of software protection than the Standard Protection mode.

Prior to entering the Password Protection mode, it is necessary to set a password and to verify it (see *Section 6.3.5: Password Program command* and *Section 6.3.6: Password Verify command*). The Password Protection mode is then activated by programming the Password Protection mode Lock bit to ‘1’. This operation is not reversible and once the bit is programmed the device will permanently remain in the Password Protection mode.

The Password Protection mode uses the same protection mechanisms as the Standard Protection mode (Block Lock/Unlock, Non-volatile Protection).

5.2.1 Block Lock/Unlock Protection

The Block Lock/Unlock Protection operates exactly in the same way as in the Standard Protection mode.

5.2.2 Non-volatile Protection

The Non-Volatile Protection is more advanced in the Password Protection mode.

In this mode, the Lock-Down bit is non-volatile and cannot be cleared through a hardware reset or a power-down/power-up sequence.

The Lock-Down bit is cleared by issuing the Password Protection Unlock command along with the correct password.

Once the correct Password has been provided, the Lock-Down bit is cleared and the Non-Volatile Modify Protection bits can be set or reset using the appropriate commands (the Set Non-Volatile Modify Protection bit command or the Clear Non-Volatile Modify Protection bits command, respectively).

If the Password provided is not correct, the Lock-Down bit remains locked and the state of the Non-Volatile Modify Protection bits cannot be modified.

The Password is a 64-bit code located in the memory space. It must be programmed by the user prior to selecting the Password Protection mode. The Password is programmed by issuing a Password Program command and checked by issuing a Password Verify command. The Password should be unique for each part.

Once the device is in Password Protection mode, the Password can no longer be read or retrieved. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 7* and *Figure 6: Software Protection scheme* for details on the block protection scheme.

Table 7. Block Protection status

Volatile Lock bit	Non-volatile Modify Protection bit	Lock-Down bit	Block Protection status	Block Protection status	
0	0	0	0000h	Block Unprotected	Non-volatile Modify Protection bit can be modified(1)
0	0	1			Non-volatile Modify Protection bit cannot be modified(1)
0	1	0	0001h	Block Program/Erase Protected	Non-volatile Modify Protection bit can be modified(1)
1	0	0			
1	1	0			
0	1	1			Non-volatile Modify Protection bit cannot be modified(1)
1	0	1			
1	1	1			

1. The Lock bit can always be modified by issuing a Clear Lock bit command or by taking the device through a Power-up or Hardware Reset.

Figure 5. Block Protection state diagram

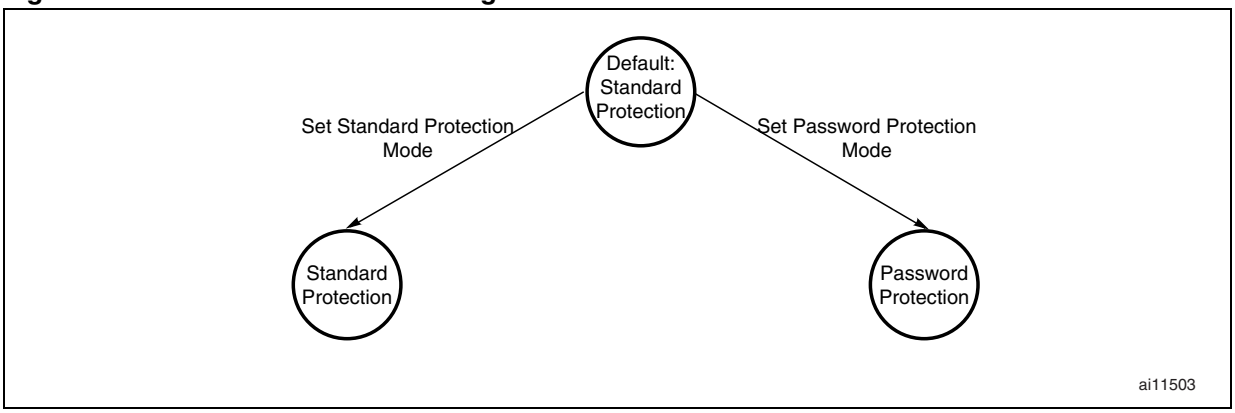
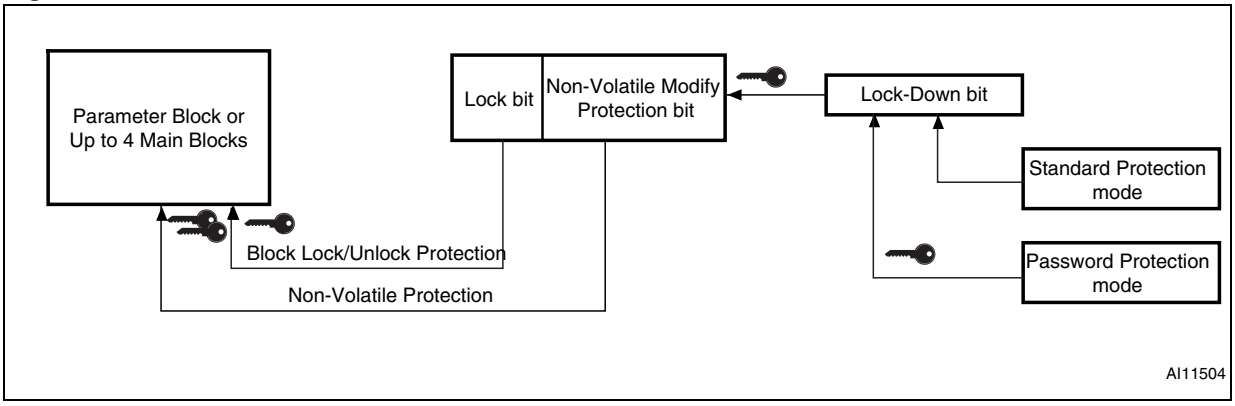


Figure 6. Software Protection scheme



6 Command interface

All Bus Write Operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write Operations. Failure to observe a valid sequence of Bus Write Operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

6.1 Standard commands

See *Table 8: Standard commands* for a summary of the Standard commands.

6.1.1 Read/Reset command

The Read/Reset command returns the memory to Read mode. It also resets the errors in the Status Register. Either one or three Bus Write Operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a Program or Erase Operation, to return the device to Read mode. If the Read/Reset command is issued during the time-out of a Block Erase Operation, the memory will take up to 10µs to abort. During the abort period no valid data can be read from the memory.

The Read/Reset command will not abort an Erase Operation when issued while in Erase Suspend.

6.1.2 Auto Select command

The Auto Select command is used to read the Manufacturer Code, the Device Code, the Protection status of each block (Block Protection status) and the Extended Block Protection indicator. It can be addressed to either Bank.

Three consecutive Bus Write Operations are required to issue the Auto Select command. Once the Auto Select command is issued, Bus Read Operations to specific addresses output the Manufacturer Code, the Device Code, the Extended Block Protection indicator and a Block Protection status (see *Table 8: Standard commands* in relation with *Table 4* and *Table 5*). The memory remains in Auto Select mode until a Read/Reset or CFI Query command is issued.

6.1.3 Read CFI Query command

The Read CFI Query command is used to put the addressed bank in Read CFI Query mode. Once in Read CFI Query mode, Bus Read Operations to the same bank will output data from the Common Flash Interface (CFI) Memory Area. If the Read Operations are to a different bank from the one specified in the command then the Read Operations will output the contents of the memory array and not the CFI data.

One Bus Write cycle is required to issue the Read CFI Query command. Care must be taken to issue the command to one of the banks (A21-A19) along with the address shown in *Table 3* Once the command is issued subsequent Bus Read Operations in the same bank (A21-A19) to the addresses shown in *Appendix B* (A7-A0), will read from the Common Flash Interface Memory Area.

This command is valid only when the device is in the Read Array or Auto Select mode. To enter Read CFI query mode from Auto Select mode, the Read CFI Query command must be issued to the same bank address as the Auto Select command, otherwise the device will not enter Read CFI Query mode.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Auto Select mode). A second Read/Reset command is required to put the device in Read Array mode from Auto Select mode.

See *Appendix B*, *Table 29*, *Table 30*, *Table 31*, *Table 32*, *Table 33* and *Table 34* for details on the information contained in the Common Flash Interface (CFI) memory area.

6.1.4 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write Operations are required to issue the Chip Erase command and start the Program/Erase Controller.

If any blocks are protected, then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase Operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Erase Operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 12*. All Bus Read Operations during the Chip Erase Operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase Operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Chip Erase command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

6.1.5 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks in one or more Banks. It sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

Six Bus Write Operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write Operation using the address of the additional block. The Block Erase Operation starts the Program/Erase Controller after a time-out period of 50µs after the last Bus Write Operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. After the sixth Bus Write Operation a Bus Read Operation within the same Bank will output the Status Register. See the Status Register section for details on how to identify if the Program/Erase Controller has started the Block Erase Operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase Operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase Operation the memory will ignore all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the 50µs time-out period. Typical block erase times are given in *Table 12*.

After the Erase Operation has started all Bus Read Operations to the Banks being erased will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase Operation has completed the memory will return to the Read mode, unless an error has occurred.

When an error occurs, Bus Read Operations to the Banks where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

6.1.6 Erase Suspend command

The Erase Suspend command may be used to temporarily suspend a Block or multiple Block Erase Operation. One Bus Write Operation specifying the Bank Address of one of the Blocks being erased is required to issue the command. Issuing the Erase Suspend command returns the whole device to Read mode.

The Program/Erase Controller will suspend within the Erase Suspend Latency time (see *Table 12* for value) of the Erase Suspend command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program Operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and

no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

During Erase Suspend a Bus Read Operation to the Extended Block will output the Extended Block data. Once in the Extended Block mode, the Exit Extended Block command must be issued before the Erase Operation can be resumed.

6.1.7 Erase Resume command

The Erase Resume command is used to restart the Program/Erase Controller after an Erase Suspend. The command must include the Bank Address of the Erase-Suspended Bank, otherwise the Program/Erase Controller is not restarted.

The device must be in Read Array mode before the Resume command will be accepted. An Erase can be suspended and resumed more than once.

6.1.8 Program Suspend command

The Program Suspend command allows the system to interrupt a Program Operation so that data can be read from any block. When the Program Suspend command is issued during a Program Operation, the device suspends the Program Operation within the Program Suspend Latency time (see *Table 12* for value) and updates the Status Register bits. The Bank Addresses of the Block being programmed must be specified in the Program Suspend command.

After the Program Operation has been suspended, the system can read array data from any address. However, data read from Program-Suspended addresses is not valid.

The Program Suspend command may also be issued during a Program Operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Extended Block area (One-time Program area), the user must use the proper command sequences to enter and exit this region.

The system may also issue the Auto Select command sequence when the device is in the Program Suspend mode. The system can read as many Auto Select codes as required. When the device exits the Auto Select mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Auto Select command sequence for more information.

6.1.9 Program Resume command

After the Program Resume command is issued, the device reverts to programming. The controller can determine the status of the Program Operation using the DQ7 or DQ6 status bits, just as in the standard Program Operation. See Write Operation status for more information.

The system must write the Program Resume command, specifying the Bank addresses of the Program-Suspended Block, to exit the Program Suspend mode and to continue the Programming Operation.

Further issuing of the Resume command is ignored. Another Program Suspend command can be written after the device has resumed programming.

6.1.10 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write Operations, the final Write Operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

Programming can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.8: Program Suspend command* and *Section 6.1.9: Program Resume command*). If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

After programming has started, Bus Read Operations in the Bank being programmed output the Status Register content, while Bus Read Operations to the other Bank output the contents of the memory array. See the section on the Status Register for more details. Typical program times are given in *Table 12*.

After the Program Operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read Operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

6.1.11 Verify command

The Verify command is used to check if a block is blank or in other words, if it has been successfully erased and all its bits set to ’1’. It reads the value of the Error bit DQ5. If the Error bit is set to ’1’, it indicates that the operation failed.

Three cycles are required to issue a Verify command:

1. The command starts with two unlock cycles.
2. The third Bus Write cycle sets up the Verify command code along with the address of the block to be checked.

Table 8. Standard commands

Command		Length	Bus Operations[1][2]											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0										
		3	555	AA	2AA	55	X	F0						
Auto Select	Manufacturer code	3	555	AA	2AA	55	(BKA) 555	90	(3)	(3)				
	Device code													
	Extended Block Protection indicator													
	Block Protection status													
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Verify		3	555	AA	2AA	55	BA	BC						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase		6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase/Program Suspend		1	BKA	B0										
Erase/Program Resume		1	BKA	30										
Read CFI Query		1	(BKA) 555	98										

1. Grey cells represent Read cycles. The other cells are Write cycles.
2. X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block, BKA Bank Address. All values in the table are in hexadecimal.
3. The Auto Select addresses and data are given in *Table 4: Read Electronic Signature*, and *Table 5: Block Protection*, except for A9 that is 'Don't Care'.

6.2 Fast Program commands

The M29DW641F offers a set of Fast Program commands to improve the programming throughput:

- Double and Quadruple Word, Program
- Unlock Bypass

When V_{PPH} is applied to the V_{PP}/Write Protect pin the memory automatically enters the Fast Program mode. The user can then choose to issue any of the Fast Program commands. Care must be taken because applying a V_{PPH} to the $V_{PP}/\overline{WP}$ pin will temporarily unprotect any protected block.

Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend. After programming has started, Bus Read Operations in the Bank being programmed output the Status Register content, while Bus Read Operations to the other Bank output the contents of the memory array. Fast Program commands can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.8: Program Suspend command* and *Section 6.1.9: Program Resume command*).

After the Fast Program command has completed, the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read Operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

Typical Program times are given in *Table 12: Program, Erase Times and Program, Erase Endurance cycles*. See either *Table 9: Fast Program commands*, for a summary of the Fast Program commands.

6.2.1 Double Word Program command

This is used to write two adjacent Words simultaneously. The addresses of the two Words must differ only in A0. Three bus write cycles are necessary to issue the command:

1. The first bus cycle sets up the command.
2. The second bus cycle latches the Address and the Data of the first Word to be written.
3. The third bus cycle latches the Address and the Data of the second Word to be written and starts the Program/Erase Controller.

6.2.2 Quadruple Word Program command

This is used to write four adjacent Words simultaneously. The addresses of the four Words must differ only in A1 and A0. Five bus write cycles are necessary to issue the command:

1. The first bus cycle sets up the command.
2. The second bus cycle latches the Address and the Data of the first Word to be written.
3. The third bus cycle latches the Address and the Data of the second Word to be written.
4. The fourth bus cycle latches the Address and the Data of the third Word to be written.
5. The fifth bus cycle latches the Address and the Data of the fourth Word to be written and starts the Program/Erase Controller.

6.2.3 Unlock Bypass command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three Bus Write Operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the bank enters Unlock Bypass mode. When in Unlock Bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. The Unlock Bypass Program command can then be issued to program addresses within the bank, or the Unlock Bypass Reset command can be issued to return the bank to Read mode. In Unlock Bypass mode the memory can be read as if in Read mode.

6.2.4 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write Operations, the final Write Operation latches the address and data and starts the Program/Erase Controller.

The Program Operation using the Unlock Bypass Program command behaves identically to the Program Operation using the Program command. The operation cannot be aborted, a Bus Read Operation to the Bank where the command was issued outputs the Status Register. See the Program command for details on the behavior.

6.2.5 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass mode. Two Bus Write Operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass mode.

Table 9. Fast Program commands

Command[1]	Length	Bus Write Operations[2]											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Double Word Program	3	555	50	PA0	PD0	PA1	PD1						
Quadruple Word Program	5	555	56	PA0	PD0	PA1	PD1	PA2	PD2	PA3	PD3		
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								

1. The sequence consisting in 555 AA 2AA 55 X 25 is reserved and must not be issued.
2. X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block, BKA Bank Address, WBL Write Buffer Location. All values in the table are in hexadecimal.

6.3 Block Protection commands

Blocks or groups of blocks can be protected against accidental program, Erase or Read Operations. The Protection Groups are shown in *Appendix A*, *Table 28: Block Addresses*. The device block protection scheme is shown in *Figure 6: Software Protection scheme* and *Figure 5: Block Protection state diagram*. See *Table 10: Block Protection commands*, for a summary of the Block Protection commands.

Only the commands related to the Extended Block Protection are available in both 8 bit and 16 bit memory configuration. The other block protection commands are available in 16-bit configuration only.

6.3.1 Enter Extended Block command

The M29DW641F has one extra 128-Word block (Extended Block) that can only be accessed using the Enter Extended Block command.

Three Bus Write cycles are required to issue the Extended Block command. Once the command has been issued the device enters Extended Block mode where all Bus Read or Program Operations to the Extended Block Addresses (see *Table 28: Block Addresses*).

The Extended Block cannot be erased, and can be treated as one-time programmable (OTP) memory. In Extended Block mode only array cell locations (Bank A) with the same addresses as the Extended Block are not accessible. In Extended Block mode Dual Operations are allowed and the Extended Block physically belongs to Bank A.

In Extended Block mode, Erase, Chip Erase, Erase Suspend and Erase resume commands are not allowed.

To exit from the Extended Block mode the Exit Extended Block command must be issued.

The Extended Block can be protected by setting the Extended Block Protection bit to ‘1’; however once protected the protection cannot be undone.

6.3.2 Exit Extended Block command

The Exit Extended Block command is used to exit from the Extended Block mode and return the device to Read mode. Four Bus Write Operations are required to issue the command.

6.3.3 Set Extended Block Protection bit command

The Set Extended Block Protection bit command programs the Extended Block Protection bit to ‘1’ thus preventing the second section of the Extended Block from being programmed.

A Read/Reset command must be issued to abort a Set Extended Block Protection bit command.

Six successive steps are required to issue the Set Extended Block Protection bit command.

1. The command starts with two unlock cycles.
2. The third Bus Write cycle sets up the Set Extended Block Protection bit command.
3. The last three cycles verify the value programmed at the Extended Block Protection bit address: if bit DQ0 of Data Inputs/Outputs is set to ’1’, it indicates that the Extended Block Protection bit has been successfully programmed. If DQ0 is ‘0’, the Set Extended Block Protection bit command must be issued and verified again.

6.3.4 Verify Extended Block Protection bit command

The Verify Extended Block Protection bit command reads the status of the Extended Block Protection bit on bit DQ0 of the Data Inputs/Outputs. If DQ0 is ‘1’, the second section of the Extended Block is protected from Program Operations.

6.3.5 Password Program command

The Password Program command is used to program the 64-bit Password used in Password Protection mode.

Four cycles are required to program the Password:

1. The first two cycles are unlock cycles.
2. The third cycle issues the Password Program command.
3. The fourth cycle inputs the 16-bit data required to program the Password.

To program the 64-bit Password, the complete command sequence must be entered four times at four consecutive addresses selected by A1 to A0.

Read Operations can be used to read the Status Register during a Password Program Operation. All other operations are forbidden.

The Password can be checked by issuing a Password Verify command.

Once Password Program Operation has completed, a Read/ Reset command must be issued to return the device to Read mode. The Password Protection mode can then be selected.

By default, all Password bits are set to ‘1’.

6.3.6 Password Verify command

The Password Verify command is used to verify the Password used in Password Protection mode.

To verify the 64-bit Password, the complete command sequence must be entered four times at four consecutive addresses selected by A1 to A0.

If this command is issued while the device is in Password Protection mode, it outputs ‘FFh’ and all Inputs/Outputs are high impedance.

The Password is output regardless of the bank address.

The user must issue a Read/reset command to return the device to Read mode.

Dual Operations are not allowed during a Password Verify Operation.

6.3.7 Password Protection Unlock command

The Password Protection Unlock command is used to clear the Lock-Down bit in order to unprotect all Non-Volatile Modify Protection bits when the device is in Password Protection mode. The Password Protection Unlock command must be issued along with the correct Password.

The complete command sequence must be entered for each 16 bits of the Password.

There must be a 2µs delay between successive Password Protection Unlock commands in order to prevent hackers from cracking the Password by trying all possible 64-bit combinations. If this delay is not respected, the latest command will be ignored.

6.3.8 Set Password Protection mode command

The Set Password Protection mode command puts the device in Password Protection mode by programming the Password Protection mode Lock bit to '1'. This command can be issued either with the Reset/Block Temporary Unprotect pin, $\overline{RP}$, at V_{ID} or at V_{IH}.

Six cycles are required to issue a Set Password Protection mode command:

1. The first two cycles are unlock cycles.
2. The third cycle issues the command.
3. The fourth and fifth cycles select the address (see *Table 11: Protection command addresses*).
4. The last cycle verifies if the operation has been successful. If DQ0 is set to '1', the device has successfully entered the Password Protection mode. If DQ0 is '0', the operation has failed and the command must be re-issued.

There must be a 100µs delay between the fourth and fifth cycles.

Once the Password Protection mode is activated the device will permanently remain in this mode.

6.3.9 Verify Password Protection mode command

The Verify Password Protection mode command reads the status of the Password Protection mode Lock bit. If it is '1', the device is in Password Protection mode.

6.3.10 Set Standard Protection mode command

The Set Standard Protection mode command puts the device in Standard Protection mode by programming the Standard Protection mode Lock bit to '1'.

Six cycles are required to issue the Standard Protection mode command:

1. The first two cycles are unlock cycles.
2. The third cycle issues the program command.
3. The fourth and fifth cycles select the address (see *Table 11: Protection command addresses*).
4. The last cycle verifies if the operation has been successful. If DQ0 is set to '1', the Standard Protection mode has been successfully activated. If DQ0 is '0', the operation has failed and the command must be re-issued.

There must be a 100µs delay between the fourth and fifth cycles. Once the Standard Protection mode is activated the device will permanently remain in this mode.

6.3.11 Verify Standard Protection mode command

The Verify Standard Protection mode command reads the status of the Standard Protection mode Lock bit. If it is ‘1’, the device is in Standard Protection mode.

6.3.12 Set Non-Volatile Modify Protection bit command

A block or group of blocks can be protected from program or erase by issuing a Set Non-Volatile Modify Protection bit command along with the block address. This command sets the Non-Volatile Modify Protection bit to ‘1’ for a given block or group of blocks.

Six cycles are required to issue the command:

1. The first two cycles are unlock cycles.
2. The third cycle issues the program command.
3. The fourth and fifth cycles select the address (see *Table 11: Protection command addresses*).
4. The last cycle verifies if the operation has been successful. If DQ0 is set to ’1’, the Non-Volatile Modify Protection bit has been successfully programmed. If DQ0 is ‘0’, the operation has failed and the command must be re-issued.

There must be a 100µs delay between the fourth and fifth cycles.

The Non-Volatile Modify Protection bits are erased simultaneously by issuing a Clear Non-Volatile Modify Protection bits command except if the Lock-Down bit is set to ‘1’.

The Non-Volatile Modify Protection bits can be set a maximum of 100 times.

6.3.13 Verify Non-volatile Modify Protection bit command

The status of a Non-Volatile Modify Protection bit for a given block or group of blocks can be read by issuing a Verify Non-Volatile Modify Protection bit command along with the block address.

6.3.14 Clear Non-volatile Modify Protection bit command

This command is used to clear all Non-Volatile Modify Protection bits. No specific block address is required. If the Lock-Down bit is set to ‘1’, the command will fail.

Six cycles are required to issue a Clear Non-Volatile Modify Protection bits command:

1. The first two cycles are unlock cycles.
2. The third cycle issues the command.
3. The last three cycles verify if the operation has been successful. If DQ0 is set to ’1’, all Non-Volatile Modify Protection bits have been successfully cleared. If DQ0 is ‘0’, the operation has failed and the command must be re-issued.

There must be a 12ms delay between the fourth and fifth cycles.

6.3.15 Set Lock bit command

The Set Lock bit command individually sets the Lock bit to ‘1’ for a given block or group of blocks.

If the Non-Volatile Lock bit for the same block or group of blocks is set, the block is locked regardless of the value of the Lock bit. (see *Table 7: Block Protection status*).

6.3.16 Clear Lock bit command

The Clear Lock bit command individually clears (sets to ‘0’) the Lock bit for a given block or group of blocks.

If the Non-Volatile Lock bit for the same block or group of blocks is set, the block or group of blocks remains locked (see *Table 7: Block Protection status*).

6.3.17 Verify Lock bit command

The status of a Lock bit for a given block can be read by issuing a Verify Lock bit command along with the block address.

6.3.18 Set Lock-Down bit command

This command is used to set the Lock-Down bit to ‘1’ thus protecting the Non-Volatile Modify Protection bits from program and erase.

There is no Unprotect Lock-Down bit command.

6.3.19 Verify Lock-Down bit command

This command is used to read the status of the Lock-Down bit. The status is output on bit DQ1. If DQ1 is ‘1’, all the Non-Volatile Modify Protection bits are protected from Program or Erase Operations.

Table 10. Block Protection commands

Command	Length	Bus Write Operations[1][2][3]													
		1st		2nd		3rd		4th		5th		6th		7th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Set Extended Block Protection bit[4]	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	DQ0		
Verify Extended Block Protection bit	4	555	AA	2AA	55	555	60	OW	DQ0						
Enter Extended Block	3	555	AA	2AA	55	555	88								
Exit Extended Block	4	555	AA	2AA	55	555	90	X	00						
Password Program[4]	4	555	AA	2AA	55	555	38	X [0-3]	PW [0-3]						
Password Verify	4	555	AA	2AA	55	555	C8	PWA [0-3]	RPW [0-3]						
Password Protection Unlock	7	555	AA	2AA	55	555	28	PWA [0]	RPW [0]	PWA [1]	RPW [1]	PWA [2]	RPW [2]	PW [3]	RPW [3]
Set Password Protection mode[4][5]	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	DQ0		
Verify Password Protection mode	4	555	AA	2AA	55	555	60	PL	DQ0						
Set Non-Volatile Modify Protection bit[4][5]	6	555	AA	2AA	55	555	60	(BA)/ NVMP	68	(BA)/ NVMP	48	(BA)/ NVMP	DQ0		
Verify Non-Volatile Modify Protection bit	4	555	AA	2AA	55	555	60	(BA)/ NVMP	48	(BA)/ NVMP	DQ0				
Clear Non-Volatile Modify Protection bits[6][7]	6	555	AA	2AA	55	555	60	NVMP	60	(BA)/ NVMP	40	(BA)/ NVMP	DQ0		
Set Lock-Down bit	3	555	AA	2AA	55	555	78								
Verify Lock-Down bit	4	555	AA	2AA	55	555	58	BA	DQ1						
Set Lock bit	4	555	AA	2AA	55	555	48	BA	X1h						
Clear Lock bit	4	555	AA	2AA	55	555	48	BA	X0h						

Table 10. Block Protection commands (continued)

Command	Length	Bus Write Operations(1)(2)(3)													
		1st		2nd		3rd		4th		5th		6th		7th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Verify Lock bit	4	555	AA	2AA	55	555	58	BA	DQ0						
Set Standard Protection mode(5)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	DQ0		
Verify Standard Protection mode(4)	4	555	AA	2AA	55	555	60	SL	DQ0						

1. The grey cell represent Read cycles. The other cells are Write cycles.
2. SA Protection Group Address, BA Any address in the Block, BKA Bank Address, SL Standard Protection mode Lock bit Address, PL Password Protection mode Lock Bit Address, PW Password Data, PWA Password Address, RPW Password Data Being Verified, NVMP Non-Volatile Modify Protection Bit Address, OW Extended Block Protection Bit Address, X Don't Care. All values in the table are in hexadecimal.
3. Refer to *Table 11: Protection command addresses* for addresses.
4. A Reset command must be issued to return to the Read mode.
5. The 4th Bus Write cycle programs a protection bit (Extended Block Protection bit, Password, Standard Protection mode Lock bits, and a block NVMP bit). The 5th and 6th cycles verify that the bit has been successively programmed when DQ0=1. If DQ0=0 in the 6th cycle, the program command must be issued again and verified again. A 100µs delay is required between the 4th and the 5th cycle.
6. Cycle 4 erases all Non-Volatile Modify Protection bits. Cycles 5 and 6 verify that the bits have been successfully cleared when DQ0=0. If DQ0=1 in the 6th cycle, the erase command must be issued again and verified again. Before issuing the erase command, all Non-Volatile Modify Protection bits should be programmed to prevent over erasure.
7. A 12ms timeout is required between cycles 4 and 5.

Table 11. Protection command addresses

Bit	Condition	Address inputs A7-A0	Other Address Inputs
Password Protection mode Lock bit Address (PL)	$\overline{RP}$ at V_{IH}	00001010	X
	$\overline{RP}$ at V_{ID}	10001010	X
Standard Protection mode Lock bit Address (SL)		00010010	X
Non-Volatile Modify Protection bit Address (NVMP)		00000010	Block Protection Group Address
Extended Block Protection bit Address (OW)		00011010	X

Table 12. Program, Erase Times and Program, Erase Endurance cycles

Parameter		Min	Typ(1)(2)	Max(2)	Unit
Chip Erase			80	400(3)	s
Block Erase (32 KWords)			0.8	6(4)	s
Erase Suspend Latency Time				50(4)	µs
Word Program	Single or Multiple Word Program (1, 2 or 4 Words at-a-time)		10	200(3)	µs
Chip Program (Word by Word)			40	200(3)	s
Chip Program (Double Word)			20	100(3)	s
Chip Program (Quadruple Word)			10	50(3)	s
Program Suspend Latency Time				4	µs
Program/Erase cycles (per Block)		100,000			Cycles
Data Retention		20			Years

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,00 program/erase cycles.
4. Maximum value measured at worst case conditions for both temperature and V_{CC}.

7 Status Register

The M29DW641F has one Status Register. The Status Register provides information on the current or previous Program or Erase Operations executed in each bank. The various bits convey information and errors on the operation. Bus Read Operations from any address within the Bank, always read the Status Register during Program and Erase Operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in *Table 13: Status Register bits*.

7.1 Data polling bit (DQ7)

The Data Polling bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling bit is output on DQ7 when the Status Register is read.

During Program Operations the Data Polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program Operation the memory returns to Read mode and Bus Read Operations from the address just programmed output DQ7, not its complement.

During Erase Operations the Data Polling bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the Erase Operation the memory returns to Read mode.

In Erase Suspend mode the Data Polling bit will output a ’1’ during a Bus Read Operation within a block being erased. The Data Polling bit will change from a ’0’ to a ’1’ when the Program/Erase Controller has suspended the Erase Operation.

Figure 7: Data polling flowchart, gives an example of how to use the Data Polling bit. A Valid Address is the address being programmed or an address within the block being erased.

7.2 Toggle bit (DQ6)

The Toggle bit can be used to identify whether the Program/Erase Controller has successfully completed its Operation or if it has responded to an Erase Suspend. The Toggle bit is output on DQ6 when the Status Register is read.

During Program and Erase Operations the Toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read Operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle bit will output when addressing a cell within a block being erased. The Toggle bit will stop toggling when the Program/Erase Controller has suspended the Erase Operation.

Figure 8: Toggle flowchart, gives an example of how to use the Data Toggle bit. *Figure 15* and *Figure 16* describe Toggle bit timing waveform.

7.3 Error bit (DQ5)

The Error bit can be used to identify errors detected by the Program/Erase Controller. The Error bit is set to ’1’ when a Program, Block Erase or Chip Erase Operation fails to write the correct data to the memory. If the Error bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to ’0’ back to ’1’ and attempting to do so will set DQ5 to ‘1’. A Bus Read Operation to that address will show the bit is still ‘0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

7.4 Erase timer bit (DQ3)

The Erase Timer bit can be used to identify the start of Program/Erase Controller Operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer bit is set to ’1’. Before the Program/Erase Controller starts the Erase Timer bit is set to ’0’ and additional blocks to be erased may be written to the Command Interface. The Erase Timer bit is output on DQ3 when the Status Register is read.

7.5 Alternative toggle bit (DQ2)

The Alternative Toggle bit can be used to monitor the Program/Erase controller during Erase Operations. The Alternative Toggle bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase Operations the Toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read Operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within the blocks being erased. Bus Read Operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase Operation that causes the Error bit to be set the Alternative Toggle bit can be used to identify which block or blocks have caused the error. The Alternative Toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle bit does not change if the addressed block has erased correctly.

Figure 15 and *Figure 16* describe Alternative Toggle bit timing waveform.

Table 13. Status Register bits(1) (2)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	RB
Program	Bank Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program During Erase Suspend	Bank Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program Error	Bank Address	$\overline{DQ7}$	Toggle	1	–	–	Hi-Z
Chip Erase	Any Address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle	0
	Non-Erasing Block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing Block	0	Toggle	0	1	Toggle	0
	Non-Erasing Block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle	Hi-Z
	Non-Erasing Block	Data read as normal					Hi-Z
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle	Hi-Z
	Faulty Block Address	0	Toggle	1	1	Toggle	Hi-Z

1. Unspecified data bits should be ignored.
2. *Figure 15* and *Figure 16* describe Toggle and Alternative Toggle bits timing waveforms.

Figure 7. Data polling flowchart

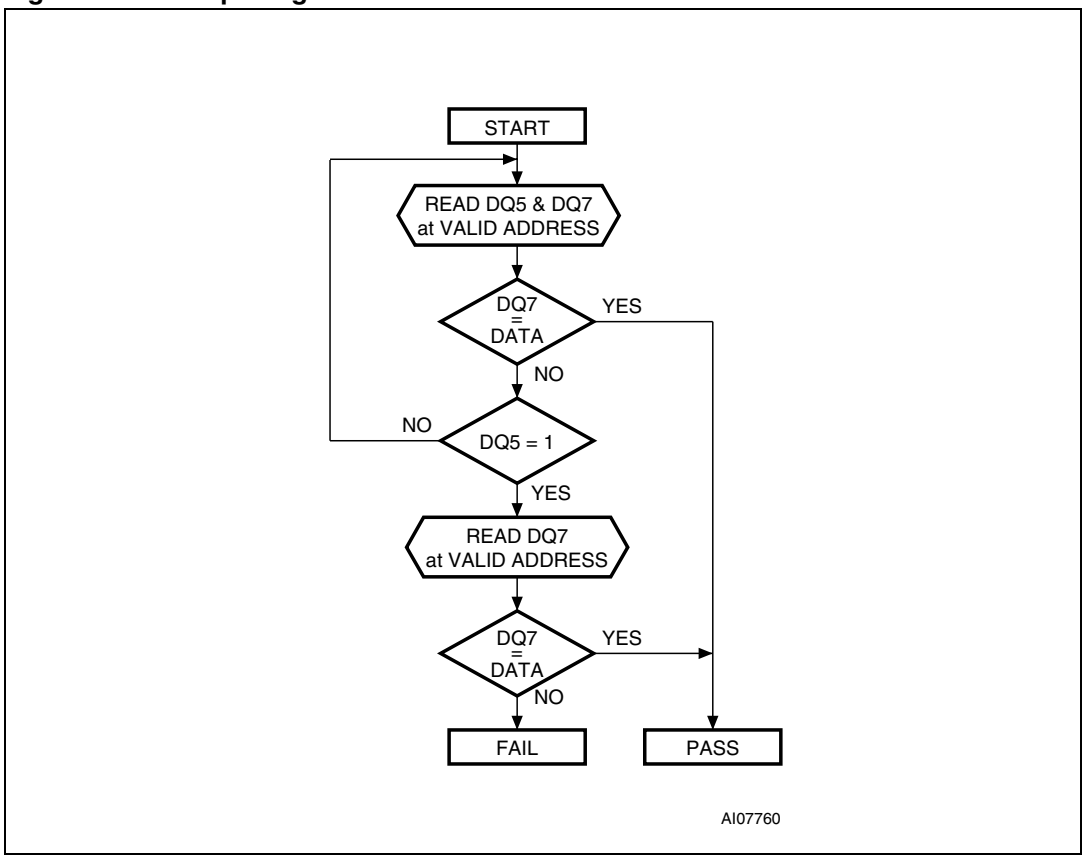
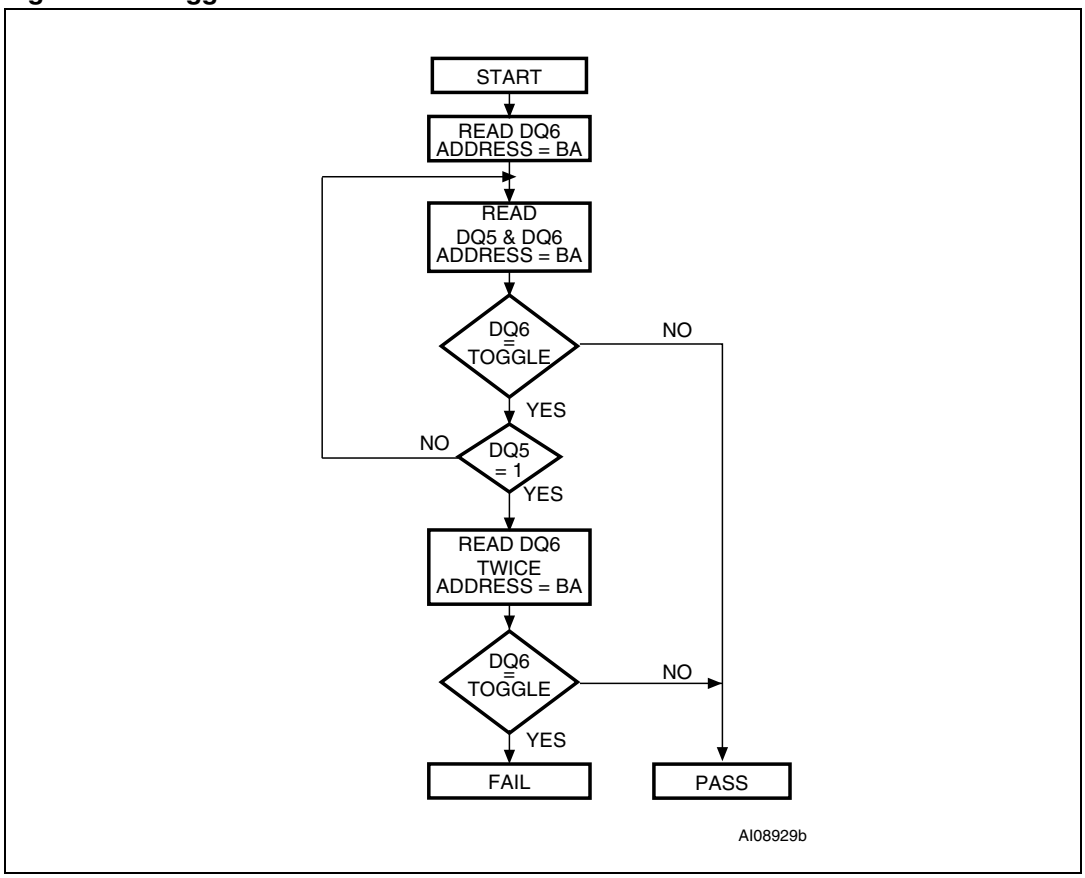


Figure 8. Toggle flowchart



1. BA = Address of Bank being Programmed or Erased.

8 Dual Operations and Multiple Bank architecture

The Multiple Bank architecture of the M29DW641F gives greater flexibility for software developers to split the code and data spaces within the memory array. The Dual Operations feature simplifies the software management of the device by allowing code to be executed from one bank while another bank is being programmed or erased.

The Dual Operations feature means that while programming or erasing in one bank, Read Operations are possible in another bank with zero latency.

Only one bank at a time is allowed to be in program or erase mode. However, certain commands can cross bank boundaries, which means that during an operation only the banks that are not concerned with the cross bank operation are available for Dual Operations. For example, if a Block Erase command is issued to erase blocks in both Bank A and Bank B, then only Banks C or D are available for read operations while the erase is being executed.

If a Read Operation is required in a bank, which is programming or erasing, the Program or Erase Operation can be suspended.

Also if the suspended operation was erase then a program command can be issued to another block, so the device can have one block in Erase Suspend mode, one programming and other banks in read mode.

By using a combination of these features, Read Operations are possible at any moment.

Figure 14 and *Figure 15* show the Dual Operations possible in other banks and in the same bank. Note that only the commonly used commands are represented in these tables.

Table 14. Dual Operations allowed in other banks

Status of bank(1)	Commands allowed in another bank(1)							
	Read Array	Read Status Register(2)	Read CFI Query	Auto Select	Program	Erase	Program /Erase Suspend	Program/ Erase Resume
Idle	Yes	Yes(3)	Yes	Yes	Yes	Yes	Yes(3)	Yes(4)
Programming	Yes	No	No	No	–	–	No	No
Erasing	Yes	No	No	No	–	–	No	No
Program Suspended	Yes	No	Yes	Yes	No	No	–	Yes(5)
Erase Suspended	Yes	No	Yes	Yes	Yes	No	–	Yes(6)

1. If several banks are involved in a Program or Erase Operation, then only the banks that are not concerned with the operation are available for Dual Operations.
2. Read Status Register is not a command. The Status Register can be read during a block Program or Erase Operation.
3. Only after a program or Erase Operation in that bank.
4. Only after a Program or Erase Suspend command in that bank.
5. Only a Program Resume is allowed if the bank was previously in Program Suspend mode.
6. Only an Erase Resume is allowed if the bank was previously in Erase Suspend mode.

Table 15. Dual Operations allowed in same bank

Status of bank	Commands allowed in same bank							
	Read Array	Read Status Register(1)	Read CFI Query	Auto Select	Program	Erase	Program/ Erase Suspend	Program/ Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes(2)	Yes(3)
Programming	No	Yes	No	No	–	–	Yes(4)	–
Erasing	No	Yes	No	No	–	No	Yes(5)	–
Program Suspended	Yes(6)	No	Yes	Yes	No	–	–	Yes
Erase Suspended	Yes(6)	Yes(7)	Yes	Yes	Yes(6)	No	–	Yes

1. Read Status Register is not a command. The Status Register can be read during a block Program or Erase Operation.
2. Only after a program or Erase Operation in that bank.
3. Only after a Program or Erase Suspend command in that bank.
4. Only a Program Suspend.
5. Only an Erase suspend.
6. Not allowed in the Block or Word that is being erased or programmed.
7. The Status Register can be read by addressing the block being erase suspended.

9 Maximum ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 16. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output voltage (1)(2)	–0.6	V_{CC} +0.6	V
V_{CC}	Supply voltage	–0.6	4	V
V_{ID}	Identification voltage	–0.6	13.5	V
V_{PP}(3)	Program voltage	–0.6	13.5	V

1. Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2V during transition and for less than 20ns during transitions.
3. V_{PP} must not remain at 12V for more than a total of 80hrs.

10 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 17: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 17. Operating and AC measurement conditions

Parameter	60		70		Unit
	Min	Max	Min	Max	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
Ambient Operating Temperature	–40	85	–40	85	°C
Load Capacitance (C_L)	30		30		pF
Input Rise and Fall Times		10		10	ns
Input Pulse voltages	0 to V_{CC}		0 to V_{CC}		V
Input and Output Timing Ref. voltages	$V_{CC}/2$		$V_{CC}/2$		V

Figure 9. AC measurement I/O waveform

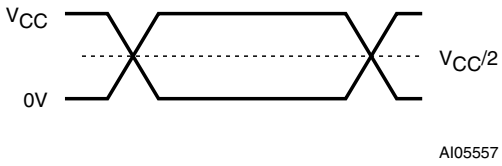


Figure 10. AC measurement load circuit

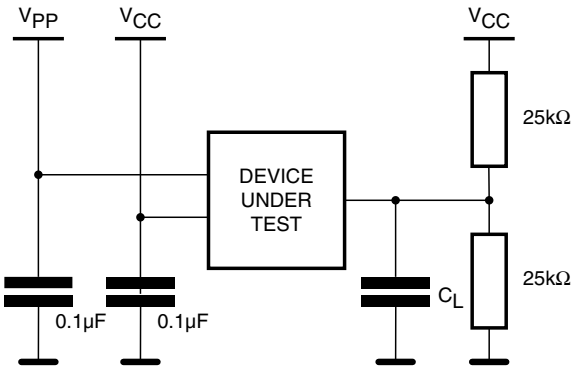


Table 18. Device capacitance

Symbol	Parameter(1)	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V		12	pF

1. Sampled only, not 100% tested.

Table 19. DC characteristics

Symbol	Parameter	Test condition		Min	Max	Unit
I_{LI}	Input Leakage current	0V ≤V_{IN} ≤V_{CC}			±1	µA
I_{LO}	Output Leakage current	0V ≤V_{OUT} ≤V_{CC}			±1	µA
I_{CC1}(1)	Supply current (Read)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 6MHz			10	mA
I_{CC2}	Supply current (Standby)	$\overline{E}$ = V_{CC} ±0.2V, $\overline{RP}$ = V_{CC} ±0.2V			100	µA
I_{CC3} (1)(2)	Supply current (Program/Erase)	Program/Erase Controller active	$V_{PP}/\overline{WP}$ = V_{IL} or V_{IH}		20	mA
			$V_{PP}/\overline{WP}$ = V_{PPH}		20	mA
V_{IL}	Input Low voltage			–0.5	0.8	V
V_{IH}	Input High voltage			0.7V_{CC}	V_{CC} +0.3	V
V_{PPH}	Voltage for Fast Program Acceleration	V_{CC} = 2.7V ±10%		11.5	12.5	V
I_{PP}	Current for Fast Program Acceleration	V_{CC} =2.7V ±10%			15	mA
V_{OL}	Output Low voltage	I_{OL} = 1.8mA			0.45	V
V_{OH}	Output High voltage	I_{OH} = –100µA		V_{CC} –0.4		V
V_{ID}	Identification voltage			11.5	12.5	V
V_{LKO}	Program/Erase Lockout Supply voltage			1.8	2.3	V

1. In Dual Operations the Supply current will be the sum of I_{CC1}(read) and I_{CC3} (program/erase).
2. Sampled only, not 100% tested.

Figure 11. Random Read AC waveforms

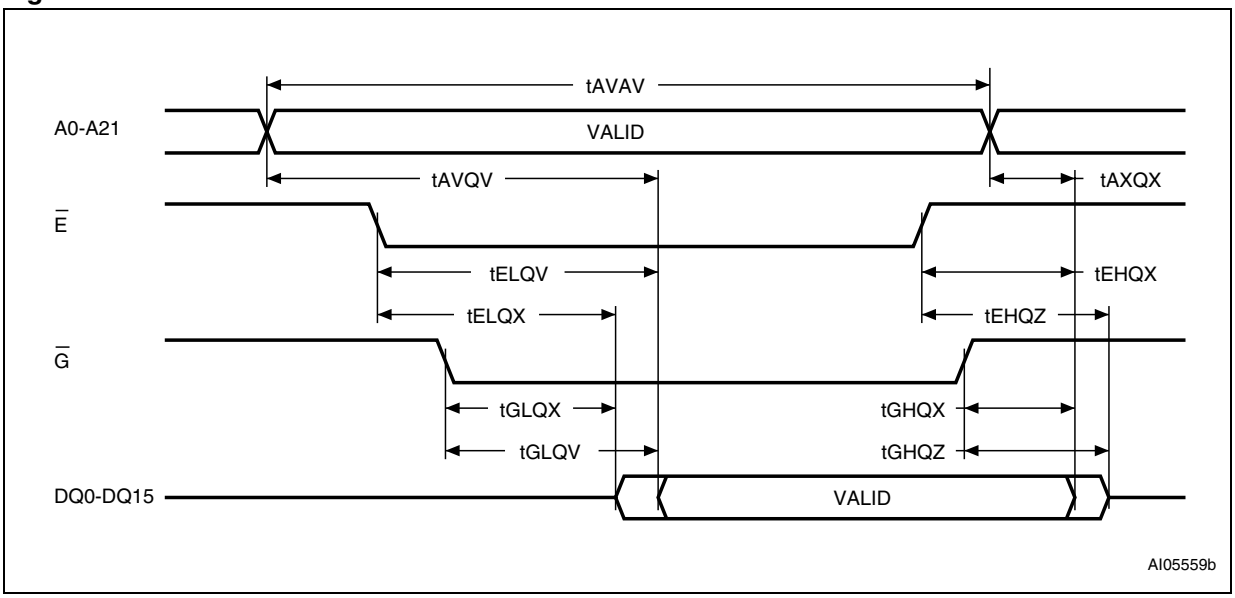


Figure 12. Page Read AC waveforms

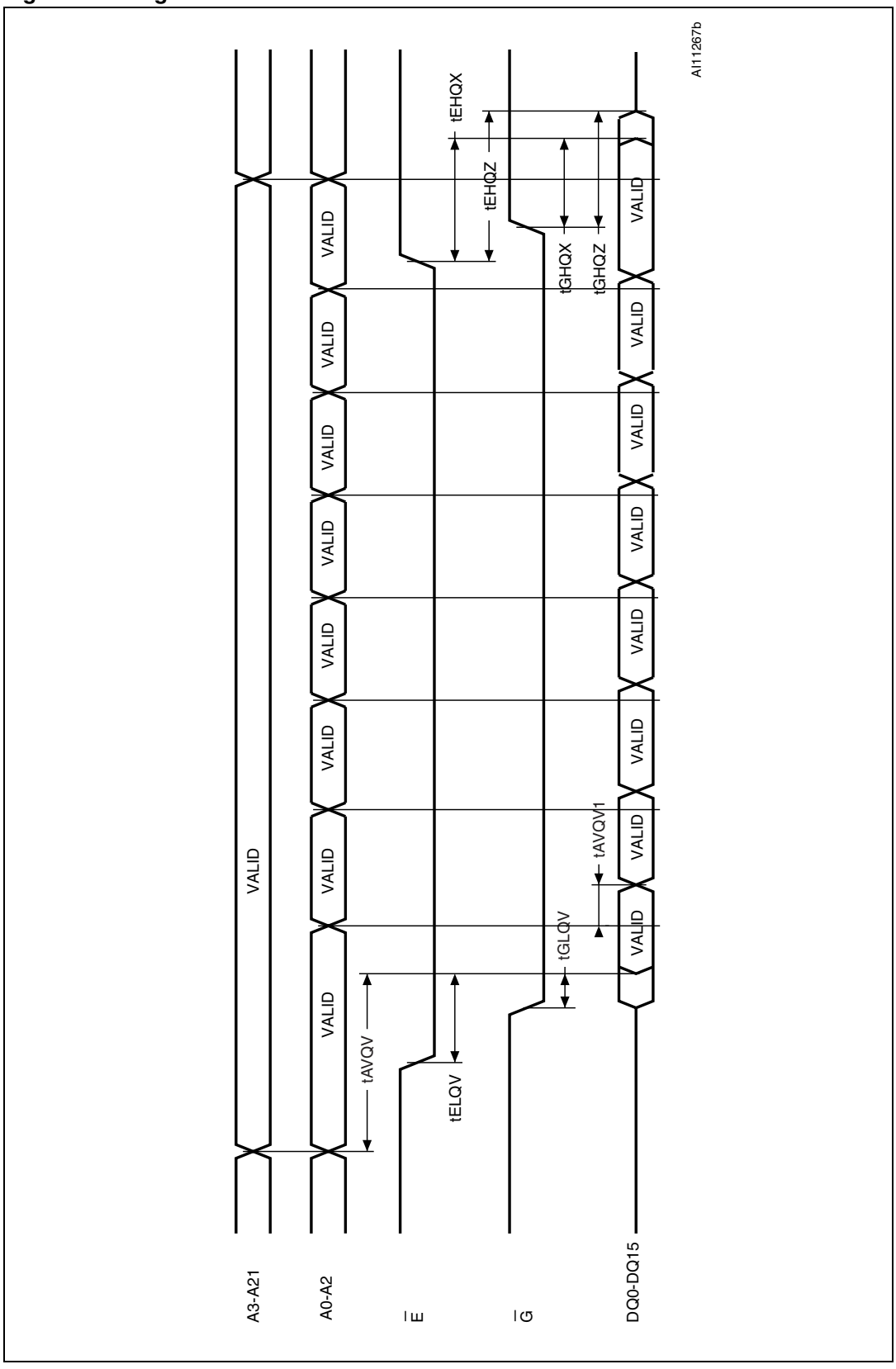


Table 20. Read AC characteristics

Symbol	Alt	Parameter	Test condition		60	70	Unit
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Min	60	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	60	70	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	25	25	ns
t_{ELQX}(1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	Min	0	0	ns
t_{EHQZ}(1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	25	25	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	60	70	ns
t_{GLQX}(1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	25	25	ns
t_{GHQZ}(1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	25	25	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns

1. Sampled only, not 100% tested.

Figure 13. Write AC waveforms, Write Enable controlled

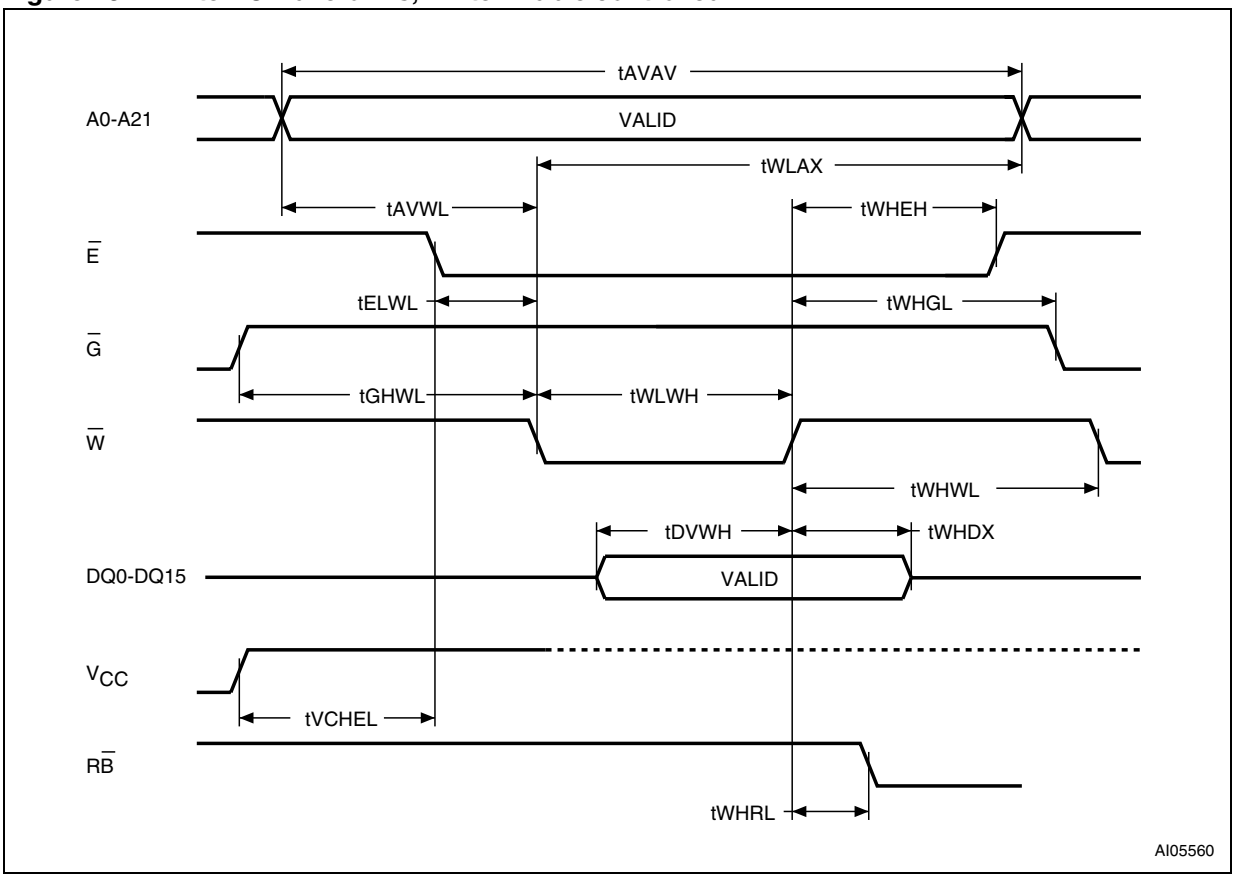


Table 21. Write AC characteristics, Write Enable controlled

Symbol	Alt	Parameter		60	70	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	60	70	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	45	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	45	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	ns

1. Sampled only, not 100% tested.

Figure 14. Write AC waveforms, Chip Enable controlled

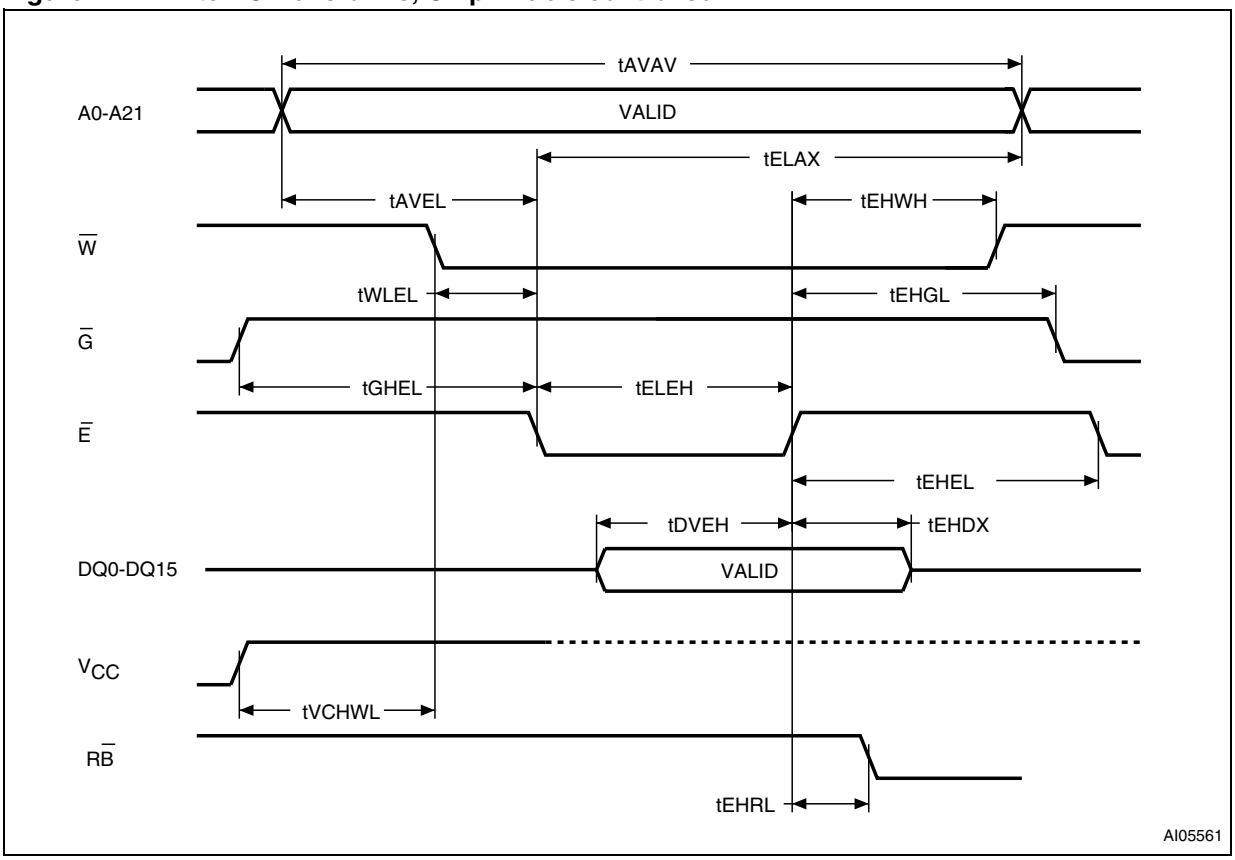
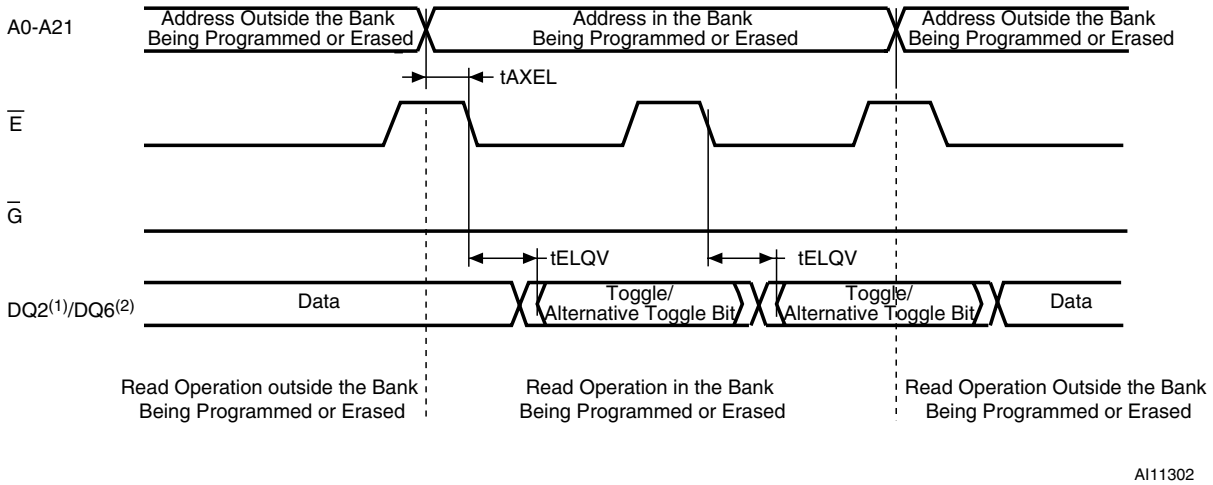


Table 22. Write AC characteristics, Chip Enable controlled

Symbol	Alt	Parameter		60	70	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	60	70	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	45	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	45	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $R\overline{B}$ Low	Max	30	30	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns

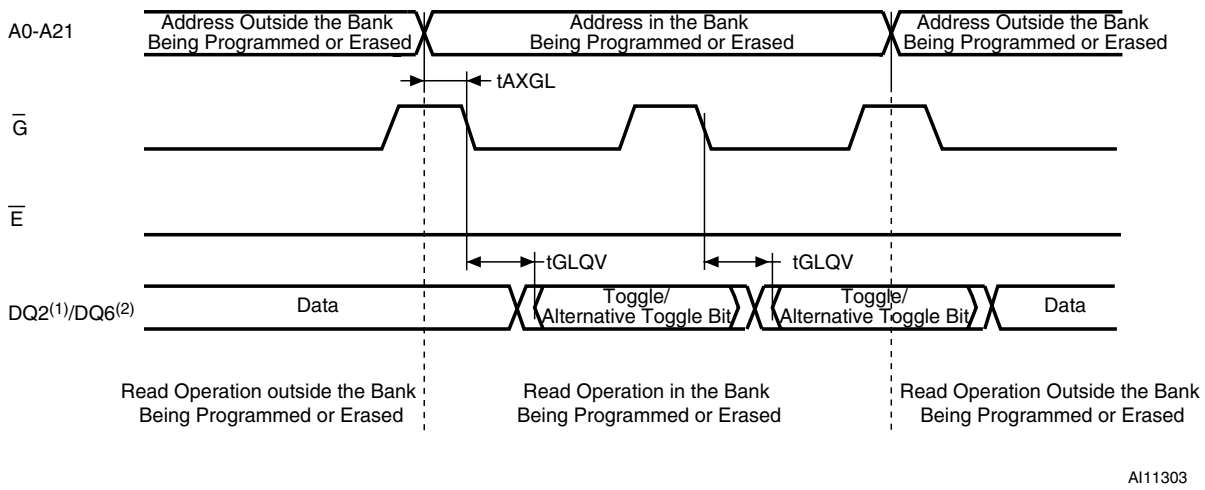
1. Sampled only, not 100% tested.

Figure 15. Toggle and alternative toggle bits mechanism, Chip Enable controlled



1. The Toggle bit is output on DQ6.
2. The Alternative Toggle bit is output on DQ2.
3. Refer to *Table 20: Read AC characteristics* for the value of t_{ELQV}.

Figure 16. Toggle and alternative toggle bits mechanism, Output Enable controlled



1. The Toggle bit is output on DQ6.
2. The Alternative Toggle bit is output on DQ2.
3. Refer to *Table 20: Read AC characteristics* for the value of t_{GLQV}.

Table 23. Toggle and alternative toggle bits AC characteristics

Symbol	Alt	Parameter		60	70	Unit
t_{AXEL}		Address Transition to Chip Enable Low	Min	10	10	ns
t_{AXGL}		Address Transition to Output Enable Low	Min	10	10	ns

Figure 17. Reset/Block Temporary Unprotect AC waveforms (no Program/Erase ongoing)

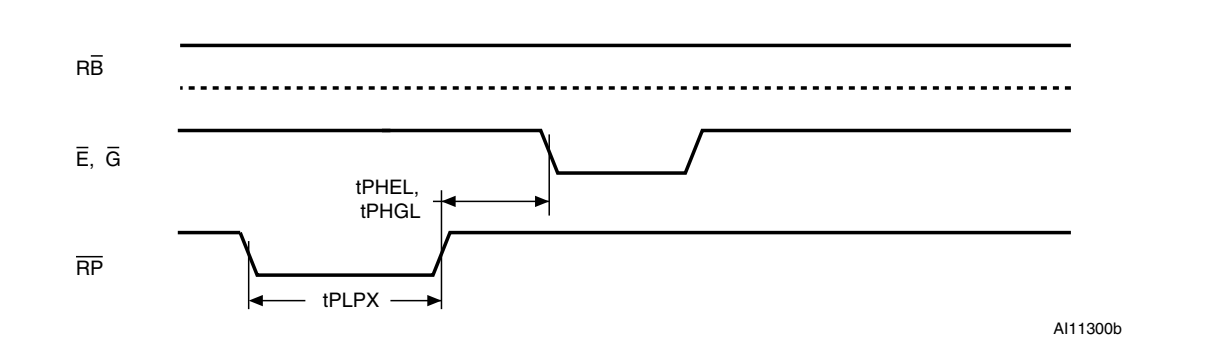


Figure 18. Reset/Block Temporary Unprotect during Program/Erase Operation AC waveforms

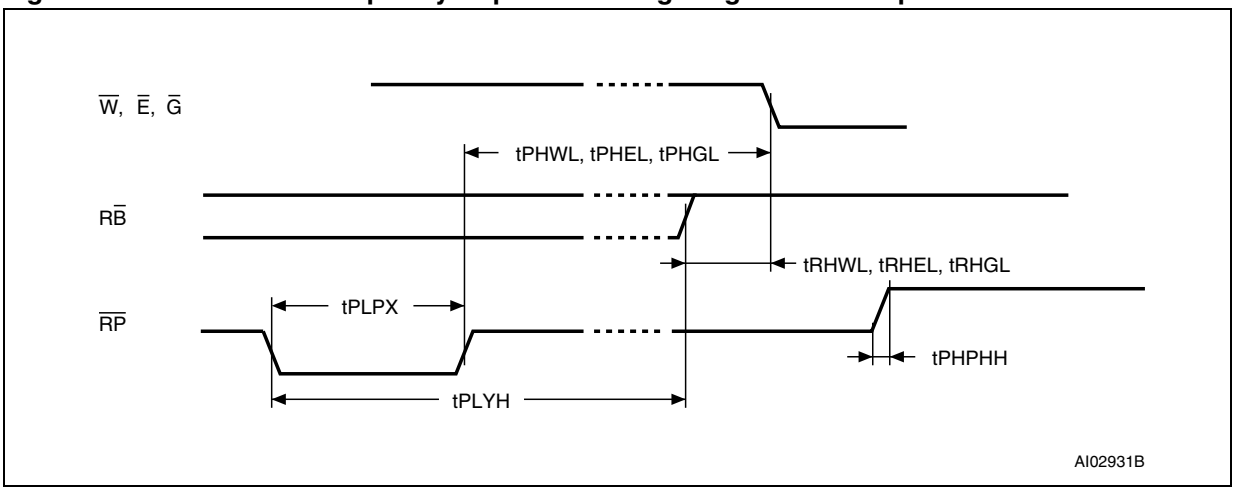


Figure 19. Accelerated Program timing waveforms

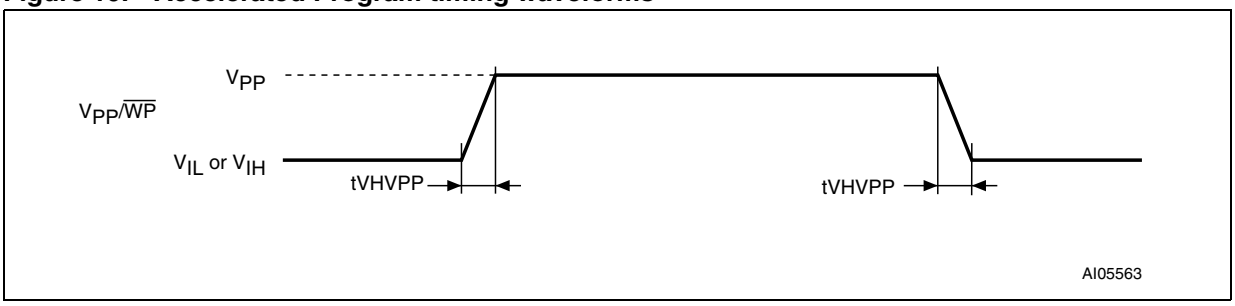


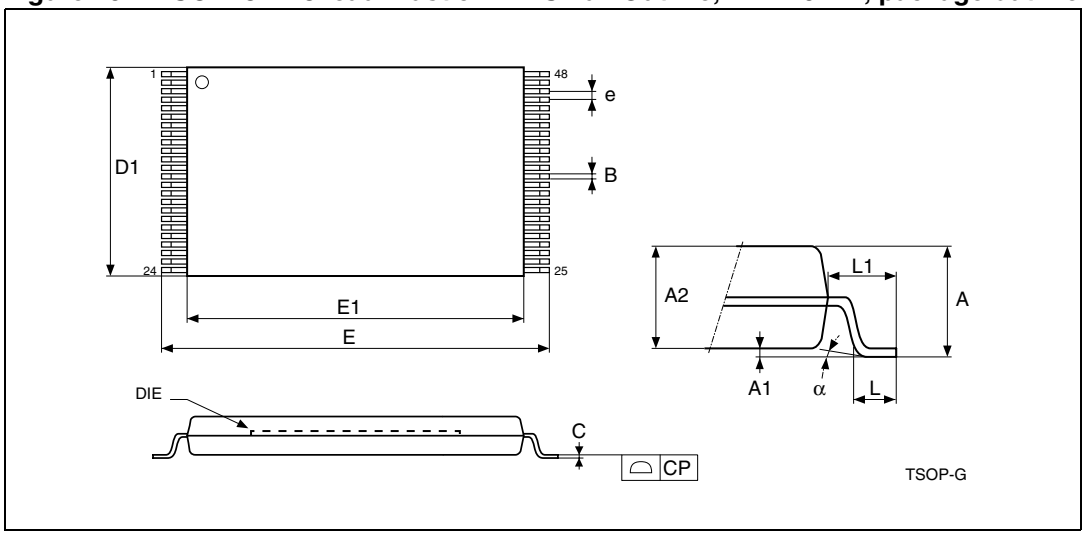
Table 24. Reset/Block Temporary Unprotect AC characteristics

Symbol	Alt	Parameter		60	70	Unit
t_{PHEL}, t_{PHWL}, t_{PHGL}(1)	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50		ns
t_{RHEL}, t_{RHWL} t_{RHGL}(1)	t_{RB}	R$\overline{B}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0		ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	Min	500		ns
t_{PLYH}(1)	t_{READY}	$\overline{RP}$ Low to Read mode, during Program or Erase	Max	20		µs
t_{PHPHH}		$\overline{RP}$ Rise Time to V_{ID}	Min	500		ns
t_{VHVPP}		V_{PP} Rise and Fall Time	Min	250		ns

1. Sampled only, not 100% tested.

11 Package mechanical data

Figure 20. TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, package outline

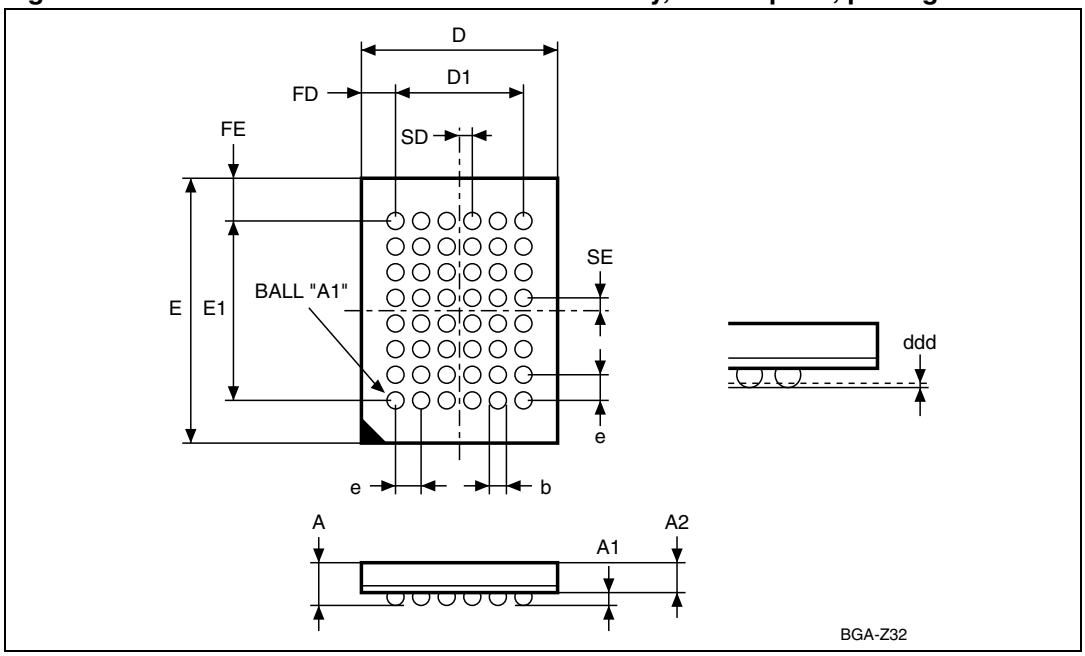


1. Drawing is not to scale.

Table 25. TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.100			0.0039
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	–
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
α	3	0	5	3	0	5

Figure 21. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.8mm pitch, package outline



1. Drawing is not to scale.

Table 26. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.8mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	4.000	–	–	0.1575	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.600	–	–	0.2205	–	–
e	0.800	–	–	0.0315	–	–
FD	1.000	–	–	0.0394	–	–
FE	1.200	–	–	0.0472	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

12 Part numbering

Table 27. Ordering information scheme

Example: M29DW641F 70 N 1 T

Device type

M29

Architecture

D = Dual or Multiple Bank

Operating voltage

W = V_{CC} = 2.7 to 3.6V

Device function

641F = 64 Mbit (x16), Multiple Bank, Page, Boot Block, 8+24+24+8 partitioning, Flash Memory

Speed

60 = 60ns

70 = 70ns

Package

N = TSOP48, 12 x 20 mm

ZE = TFBGA48 6 x 8mm, 0.8mm pitch

Temperature range

1 = 0 to 70 °C

6 = –40 to 85 °C

Option

Blank = Standard Packing

T = Tape & Reel Packing

E = ECOPACK Package, Standard Packing

F = ECOPACK Package, Tape & Reel 24mm Packing

Note: This product is also available with the Extended Block factory locked. For further details and ordering information contact your nearest Numonyx sales office.

The device is shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact your nearest Numonyx Sales Office.

Appendix A Block addresses

Table 28. Block Addresses

Bank	Block	Block size (KWords)	Protection Block Group	Addresses
Bank A	0	4	Protection Group	000000h–000FFFh(1)
	1	4	Protection Group	001000h–001FFFh(1)
	2	4	Protection Group	002000h–002FFFh(1)
	3	4	Protection Group	003000h–003FFFh((1)
	4	4	Protection Group	004000h–004FFFh(1)
	5	4	Protection Group	005000h–005FFFh(1)
	6	4	Protection Group	006000h–006FFFh(1)
	7	4	Protection Group	007000h–007FFFh(1)
	8	32	Protection Group	008000h–00FFFFh
	9	32	Protection Group	010000h–017FFFh
	10	32	Protection Group	018000h–01FFFFh
	11	32	Protection Group	020000h–027FFFh
	12	32		028000h–02FFFFh
	13	32		030000h–037FFFh
	14	32		038000h–03FFFFh
	15	32	Protection Group	040000h–047FFFh
	16	32		048000h–04FFFFh
	17	32		050000h–057FFFh
	18	32		058000h–05FFFFh
	19	32	Protection Group	060000h–067FFFh
	20	32		068000h–06FFFFh
	21	32		070000h–077FFFh
	22	32		078000h–07FFFFh

Table 28. Block Addresses (continued)

Bank	Block	Block size (KWords)	Protection Block Group	Addresses
Bank B	23	32	Protection Group	080000h–087FFFh
	24	32		088000h–08FFFFh
	25	32		090000h–097FFFh
	26	32		098000h–09FFFFh
	27	32	Protection Group	0A0000h–0A7FFFh
	28	32		0A8000h–0AFFFFh
	29	32		0B0000h–0B7FFFh
	30	32		0B8000h–0BFFFFh
	31	32	Protection Group	0C0000h–0C7FFFh
	32	32		0C8000h–0CFFFFh
	33	32		0D0000h–0D7FFFh
	34	32		0D8000h–0DFFFFh
	35	32	Protection Group	0E0000h–0E7FFFh
	36	32		0E8000h–0EFFFFh
	37	32		0F0000h–0F7FFFh
	38	32		0F8000h–0FFFFFh
	39	32	Protection Group	100000h–107FFFh
	40	32		108000h–10FFFFh
	41	32		110000h–117FFFh
	42	32		118000h–11FFFFh
	43	32	Protection Group	120000h–127FFFh
	44	32		128000h–12FFFFh
	45	32		130000h–137FFFh
	46	32		138000h–13FFFFh
	47	32	Protection Group	140000h–147FFFh
	48	32		148000h–14FFFFh
	49	32		150000h–157FFFh
	50	32		158000h–15FFFFh
	51	32	Protection Group	160000h–167FFFh
	52	32		168000h–16FFFFh
	53	32		170000h–177FFFh
	54	32		178000h–17FFFFh

Table 28. Block Addresses (continued)

Bank	Block	Block size (KWords)	Protection Block Group	Addresses
Bank B	55	32	Protection Group	180000h–187FFFh
	56	32		188000h–18FFFFh
	57	32		190000h–197FFFh
	58	32		198000h–19FFFFh
	59	32	Protection Group	1A0000h–1A7FFFh
	60	32		1A8000h–1AFFFFh
	61	32		1B0000h–1B7FFFh
	62	32		1B8000h–1BFFFFh
	63	32	Protection Group	1C0000h–1C7FFFh
	64	32		1C8000h–1CFFFFh
	65	32		1D0000h–1D7FFFh
	66	32		1D8000h–1DFFFFh
	67	32	Protection Group	1E0000h–1E7FFFh
	68	32		1E8000h–1EFFFFh
	69	32		1F0000h–1F7FFFh
	70	32		1F8000h–1FFFFFh
Bank C	71	32	Protection Group	200000h–207FFFh
	72	32		208000h–20FFFFh
	73	32		210000h–217FFFh
	74	32		218000h–21FFFFh
	75	32	Protection Group	220000h–227FFFh
	76	32		228000h–22FFFFh
	77	32		230000h–237FFFh
	78	32		238000h–23FFFFh
	79	32	Protection Group	240000h–247FFFh
	80	32		248000h–24FFFFh
	81	32		250000h–257FFFh
	82	32		258000h–25FFFFh
	83	32	Protection Group	260000h–267FFFh
	84	32		268000h–26FFFFh
	85	32		270000h–277FFFh
	86	32		278000h–27FFFFh

Table 28. Block Addresses (continued)

Bank	Block	Block size (KWords)	Protection Block Group	Addresses
Bank C	87	32	Protection Group	280000h–287FFFh
	88	32		288000h–28FFFFh
	89	32		290000h–297FFFh
	90	32		298000h–29FFFFh
	91	32	Protection Group	2A0000h–2A7FFFh
	92	32		2A8000h–2AFFFFh
	93	32		2B0000h–2B7FFFh
	94	32		2B8000h–2BFFFFh
	95	32	Protection Group	2C0000h–2C7FFFh
	96	32		2C8000h–2CFFFFh
	97	32		2D0000h–2D7FFFh
	98	32		2D8000h–2DFFFFh
	99	32	Protection Group	2E0000h–2E7FFFh
	100	32		2E8000h–2EFFFFh
	101	32		2F0000h–2F7FFFh
	102	32		2F8000h–2FFFFFh
	103	32	Protection Group	300000h–307FFFh
	104	32		308000h–30FFFFh
	105	32		310000h–317FFFh
	106	32		318000h–31FFFFh
	107	32	Protection Group	320000h–327FFFh
	108	32		328000h–32FFFFh
	109	32		330000h–337FFFh
	110	32		338000h–33FFFFh
	111	32	Protection Group	340000h–347FFFh
	112	32		348000h–34FFFFh
	113	32		350000h–357FFFh
	114	32		358000h–35FFFFh
	115	32	Protection Group	360000h–367FFFh
	116	32		368000h–36FFFFh
	117	32		370000h–377FFFh
	118	32		378000h–37FFFFh

Table 28. Block Addresses (continued)

Bank	Block	Block size (KWords)	Protection Block Group	Addresses
Bank D	119	32	Protection Group	380000h–387FFFh
	120	32		388000h–38FFFFh
	121	32		390000h–397FFFh
	122	32		398000h–39FFFFh
	123	32	Protection Group	3A0000h–3A7FFFh
	124	32		3A8000h–3AFFFFh
	125	32		3B0000h–3B7FFFh
	126	32		3B8000h–3BFFFFh
	127	32	Protection Group	3C0000h–3C7FFFh
	128	32		3C8000h–3CFFFFh
	129	32		3D0000h–3D7FFFh
	130	32		3D8000h–3DFFFFh
	131	32	Protection Group	3E0000h–3E7FFFh
	132	32	Protection Group	3E8000h–3EFFFFh
	133	32	Protection Group	3F0000h–3F7FFFh
	134	4	Protection Group	3F8000h–3F8FFFh
	135	4	Protection Group	3F9000h–3F9FFFh
	136	4	Protection Group	3FA000h–3FAFFFh
	137	4	Protection Group	3FB000h–3FBFFFh
	138	4	Protection Group	3FC000h–3FCFFFh
	139	4	Protection Group	3FD000h–3FDFFFh
	140	4	Protection Group	3FE000h–3FEFFFh
	141	4	Protection Group	3FF000h–3FFFFFh

1. Used as the Extended Block Addresses in Extended Block mode.

Appendix B Common Flash Interface (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query command is issued the addressed bank enters Read CFI Query mode and Read Operations in the same bank (A21-A19) output the CFI data. *Table 29*, *Table 30*, *Table 31*, *Table 32*, *Table 33* and *Table 34* show the addresses (A0-A10) used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see *Table 34: Security Code Area*). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by Numonyx.

Table 29. Query structure overview

Address	Sub-section name	Description
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
40h	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
61h	Security Code Area	64 bit unique device number

1. Query data are always presented on the lowest order data outputs.

Table 30. CFI Query Identification String

Address	Data	Description	Value
10h	0051h		“Q”
11h	0052h	Query Unique ASCII String "QRY"	"R"
12h	0059h		"Y"
13h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	AMD Compatible
14h	0000h		
15h	0040h	Address for Primary Algorithm extended Query table (see *Table 33*)	P = 40h
16h	0000h		
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
18h	0000h		
19h	0000h	Address for Alternate Algorithm extended Query table	NA
1Ah	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 31. CFI Query System Interface Information

Address	Data	Description	Value
1Bh	0027h	V_{CC} Logic Supply Minimum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	2.7V
1Ch	0036h	V_{CC} Logic Supply Maximum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	3.6V
1Dh	00B5h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	11.5V
1Eh	00C5h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	12.5V
1Fh	0004h	Typical timeout per single byte/Word program = 2^n µs	16µs
20h	0000h	Typical timeout for minimum size write buffer program = 2^n µs	NA
21h	000Ah	Typical timeout per individual block erase = 2^n ms	1s
22h	0000h	Typical timeout for full Chip Erase = 2^n ms	NA
23h	0004h	Maximum timeout for byte/Word program = 2^n times typical	256 µs
24h	0000h	Maximum timeout for write buffer program = 2^n times typical	NA
25h	0003h	Maximum timeout per individual block erase = 2^n times typical	8s
26h	0000h	Maximum timeout for Chip Erase = 2^n times typical	NA

Table 32. Device Geometry Definition

Address	Data	Description	Value
27h	0017h	Device Size = 2^n in number of bytes	8 Mbytes
28h 29h	0002h 0000h	Flash Device Interface Code description	x16 Async.
2Ah 2Bh	0003h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	8
2Ch	0003h	Number of Erase Block Regions(1). It specifies the number of regions containing contiguous Erase Blocks of the same size.	3
2Dh 2Eh	0007h 0000h	Erase Block Region 1 Information Number of Erase Blocks of identical size = 0007h+1	8
2Fh 30h	0020h 0000h	Erase Block Region 1 Information Block size in Region 1 = 0020h * 256 byte	8 Kbytes
31h 32h	007Dh 0000h	Erase Block Region 2 Information Number of Erase Blocks of identical size = 007Dh+1	126
33h 34h	0000h 0001h	Erase Block Region 2 Information Block size in Region 2 = 0100h * 256 byte	64 Kbytes
35h 36h	0007h 0000h	Erase Block Region 3 information Number of Erase Blocks of identical size = 0007h + 1	8
37h 38h	0020h 0000h	Erase Block Region 3 information Block size in region 3 = 0020h * 256 bytes	8 Kbytes
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 information	0

1. Erase Block Region 1 corresponds to addresses 000000h to 007FFFh; Erase block Region 2 corresponds to addresses 008000h to 3F7FFFh and Erase Block Region 3 corresponds to addresses 3F8000h to 3FFFFFh.

Table 33. Primary Algorithm-specific extended Query table

Address	Data	Description	Value
40h	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P"
41h	0052h		"R"
42h	0049h		"I"
43h	0031h	Major version number, ASCII	"1"
44h	0033h	Minor version number, ASCII	"3"
45h	0000h	Address Sensitive Unlock (bits 1 to 0) 00 = required, 01= not required Silicon Revision Number (bits 7 to 2)	Yes
46h	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = Read and Write	2
47h	0001h	Block Protection 00 = not supported, x = number of sectors in per group	1
48h	0001h	Temporary Block Unprotect 00 = not supported, 01 = supported	Yes
49h	0007h	Block Protect /Unprotect 07 = M29DW641F	7
4Ah	0077h	Simultaneous Operations, x = number of blocks (excluding Bank A)	119
4Bh	0000h	Burst mode, 00 = not supported, 01 = supported	No
4Ch	0002h	Page mode, 00 = not supported, 01 = 4 page Word, 02 = 8 page Word	Yes
4Dh	00B5h	V_{PP} Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5V
4Eh	00C5h	V_{PP} Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5V
4Fh	0001h	Top/Bottom Boot Block Flag 00h = uniform device 01h = 8 x8 Kbyte Blocks, Top and Bottom Boot with Write Protect 02h = Bottom boot device 03h = Top Boot Device 04h = Both Top and Bottom	T/B
50h	0001h	Program Suspend, 00 = not supported, 01 = supported	Yes
57h	0004h	Bank Organization, 00 = data at 4Ah is zero X = number of banks	4
58h	0017h	Bank A information X = number of blocks in Bank A	23
59h	0030h	Bank B information X = number of blocks in Bank B	48

Table 33. Primary Algorithm-specific extended Query table (continued)

Address	Data	Description	Value
5Ah	0030h	Bank C information X = number of blocks in Bank C	48
5Bh	0017h	Bank D information X = number of blocks in Bank D	23

Table 34. Security Code Area

Address	Data	Description
61h	XXXX	64 bit: unique device number
62h	XXXX	
63h	XXXX	
64h	XXXX	

Appendix C Extended Memory Block

The M29DW641F has an extra block, the Extended Block, that can be accessed using a dedicated command.

This Extended Block is 128 Words. It is used as a security block (to provide a permanent security identification number) or to store additional information.

The Extended Block is divided into two memory areas of 64 Words each:

- The first one is Factory Locked.
- The second one is Customer Lockable. It is up to the customer to protect it from Program Operations. Its status is indicated by bit DQ6 and DQ7. When DQ7 is set to '1' and DQ6 to '0', it indicates that this second memory area is Customer Lockable. When DQ7 and DQ6 are both set to '1', it indicates that the second part of the Extended Block is Customer Locked and protected from Program Operations. Bit DQ7 being permanently locked to either '1' or '0' is another security feature which ensures that a customer lockable device cannot be used instead of a factory locked one.

Bits DQ6 and DQ7 are the most significant bits in the Extended Block Protection indicator and a specific procedure must be followed to read it. See *Section 3.6.2: Verify Extended Block Protection indicator*" in *Table 5: Block Protection*, for details of how to read bit DQ7.

The Extended Block can only be accessed when the device is in Extended Block mode. For details of how the Extended Block mode is entered and exited, refer to the *Section 6.1.10: Program command* and *Section 6.3.2: Exit Extended Block command*, and to *Table 10: Block Protection commands*.

C.1 Factory Locked section of the Extended Block

The first section of The Extended Block is permanently protected from Program Operations and cannot be unprotected. The Random Number, Electronic Serial Number (ESN) and Security Identification Number (see *Table 35: Extended Block Address and Data*) are written in this section in the factory.

C.2 Customer Lockable section of the Extended Block

The device is delivered with the second section of the Extended Block "Customer Lockable": bits DQ7 and DQ6 are set to '1' and '0' respectively. It is up to the customer to program and protect this section of the Extended Block but care must be taken because the protection is not reversible.

There are three ways of protecting this section:

- Issue the Enter Extended Block command to place the device in Extended Block mode, then use the In-System Technique with $\overline{RP}$ either at V_{IH} or at V_{ID}. Refer to *Section D.2: In-system technique* in *Appendix D: High voltage Block Protection*, and to the corresponding flowcharts *Figure 24* and *Figure 25* for a detailed explanation of the technique).
- Issue the Enter Extended Block command to place the device in Extended Block mode, then use the Programmer Technique. Refer to *Section D.1: Programmer technique* in *Appendix D: High voltage Block Protection*, and to the corresponding flowcharts *Figure 22* and *Figure 23* for a detailed explanation of the technique).
- Issue a Set Extended Block Protection bit command to program the Extended Block Protection bit to '1' thus preventing the second section of the Extended Block from being programmed.

Bit DQ6 of the Extended Block Protection indicator is automatically set to '1' to indicate that the second section of the Extended Block is Customer Locked.

Once the Extended Block is programmed and protected, the Exit Extended Block command must be issued to exit the Extended Block mode and return the device to Read mode.

Table 35. Extended Block Address and Data

Device	Address(1)	Data	
		Factory Locked	Customer Lockable
M29DW641F	000000h-00003Fh	Random Number, Security Identification Number, ESN(2)	Unavailable
	000040h-00007Fh	Unavailable	Determined by Customer

1. See *Table 28: Block Addresses*.
2. ENS = Electronic Serial Number.

Appendix D High voltage Block Protection

he High voltage Block Protection can be used to prevent any operation from modifying the data stored in the memory. The blocks are protected in groups, refer to *Appendix A*, *Table 28: Block Addresses* for details of the Protection Groups. Once protected, Program and Erase Operations within the protected group fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the Signal Descriptions section.

To protect the Extended Block issue the Enter Extended Block command and then use either the Programmer or In-System technique. Once protected issue the Exit Extended Block command to return to read mode. The Extended Block protection is irreversible, once protected the protection cannot be undone.

D.1 Programmer technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a group of blocks follow the flowchart in *Figure 22: Programmer equipment Group Protect flowchart*. To unprotect the whole chip it is necessary to protect all of the groups first, then all groups can be unprotected at the same time. To unprotect the chip follow *Figure 23: Programmer equipment Chip Unprotect flowchart*. *Figure 36: Programmer technique Bus Operations, 8-bit or 16-bit mode*, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

D.2 In-system technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$ (1). This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the memory has been fitted to the system.

To protect a group of blocks follow the flowchart in *Figure 24: In-System equipment Group Protect flowchart*. To unprotect the whole chip it is necessary to protect all of the groups first, then all the groups can be unprotected at the same time. To unprotect the chip follow *Figure 25: In-System equipment Chip Unprotect flowchart*.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

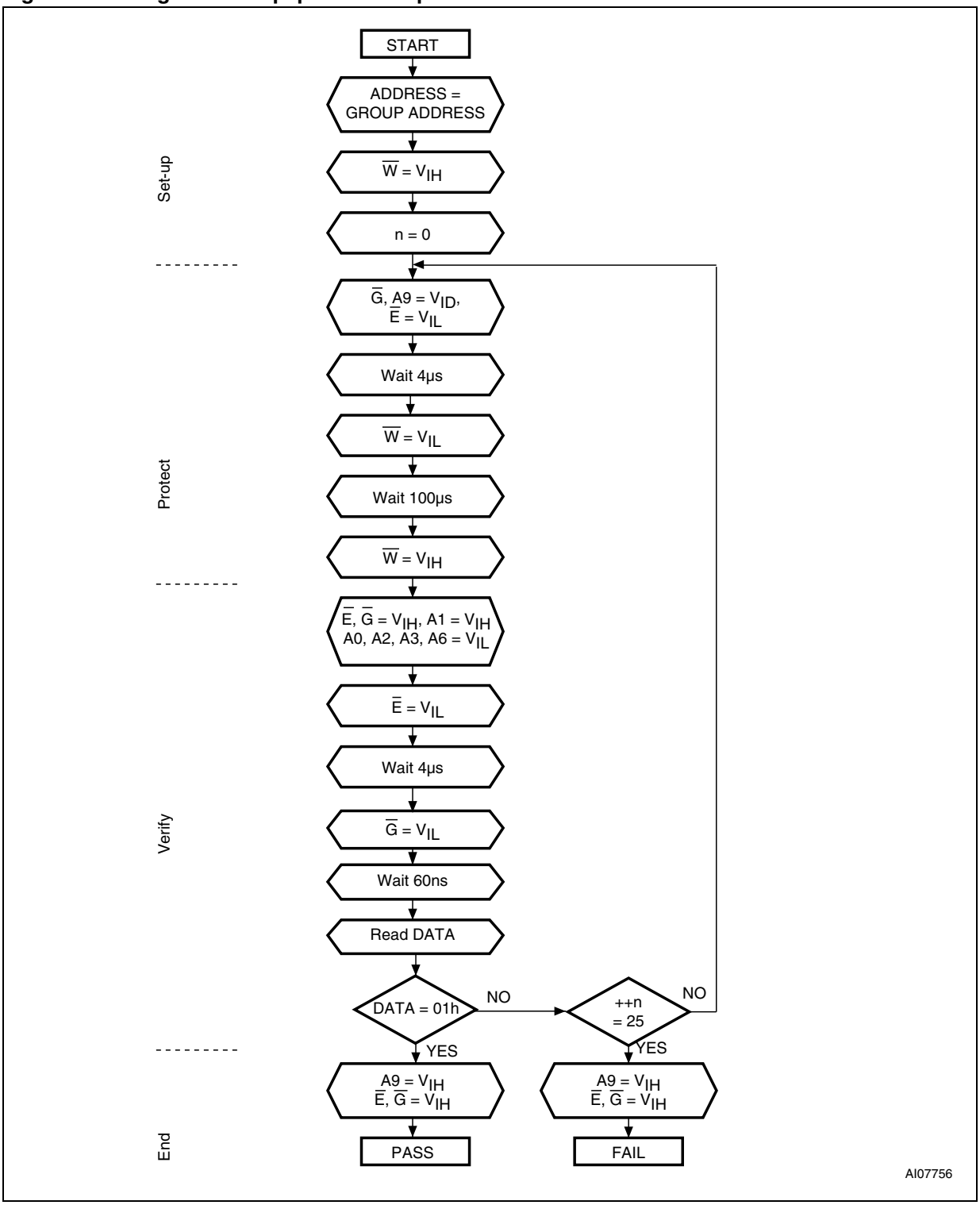
Note: $\overline{RP}$ can be either at V_{IH} or at V_{ID} when using the In-System Technique to protect the Extended Block.

Table 36. Programmer technique Bus Operations, 8-bit or 16-bit mode

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A21	Data Inputs/Outputs DQ15-DQ0
Block (Group) Protect(1)	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12-A21 Block Address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A6 = V_{IH}, A9 = V_{ID}, A12 = V_{IH}, A15 = V_{IH} Others =X	X
Block (Group) Protect Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A2 = V_{IL}, A3 = V_{IL}, A6 = V_{IL}, A9 = V_{ID}, A12- 21 Block Address, Others = X	Pass = xx01h Retry = xx00h.
Block (Group) Unprotect Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A2 = V_{IL}, A3 = V_{IL}, A6 = V_{IH}, A9 = V_{ID}, A12-A21 Block Address Others = X	Pass = xx00h Retry = xx01h.

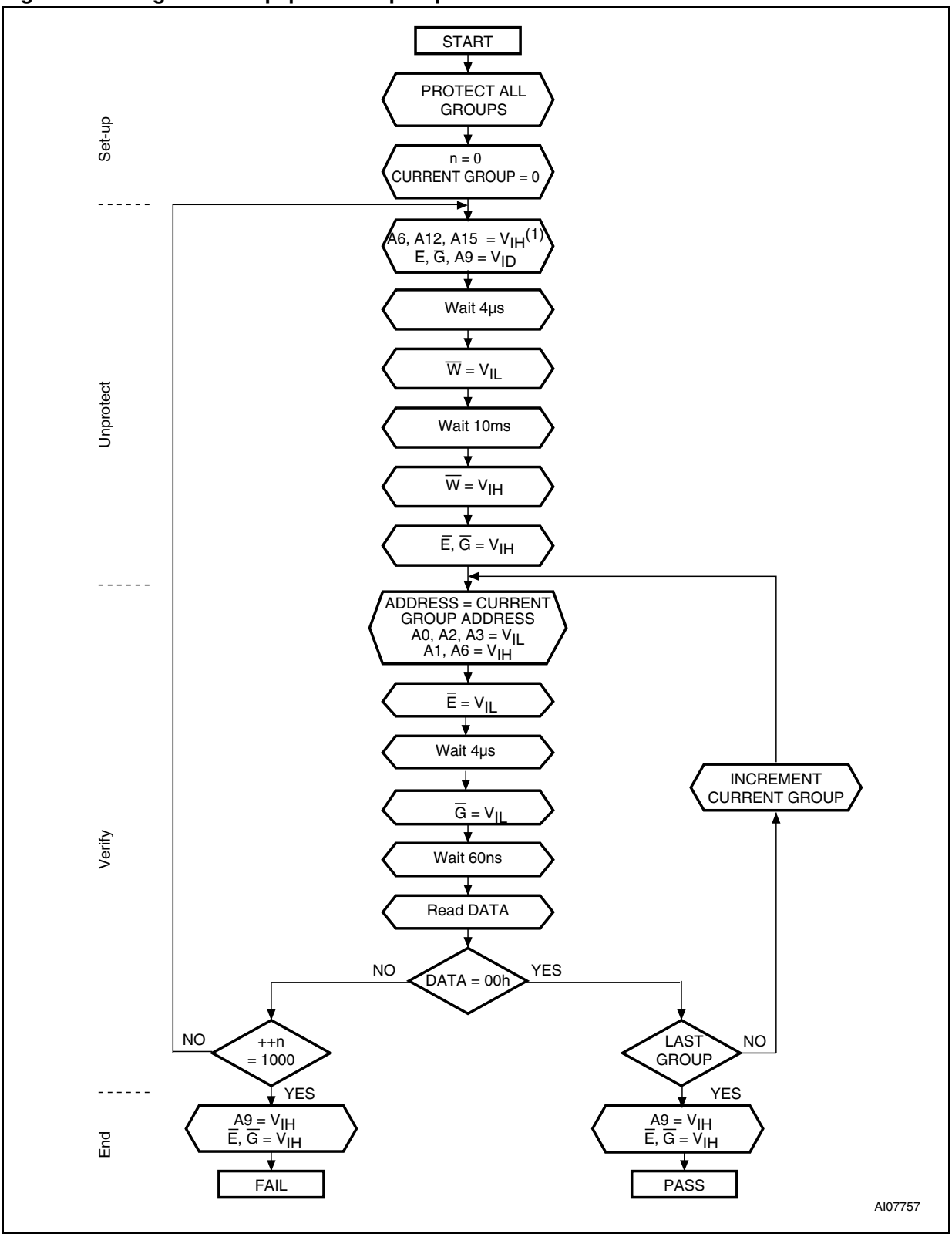
1. Block Protection Groups are shown in *Appendix D*, *Table 28*.

Figure 22. Programmer equipment Group Protect flowchart



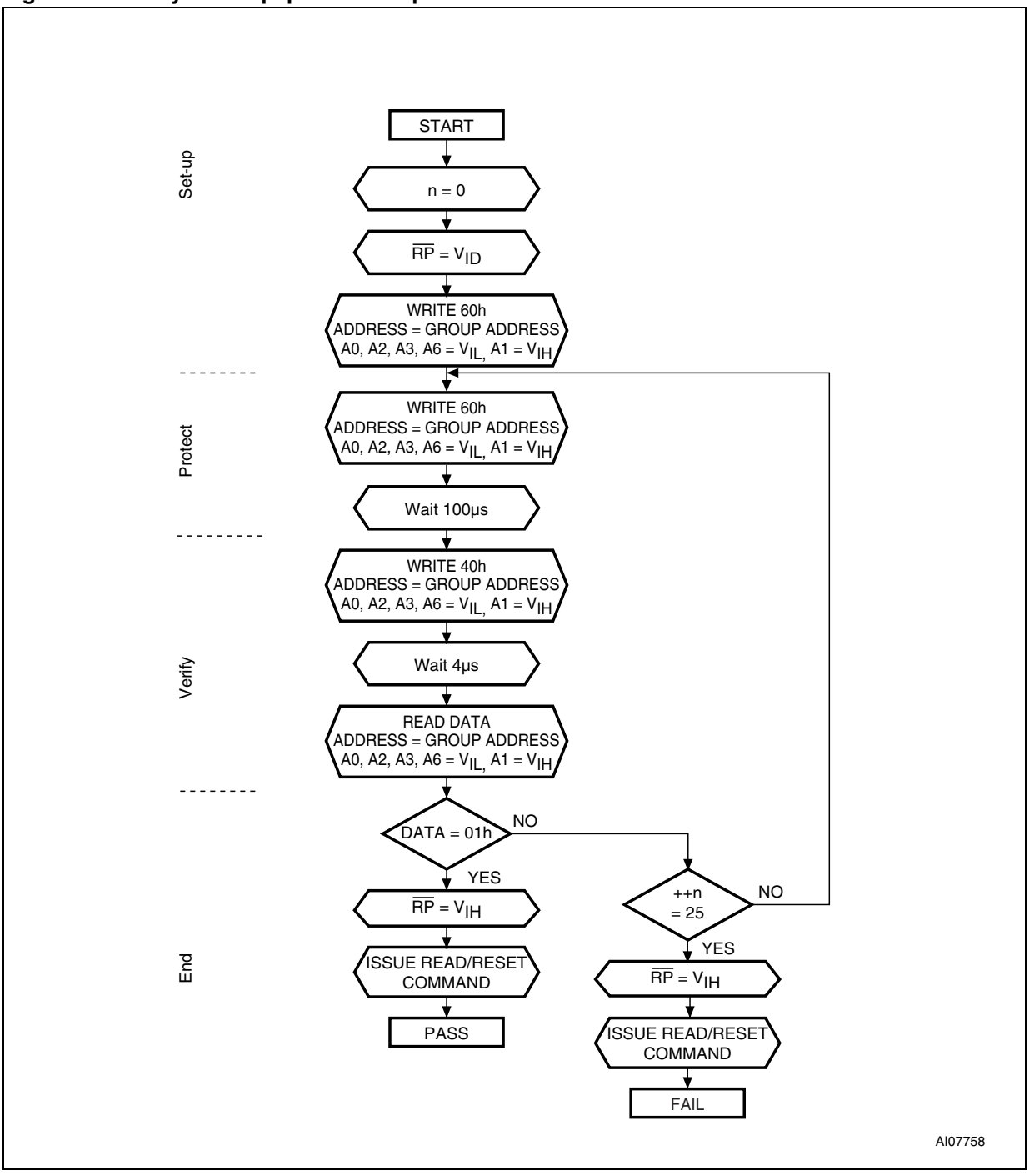
1. Block Protection Groups are shown in *Appendix D*, *Table 28*.

Figure 23. Programmer equipment Chip Unprotect flowchart



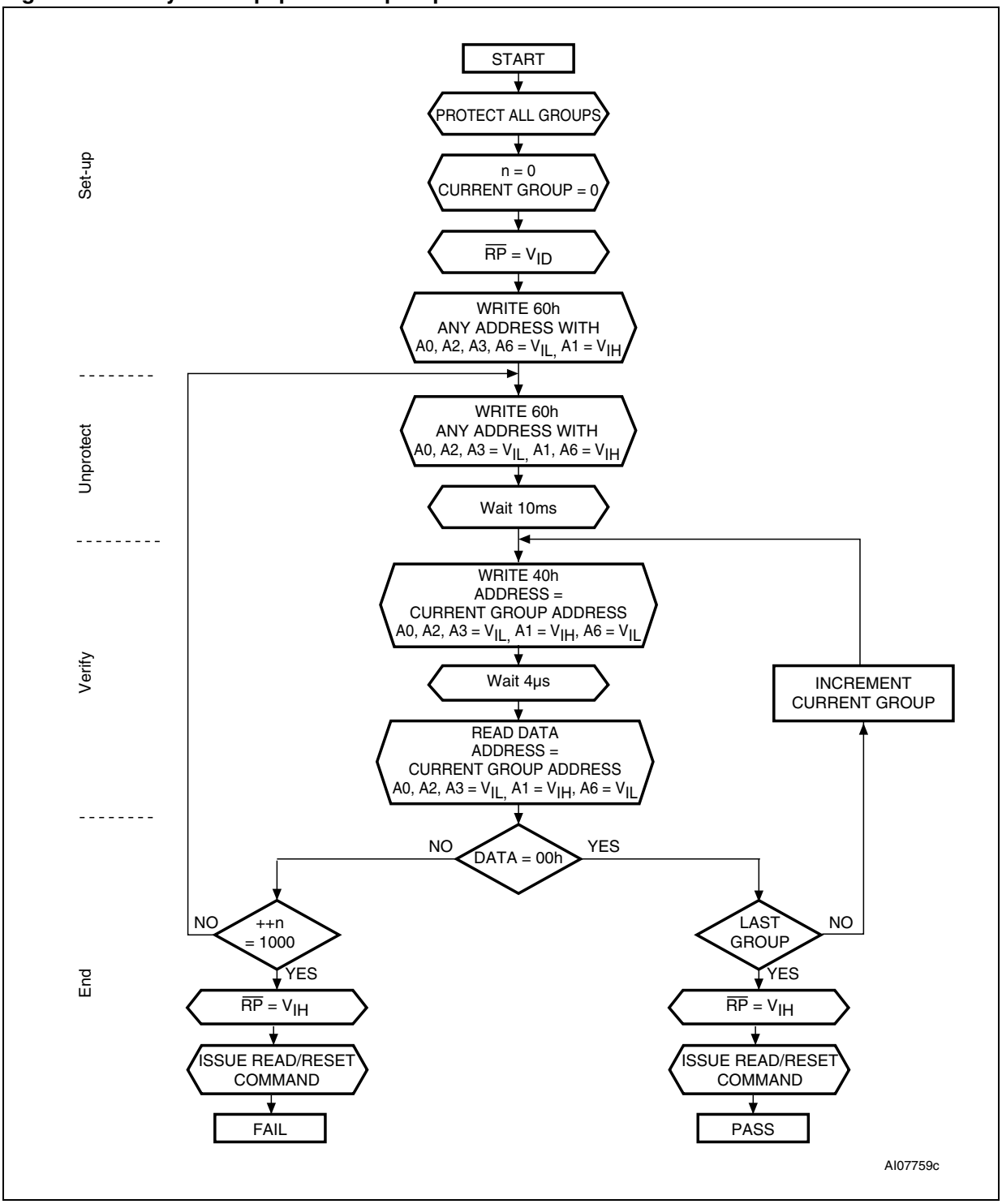
1. Block Protection Groups are shown in *Appendix D*, *Table 28*.

Figure 24. In-System equipment Group Protect flowchart



1. Block Protection Groups are shown in *Appendix D*, *Table 28*.
2. $\overline{RP}$ can be either at V_{IH} or at V_{ID} when using the In-System Technique to protect the Extended Block.

Figure 25. In-System equipment Chip Unprotect flowchart



1. Block Protection Groups are shown in *Appendix D*, *Table 28*.

Revision history

Table 37. Document revision history

Date	Revision	Changes
02-Dec-2005	1	First issue.
10-Mar-2006	2	DQ7 changed to $\overline{DQ7}$ for Program, Program During Erase Suspend and Program Error in *Table 13: Status Register bits*. Converted to new template. Updated address values in *Table 35: Extended Block Address and Data*.
19-Jun-2006	3	Small text changes. NVMP address corrected in *Table 11: Protection command addresses*.
24-Nov-2006	4	Updated R$\overline{B}$ for Program Error and Erase Error in *Table 13: Status Register bits*; updated package mechanical data for TSOP48 package in *Section 11*.
10-Dec-2007	5	Applied Numonyx branding.

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