THE DATASHEET OF

HMC1114PM5E

>10 W (42 dBm), 2.7 GHz to 3.8 GHz, GaN Power Amplifier

Data Sheet

HMC1114PM5E

FEATURES

- High small signal gain: 34.5 dB typical
- High output power: 42 dBm typical at P_{IN} = 18 dBm
- High PAE: 55% typical at P_{IN} = 18 dBm
- Frequency range: 2.7 GHz to 3.8 GHz
- Supply voltage: V_{DD} = 28 V at a quiescent current of 150 mA
- 5 mm × 5 mm, 32-lead LFCSP_CAV package

APPLICATIONS

- Extended battery operation for public mobile radios
- Power amplifier stage for wireless infrastructures
- Test and measurement equipment
- Commercial and military radars
- General-purpose transmitter amplification

FUNCTIONAL BLOCK DIAGRAM

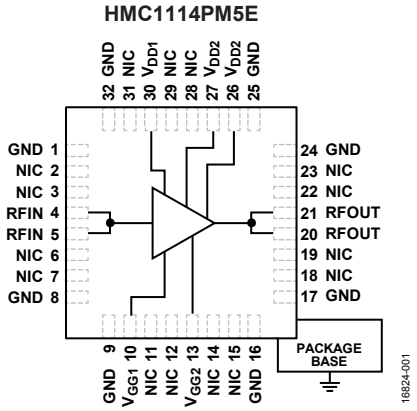

Figure 1.

GENERAL DESCRIPTION

The HMC1114PM5E is a gallium nitride (GaN), broadband power amplifier delivering >10 W (up to 42 dBm) typical with up to 55% power added efficiency (PAE) across an instantaneous bandwidth range of 2.7 GHz to 3.8 GHz, at an input power (P_{IN}) of 18 dBm. The gain flatness is <1 dB typical at small signal levels.

The HMC1114PM5E is ideal for pulsed or continuous wave (CW) applications, such as wireless infrastructure, radars, public mobile radios, and general-purpose amplification.

Rev. 0

Document Feedback

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REVISION HISTORY

9/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, supply voltage (V_{DD}) = 28 V, quiescent current (I_{DDQ}) = 150 mA, and frequency range = 2.7 GHz to 3.2 GHz, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		2.7		3.2	GHz	
GAIN						
Small Signal Gain		31	34.5		dB	
Gain Flatness			0.8		dB	
RETURN LOSS						
Input			12		dB	
Output			7.5		dB	
POWER						
Output Power	P_{OUT}		42		dBm	P_{IN} = 16 dBm
			42		dBm	P_{IN} = 18 dBm
Power Gain			25.5		dB	P_{IN} = 16 dBm
			25.5		dB	P_{IN} = 18 dBm
Power Added Efficiency	PAE		47.5		%	P_{IN} = 16 dBm
			47.5		%	P_{IN} = 18 dBm
OUTPUT THIRD-ORDER INTERCEPT	IP3		42.5		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE	NF		5.5		dB	
QUIESCENT CURRENT	I_{DDQ}		150		mA	Adjust the gate bias control voltage (V_{GG}) from −5 V to 0 V to achieve I_{DDQ} = 150 mA, V_{GG} = −2.78 V typical to achieve I_{DDQ} = 150 mA
SUPPLY VOLTAGE	V_{DD}	24	28	32	V	

T_A = 25°C, V_{DD} = 28 V, I_{DDQ} = 150 mA, and frequency range = 3.2 GHz to 3.8 GHz, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		3.2		3.8	GHz	
GAIN						
Small Signal Gain		30	33.5		dB	
Gain Flatness			1		dB	
RETURN LOSS						
Input			18		dB	
Output			10		dB	
POWER						
Output Power	P_{OUT}		41.5		dBm	P_{IN} = 16 dBm
			41.5		dBm	P_{IN} = 18 dBm
Power Gain			24		dB	P_{IN} = 16 dBm
			23.5		dB	P_{IN} = 18 dBm
Power Added Efficiency	PAE		52		%	P_{IN} = 16 dBm
			55		%	P_{IN} = 18 dBm
OUTPUT THIRD-ORDER INTERCEPT	IP3		44		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE	NF		5		dB	
QUIESCENT CURRENT	I_{DDQ}		150		mA	Adjust V_{GG} from −5 V to 0 V to achieve I_{DDQ} = 150 mA, V_{GG} = −2.78 V typical to achieve I_{DDQ} = 150 mA
SUPPLY VOLTAGE	V_{DD}	24	28	32	V	

TOTAL SUPPLY CURRENT BY V_{DD}

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
QUIESCENT CURRENT	I_{DDQ}					Adjust V_{GG} between −5 V and 0 V to achieve I_{DDQ} = 150 mA typical
			150		mA	V_{DD} = 24 V
			150		mA	V_{DD} = 28 V
			150		mA	V_{DD} = 32 V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	35 V
V_{GG}	−8 V to 0 V dc
Radio Frequency Input (RFIN) Power	30 dBm
Maximum Voltage Standing Wave Ratio (VSWR)[1]	6:1
Channel Temperature	225°C
Maximum Peak Reflow Temperature (Moisture Sensitivity Level 3 (MSL3))[2]	260°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 182 mW/°C Above 85°C)	25.5 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	Class 1A, passed 250 V

[1] Restricted by maximum power dissipation.
[2] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

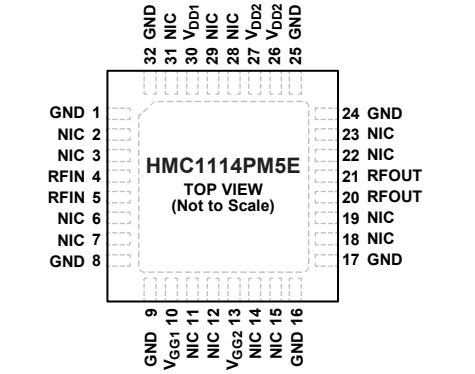
Package Type	θ_{JC}[1]	Unit
CG-32-2	5.5	°C/W

[1] Thermal resistance (θ_{JC}) was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground paddle, to the PCB, and the ground paddle is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, ALL DATA IS MEASURED WITH THESE PINS CONNECTED TO RF AND DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 17, 24, 25, 32	GND	Ground. These pins must be connected to RF and dc ground. See Figure 3 for the GND interface schematic.
2, 3, 6, 7, 11, 12, 14, 15, 18, 19, 22, 23, 28, 29, 31	NIC	Not Internally Connected. These pins are not connected internally. However, all data is measured with these pins connected to RF and dc ground externally.
4, 5	RFIN	RF Input. These pins are ac-coupled and matched to 50 Ω. See Figure 4 for the RFIN interface schematic.
10, 13	V_{GG1}, V_{GG2}	Gate Control Voltage Pins. External bypass capacitors of 1 µF and 10 µF are required. See Figure 5 for the V_{GG1} and V_{GG2} interface schematic.
20, 21	RFOUT	RF Output. These pins are ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.
26, 27, 30	V_{DD1}, V_{DD2}	Drain Bias Pins for the Amplifier. External bypass capacitors of 1000 pF, 1 µF, and 10 µF are required. See Figure 7 for the V_{DD1} and V_{DD2} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface

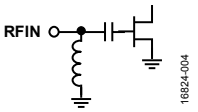


Figure 4. RFIN Interface

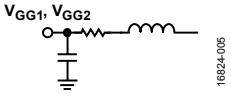


Figure 5. V_{GG1} and V_{GG2} Interface

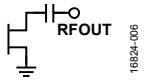


Figure 6. RFOUT Interface

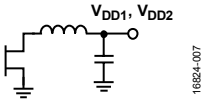


Figure 7. V_{DD1} and V_{DD2} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

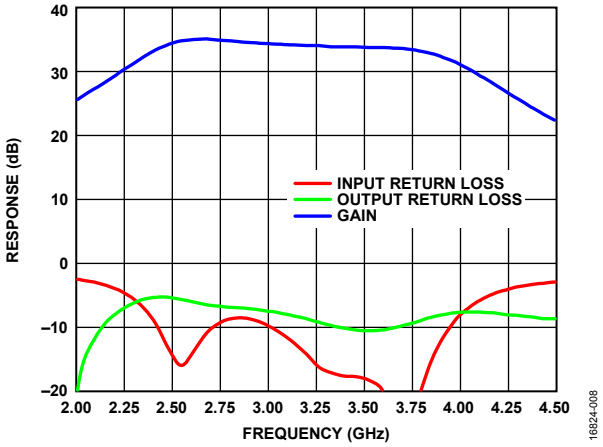


Figure 8. Broadband Small Signal Gain and Return Loss (Response) vs. Frequency

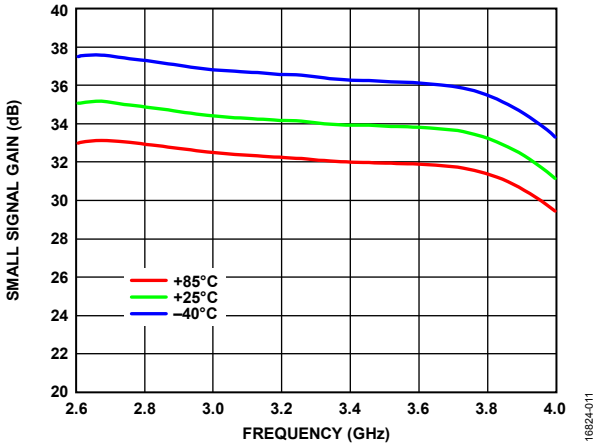


Figure 11. Small Signal Gain vs. Frequency at Various Temperatures

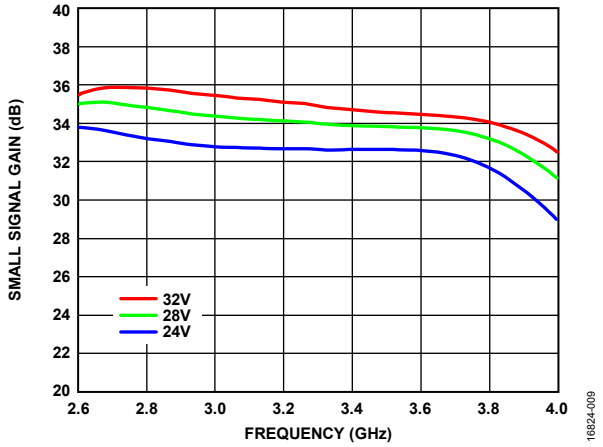


Figure 9. Small Signal Gain vs. Frequency at Various Supply Voltages

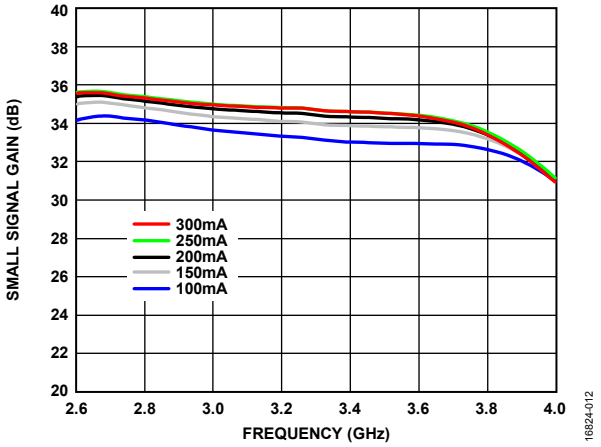


Figure 12. Small Signal Gain vs. Frequency at Various Quiescent Currents

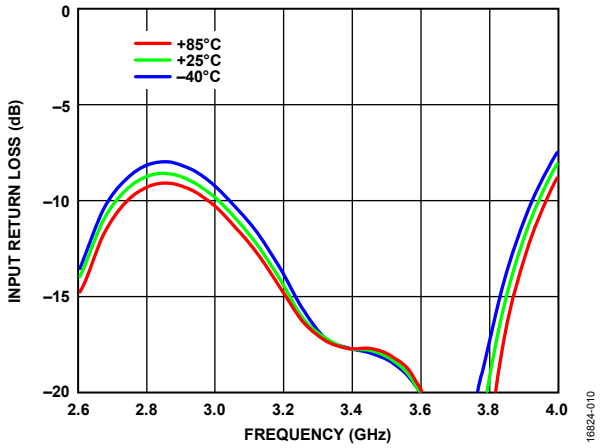


Figure 10. Input Return Loss vs. Frequency at Various Temperatures

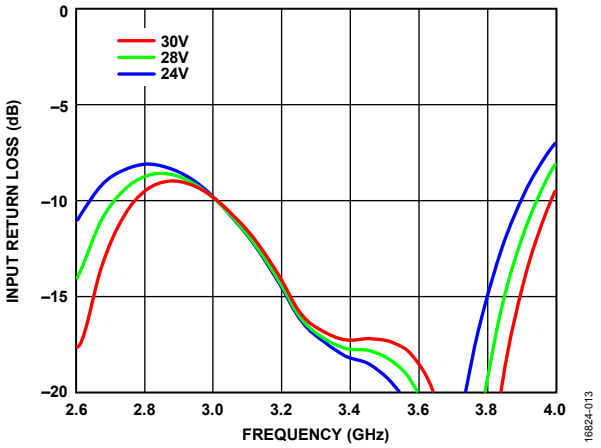


Figure 13. Input Return Loss vs. Frequency at Various Supply Voltages

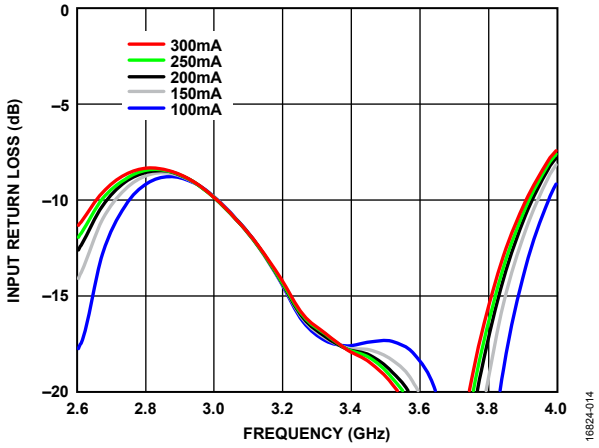


Figure 14. Input Return Loss vs. Frequency at Various Quiescent Currents

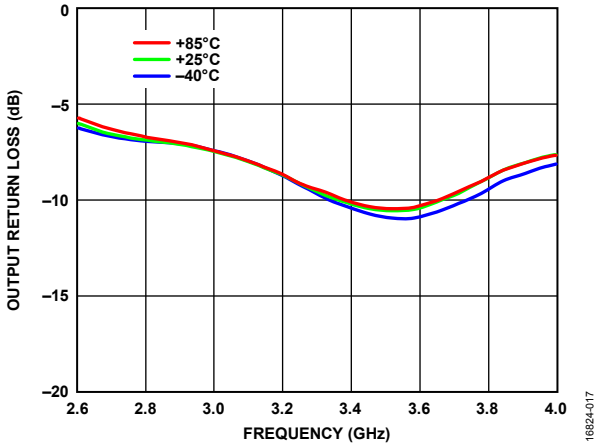


Figure 17. Output Return Loss vs. Frequency at Various Temperatures

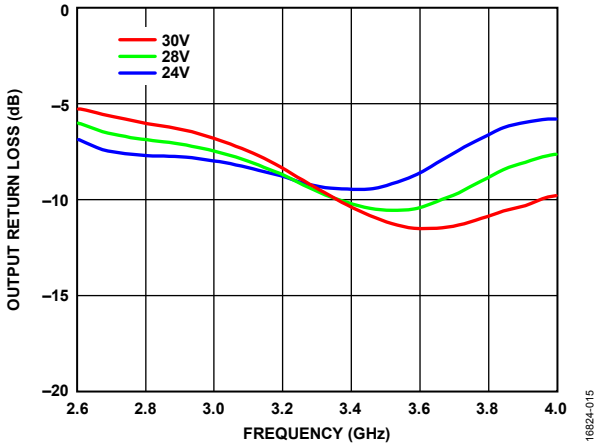


Figure 15. Output Return Loss vs. Frequency at Various Supply Voltages

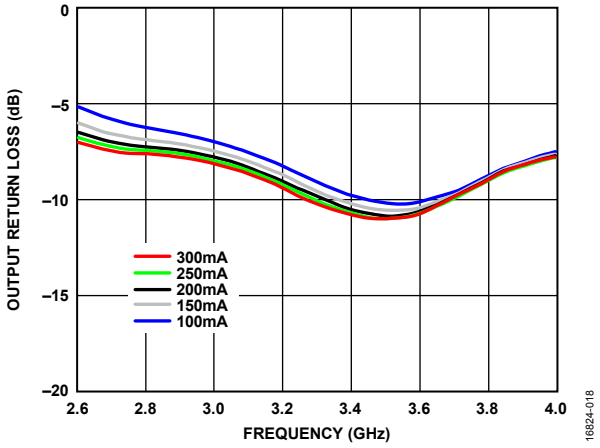


Figure 18. Output Return Loss vs. Frequency at Various Quiescent Currents

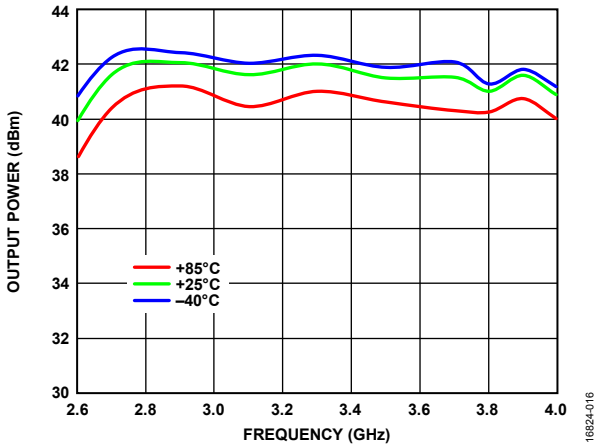


Figure 16. Output Power vs. Frequency at Various Temperatures, Input Power = 16 dBm

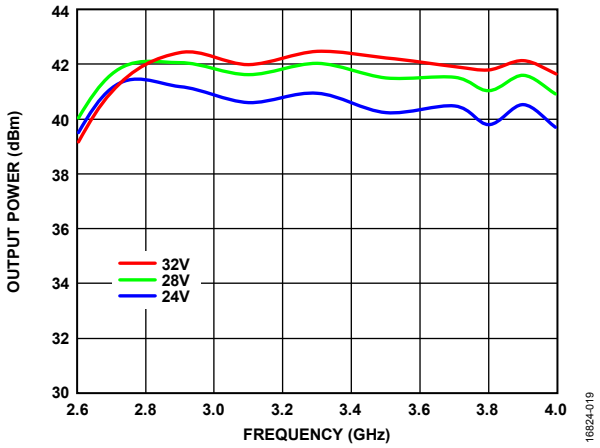


Figure 19. Output Power vs. Frequency at Various Supply Voltages, Input Power = 16 dBm

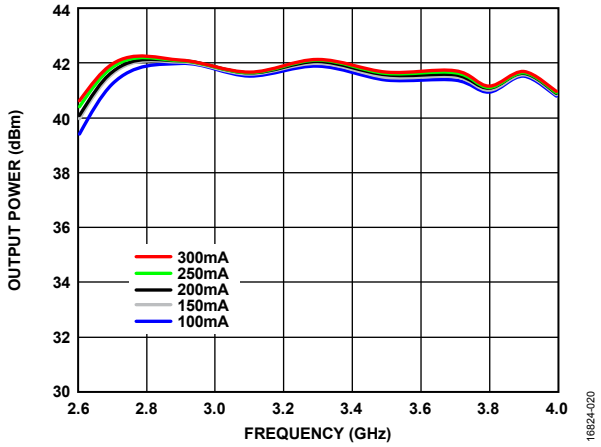


Figure 20. Output Power vs. Frequency at Various Quiescent Currents, Input Power = 16 dBm

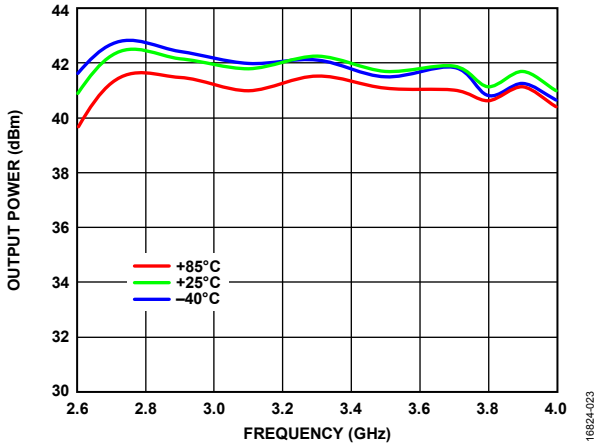


Figure 23. Output Power vs. Frequency at Various Temperatures, Input Power = 18 dBm

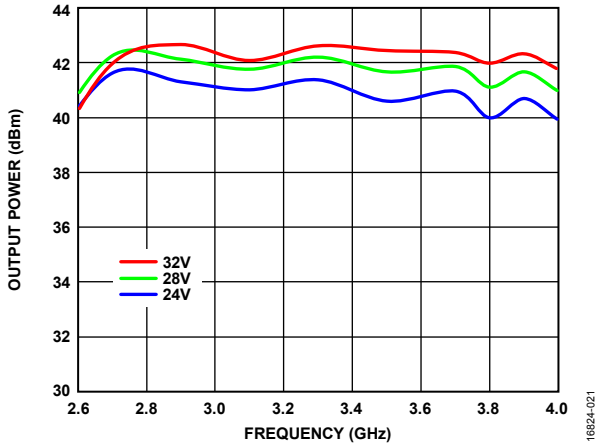


Figure 21. Output Power vs. Frequency at Various Supply Voltages, Input Power = 18 dBm

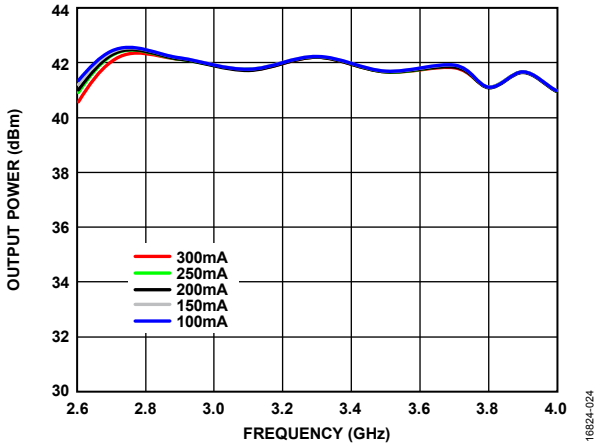


Figure 24. Output Power vs. Frequency at Various Quiescent Currents, Input Power = 18 dBm

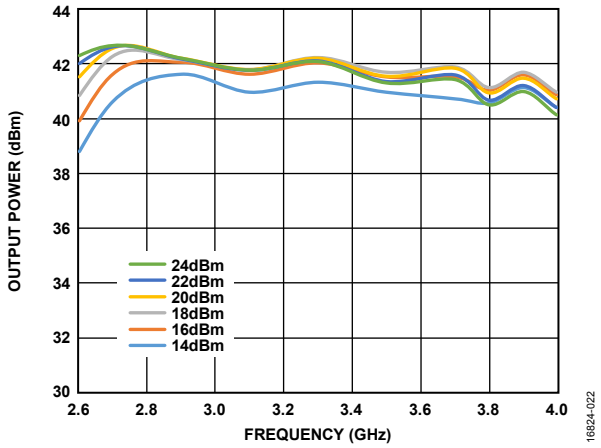


Figure 22. Output Power vs. Frequency at Various Input Powers

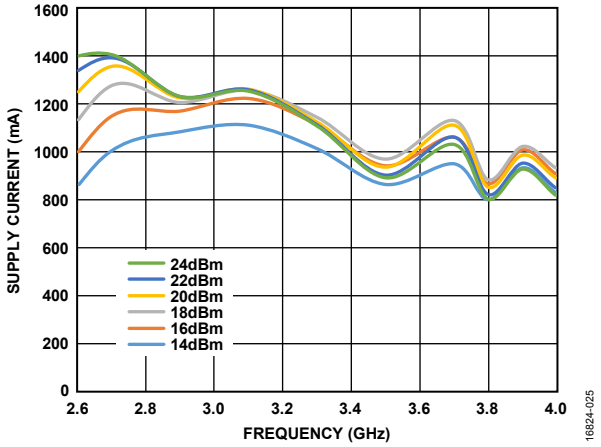


Figure 25. Supply Current vs. Frequency at Various Input Powers

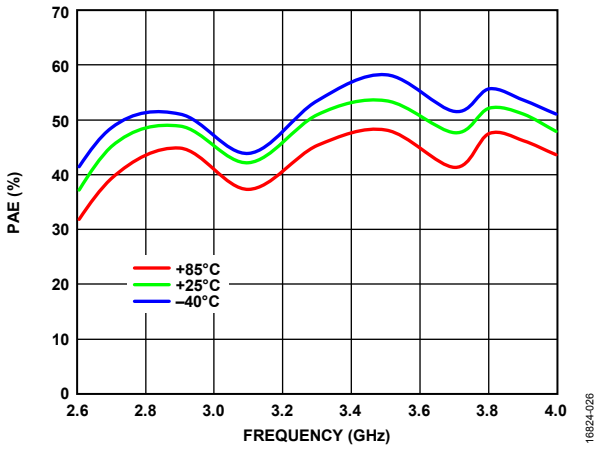


Figure 26. PAE vs. Frequency at Various Temperatures, Input Power = 16 dBm

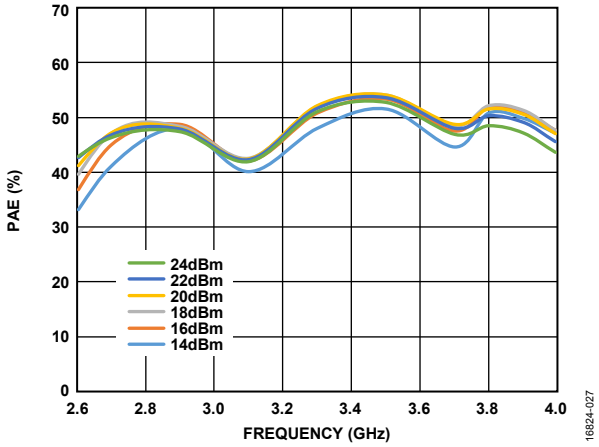


Figure 27. PAE vs. Frequency at Various Input Powers

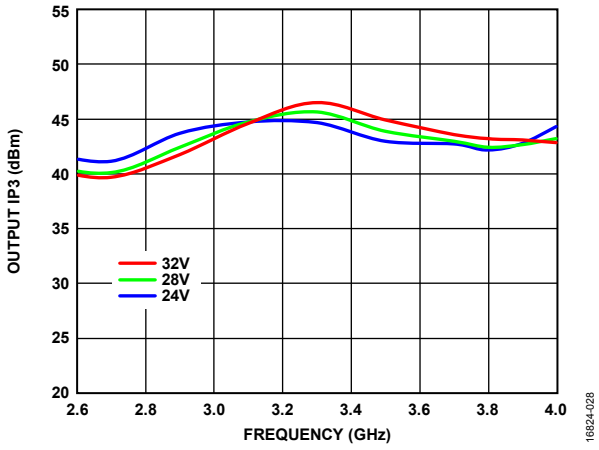


Figure 28. Output IP3 vs. Frequency at Various Supply Voltages, P_{OUT} per Tone = 30 dBm

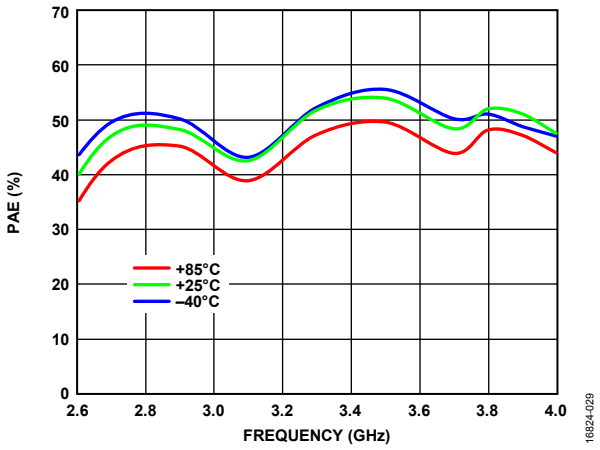


Figure 29. PAE vs. Frequency at Various Temperatures, Input Power = 18 dBm

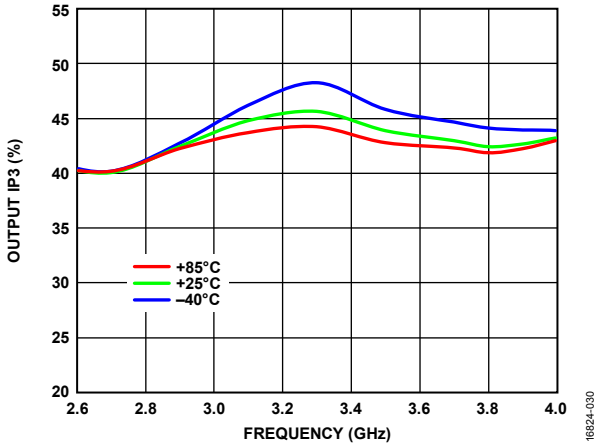


Figure 30. Output IP3 vs. Frequency at Various Temperatures, P_{OUT} per Tone = 30 dBm

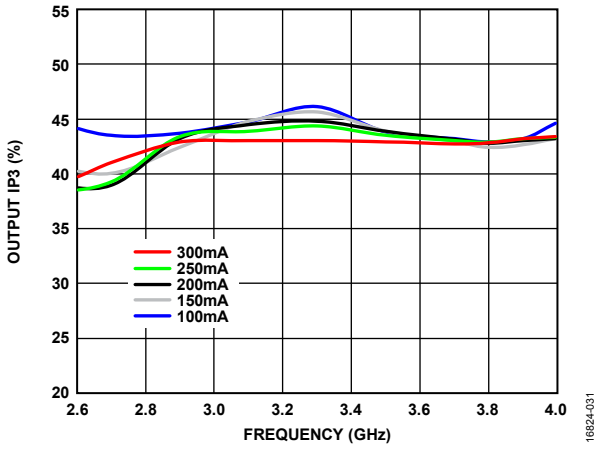


Figure 31. Output IP3 vs. Frequency at Various Quiescent Currents, P_{OUT} per Tone = 30 dBm

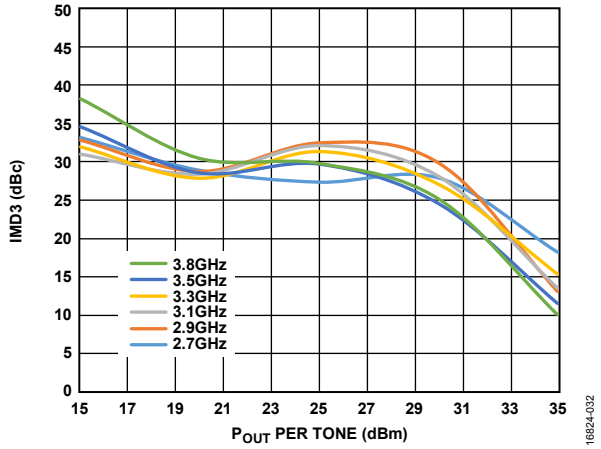


Figure 32. Output Third-Order Intermodulation (IMD3) vs. P_{OUT} per Tone, V_{DD} = 24 V

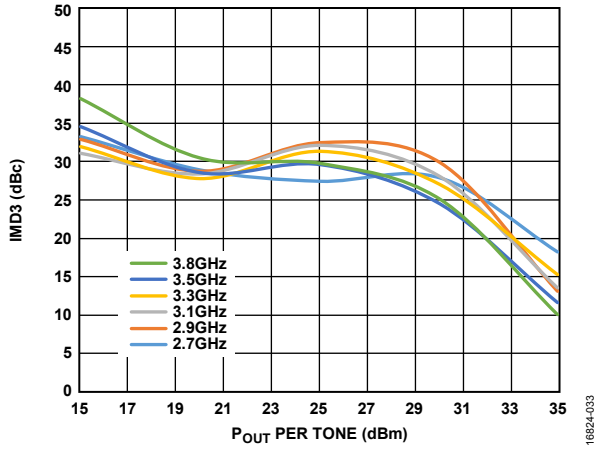


Figure 33. IMD3 vs. P_{OUT} per Tone, V_{DD} = 32 V

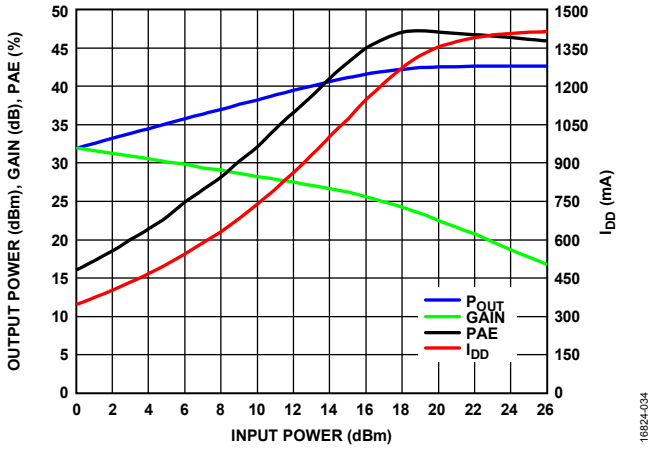


Figure 34. Output Power, Gain, PAE, and Total Supply Current (I_{DD}) vs. Input Power at 2.7 GHz

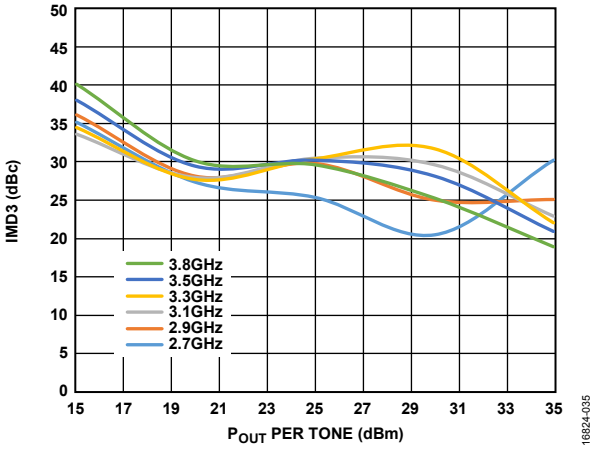


Figure 35. IMD3 vs. P_{OUT} per Tone, V_{DD} = 28 V

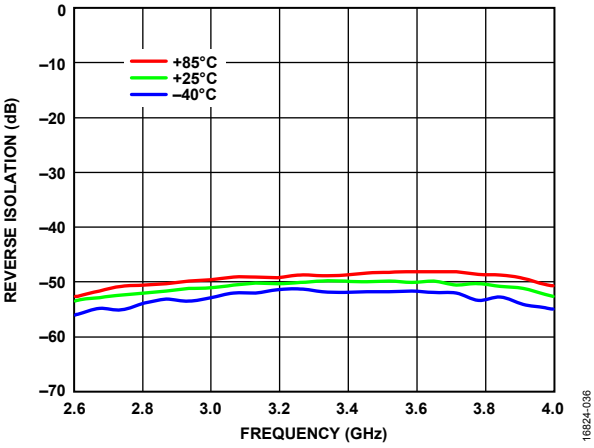


Figure 36. Reverse Isolation vs. Frequency at Various Temperatures

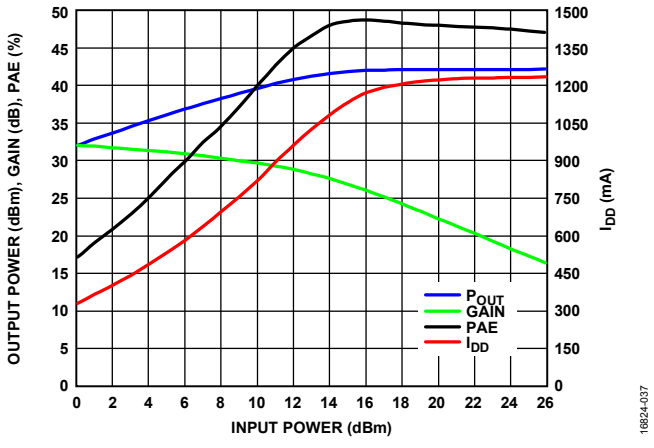


Figure 37. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 2.9 GHz

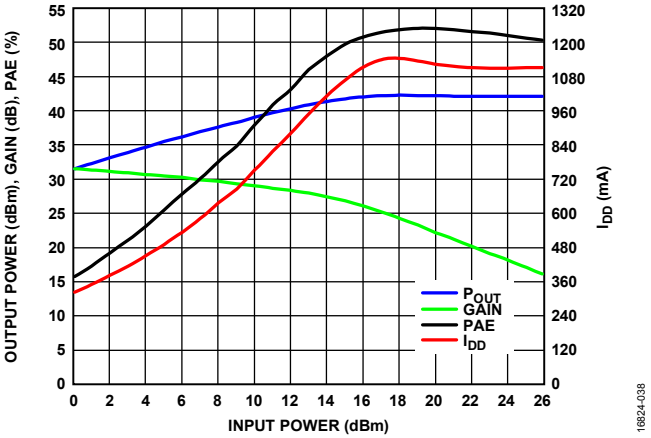


Figure 38. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 3.3 GHz

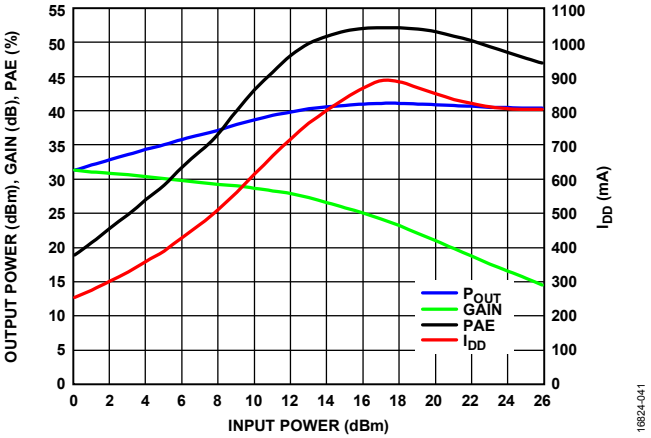


Figure 41. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 3.8 GHz

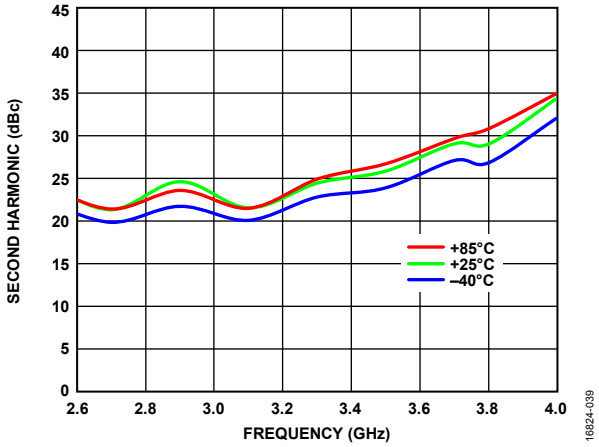


Figure 39. Second Harmonic vs. Frequency at Various Temperatures, P_{OUT} = 30 dBm

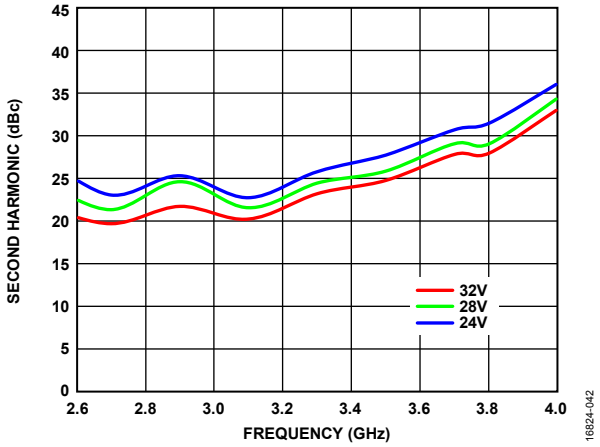


Figure 42. Second Harmonic vs. Frequency at Various Supply Voltages, P_{OUT} = 30 dBm

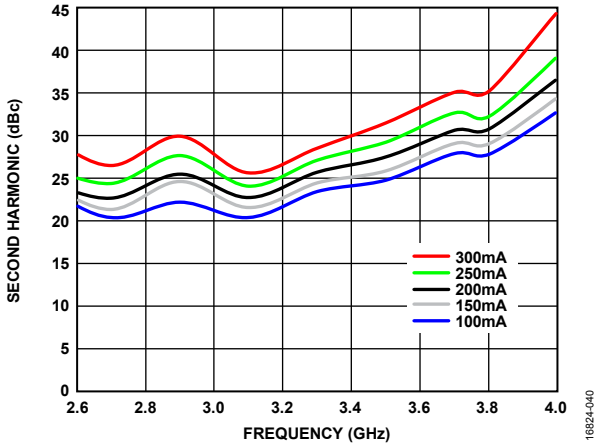


Figure 40. Second Harmonic vs. Frequency at Various Quiescent Currents, P_{OUT} = 30 dBm

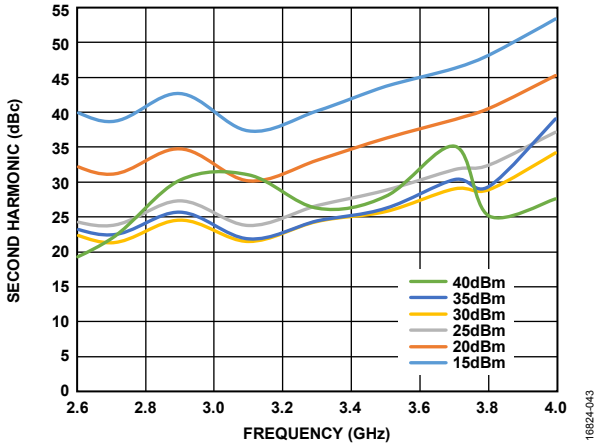


Figure 43. Second Harmonic vs. Frequency at Various Output Powers,

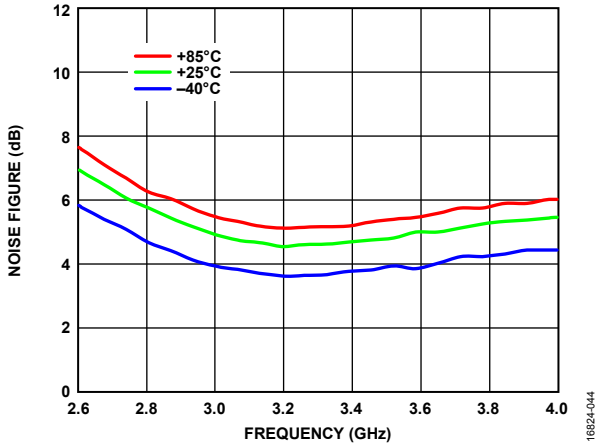


Figure 44. Noise Figure vs. Frequency at Various Temperatures

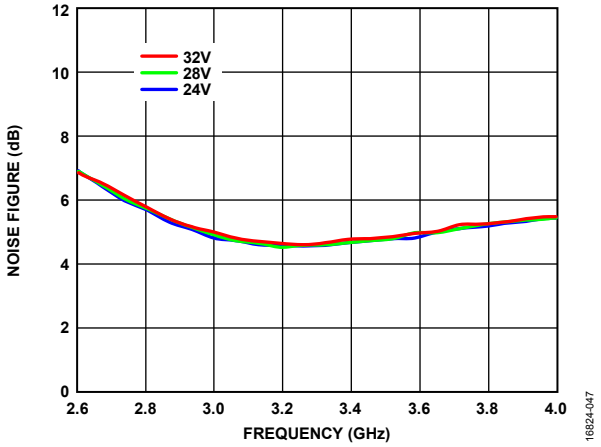


Figure 47. Noise Figure vs. Frequency at Various Supply Voltages

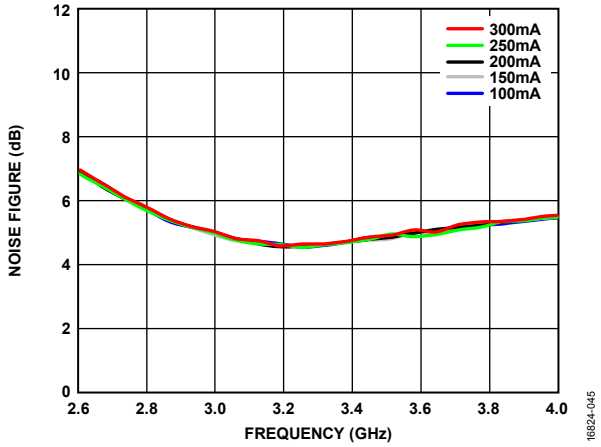


Figure 45. Noise Figure vs. Frequency at Various Quiescent Currents

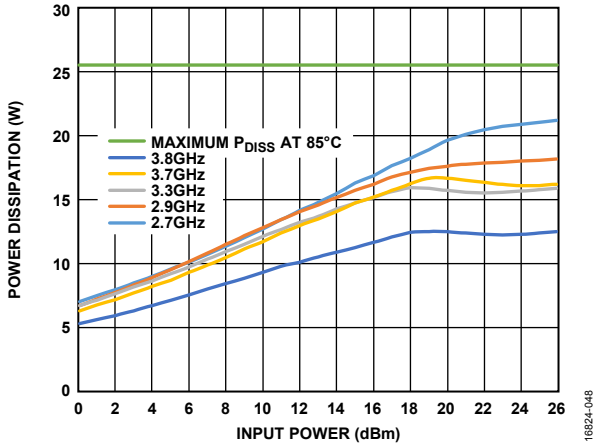


Figure 48. Power Dissipation vs. Input Power at Various Frequencies, T_A = 85°C

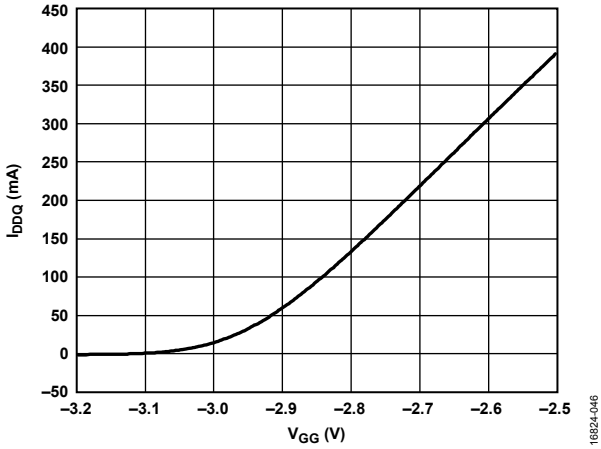


Figure 46. I_{DDQ} vs. V_{GG} at V_{DD} = 28 V, Representative of a Typical Device

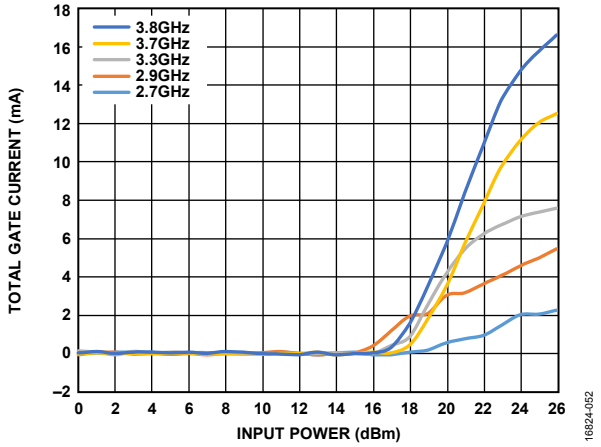


Figure 49. Total Gate Current vs. Input Power at Various Frequencies, V_{DD} = 28 V

THEORY OF OPERATION

The HMC1114PM5E is a >10 W (42 dBm), GaN, power amplifier that consists of two gain stages in series. The basic block diagram for the amplifier is shown in Figure 50.

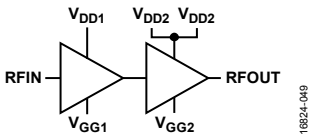


Figure 50. Basic Block Diagram

The recommended dc bias conditions put the device in Class AB operation, resulting in high P_{OUT} (42 dBm typical) at improved levels of PAE (<55% typical). The voltage applied to the V_{GG1} and V_{GG2} pads sets the gate bias of the field effect transistors (FETs), providing control of the drain current. For this reason, the application of a bias voltage to the V_{GG1} and V_{GG2} pads is required and not optional.

The HMC1114PM5E has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the 2.7 GHz to 3.8 GHz frequency range. Consequently, the device can directly insert into a 50 Ω system with no required impedance matching circuitry, which also means that multiple HMC1114PM5E amplifiers can be cascaded back to back without the need for external matching circuitry. The input and output impedances are sufficiently stable across variations in temperature and supply voltage so that no impedance matching compensation is required.

Note that it is critical to supply low inductance ground connections to the GND pins and the package base exposed pad to ensure stable operation. To achieve optimal performance from the HMC1114PM5E and prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Figure 51 shows the basic connections for operating the HMC1114PM5E. The RFIN port is dc-coupled. An appropriate valued external dc block capacitor is required at the RFIN port. The RFOUT port has on-chip dc block capacitors that eliminate the need for external ac coupling capacitors.

RECOMMENDED BIAS SEQUENCE

During Power-Up

The recommended bias sequence during power-up is the following:

1. Connect the power supply ground to the circuit ground (GND).
2. Set V_{GG1} and V_{GG2} to −8 V.
3. Set V_{DD1} and V_{DD2} to 28 V.
4. Increase V_{GG1} and V_{GG2} to achieve a typical I_{DDQ} = 150 mA.
5. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down is the following:

1. Turn off the RF signal.
2. Decrease V_{GG1} to −8 V to achieve a typical I_{DDQ} = 0 mA.
3. Decrease V_{DD1} and V_{DD2} to 0 V.
4. Increase V_{GG1} to 0 V.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 51) on the evaluation board (see Figure 52) and biased per the conditions in the Recommended Bias Sequence section. The V_{DD1} and two V_{DD2} pins are connected together. Similarly, the V_{GG1} and V_{GG2} pins are also connected together. The bias conditions shown in the Recommended Bias Sequence section are the operating points recommended to optimize the overall performance. Operating using other bias conditions may provide performance that differs from what is in Table 1 and Table 2. Increasing the V_{DD1} and V_{DD2} levels typically increase gain and P_{OUT} at the expense of power consumption. This behavior is seen in the Typical Performance Characteristics section. For applications where the P_{SAT} requirement is not stringent, reduce the V_{DD1} and the V_{DD2} of the HMC1114PM5E to improve power consumption. To obtain the best performance while not damaging the device, follow the recommended biasing sequence outlined in the Recommended Bias Sequence section.

TYPICAL APPLICATION CIRCUIT

Figure 51 shows the typical application circuit.

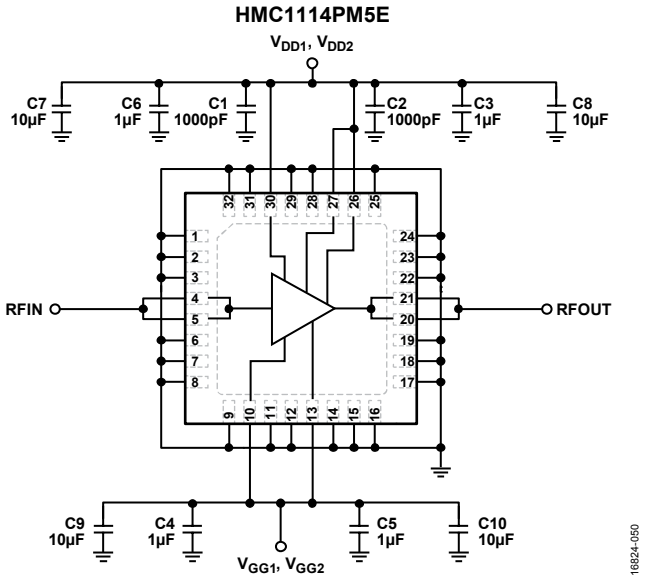


Figure 51. Typical Application Circuit

EVALUATION PCB

The EV1HMC1114PM5 (08-047732) evaluation PCB is shown in Figure 52.

Use RF circuit design techniques for the circuit board used in the application. Provide 50 Ω impedance for the signal lines and directly connect the package ground leads and exposed pad to the ground plane, similar to that shown in Figure 52. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation PCB shown in Figure 52 is available from Analog Devices, Inc., upon request.

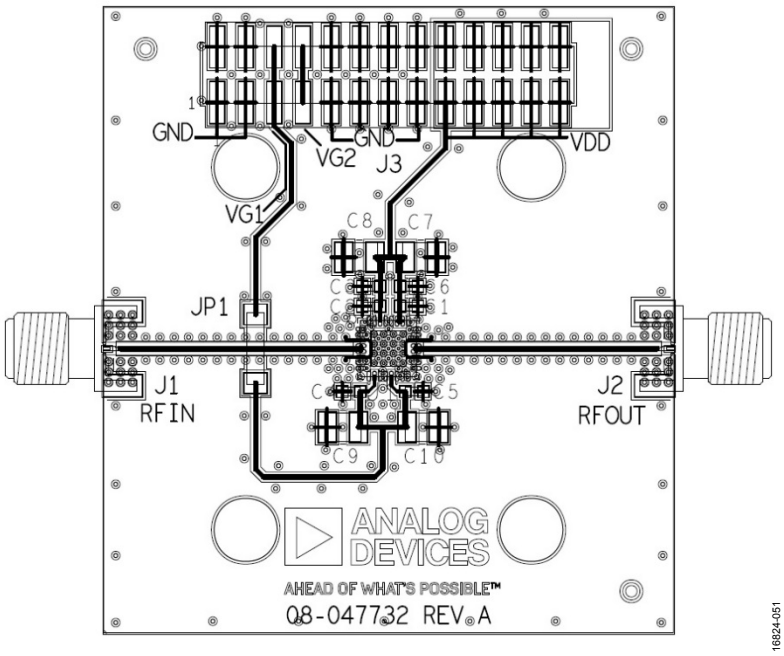


Figure 52. EV1HMC1114PM5 (08-047732) Evaluation Board PCB

Table 7. Bill of Materials for the EV1HMC1114PM5 Evaluation Board PCB

Item	Description
J1, J2	25-146-1000-92
J3	DC pins
JP1	Preform jumper
C1, C2	1000 pF capacitors, 0603 package
C3 to C6	1 µF capacitors, 0603 package
C7 to C10	10 µF capacitors, 1210 package
U1	HMC1114PM5E amplifier
PCB	08-047732, Revision A evaluation PCB; circuit board material: Rogers 4350 or Arlon 25FR
Heat sink	Used for thermal transfer from the HMC1114PM5E amplifier

OUTLINE DIMENSIONS

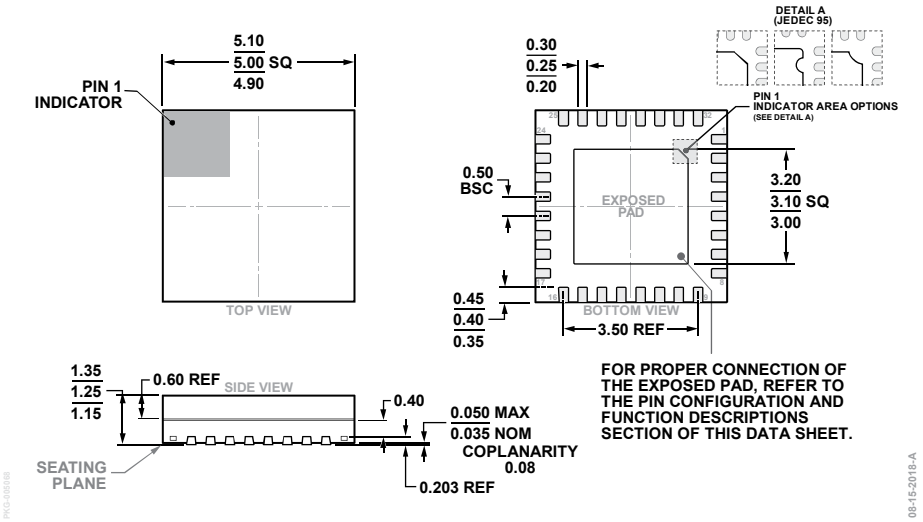


Figure 53. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	MSL Rating[3]	Package Description[4]	Package Option
HMC1114PM5E	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
HMC1114PM5ETR	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
EV1HMC1114PM5			Evaluation Board	

[1] All models are RoHS compliant parts.
[2] When ordering the evaluation board, use the reference model number EV1HMC1114PM5.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC1114PM5E and the HMC1114PM5ETR is nickel palladium gold (NiPdAu).

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