



**THE DATASHEET OF
HMC1099PM5ETR**



FEATURES

- High small signal gain: 20 dB typical**
- P_{OUT} : 41.5 dBm typical at $P_{IN} = 27$ dBm**
- High PAE: 60% typical at $P_{IN} = 27$ dBm**
- Instantaneous bandwidth: 0.01 GHz to 1.1 GHz across all frequencies**
- Supply voltage: $V_{DD} = 28$ V at a quiescent current of 100 mA**
- Internal prematching**
 - Simple and compact external tuning for optimal performance
- 5 mm × 5 mm, 32-lead LFCSP**

APPLICATIONS

- Extended battery operation for public mobile radios
- Power amplifier stage for wireless infrastructures
- Test and measurement equipment
- Commercial and military radars
- General-purpose transmitter amplification

GENERAL DESCRIPTION

The HMC1099PM5E is a gallium nitride (GaN), broadband power amplifier that delivers 10 W (40 dBm) with up to 60% power added efficiency (PAE) across an instantaneous bandwidth of 0.01 GHz to 1.1 GHz, at an input power (P_{IN}) of 27 dBm. The gain flatness is between 0.5 dB to 2 dB typical at small signal levels.

FUNCTIONAL BLOCK DIAGRAM

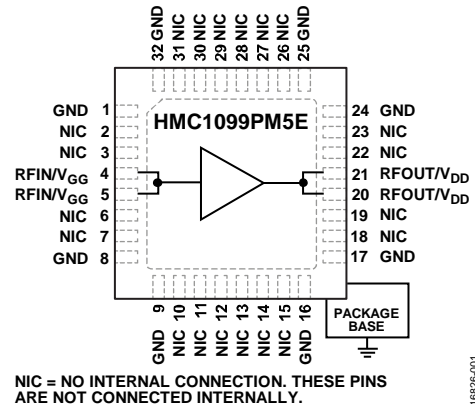


Figure 1.

The HMC1099PM5E is ideal for pulsed or continuous wave (CW) applications, such as wireless infrastructure, radars, public mobile radios, and general-purpose amplification.

The HMC1099PM5E amplifier is externally tuned using low cost, surface-mount components and is available in a compact LFCSP.

Multifunction pin names may be referenced by their relevant function only.

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REVISION HISTORY

9/2018—Rev. A to Rev. B

Change to Storage Temperature Range Parameter, Table 5 5

8/2018—Rev. 0 to Rev. A

Changes to Figure 34..... 11

Changes to Figure 35 and Figure 36..... 12

8/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{DD} = 28\text{ V}$, quiescent current (I_{DDQ}) = 100 mA, and frequency range = 0.01 GHz to 0.4 GHz unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		0.4	GHz	
GAIN						
Small Signal Gain		18	20		dB	
Gain Flatness			2		dB	
RETURN LOSS						
Input			12		dB	
Output			15		dB	
POWER						
Output Power	P_{OUT}		40		dBm	Input power (P_{IN}) = 25 dBm
			41		dBm	$P_{IN} = 27\text{ dBm}$
Power Added Efficiency	PAE		55		%	$P_{IN} = 25\text{ dBm}$
			60		%	$P_{IN} = 27\text{ dBm}$
OUTPUT THIRD-ORDER INTERCEPT	OIP3		50		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE			8		dB	
SUPPLY VOLTAGE	V_{DD}	24	28	30	V	
QUIESCENT CURRENT	I_{DDQ}		100		mA	Adjust the gate bias control voltage (V_{GG}) from -5 V to 0 V to achieve $I_{DDQ} = 100\text{ mA}$, $V_{GG} = -2.9\text{ V}$ typical to achieve $I_{DDQ} = 100\text{ mA}$

$T_A = 25^\circ\text{C}$, $V_{DD} = 28\text{ V}$, $I_{DDQ} = 100\text{ mA}$, and frequency range = 0.4 GHz to 0.8 GHz unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.4		0.8	GHz	
GAIN						
Small Signal Gain		16.5	18		dB	
Gain Flatness			0.5		dB	
RETURN LOSS						
Input			8		dB	
Output			13		dB	
POWER						
Output Power	P_{OUT}		39		dBm	$P_{IN} = 25\text{ dBm}$
			41		dBm	$P_{IN} = 27\text{ dBm}$
Power Added Efficiency	PAE		45		%	$P_{IN} = 25\text{ dBm}$
			50		%	$P_{IN} = 27\text{ dBm}$
OUTPUT THIRD-ORDER INTERCEPT	OIP3		47.5		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE			5		dB	
SUPPLY VOLTAGE	V_{DD}	24	28	30	V	
QUIESCENT CURRENT	I_{DDQ}		100		mA	Adjust V_{GG} from -5 V to 0 V to achieve $I_{DDQ} = 100\text{ mA}$, $V_{GG} = -2.9\text{ V}$ typical to achieve $I_{DDQ} = 100\text{ mA}$

$T_A = 25^\circ\text{C}$, $V_{DD} = 28\text{ V}$, $I_{DDQ} = 100\text{ mA}$, and frequency range = 0.8 GHz to 1.1 GHz unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.8		1.1	GHz	
GAIN						
Small Signal Gain		16.5	18		dB	
Gain Flatness			1		dB	
RETURN LOSS						
Input			12		dB	
Output			15		dB	
POWER						
Output Power	P_{OUT}		40		dBm	$P_{IN} = 25\text{ dBm}$
			41.5		dBm	$P_{IN} = 27\text{ dBm}$
Power Added Efficiency	PAE		55		%	$P_{IN} = 25\text{ dBm}$
			60		%	$P_{IN} = 27\text{ dBm}$
OUTPUT THIRD-ORDER INTERCEPT	OIP3		45		dBm	P_{OUT} per tone = 30 dBm
NOISE FIGURE			5		dB	
SUPPLY VOLTAGE	V_{DD}	24	28	30	V	
QUIESCENT CURRENT	I_{DDQ}		100		mA	Adjust V_{GG} from -5 V to 0 V to achieve $I_{DDQ} = 100\text{ mA}$, $V_{GG} = -2.9\text{ V}$ typical to achieve $I_{DDQ} = 100\text{ mA}$

TOTAL QUIESCENT CURRENT BY V_{DD}

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
QUIESCENT CURRENT	I_{DDQ}		100		mA	Adjust V_{GG} between -5 V and 0 V to achieve $I_{DDQ} = 100\text{ mA}$ typical
			100		mA	$V_{DD} = 24\text{ V}$
			100		mA	$V_{DD} = 26\text{ V}$
			100		mA	$V_{DD} = 28\text{ V}$
			100		mA	$V_{DD} = 30\text{ V}$

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter ¹	Rating
Supply Voltage (V_{DD})	32 V
Gate Bias Voltage (V_{GG})	-8 V to 0 V
Radio Frequency Input Power (RFIN)	33 dBm
Voltage Standing Wave Ratio (VSWR) ²	6:1
Channel Temperature	225°C
Peak Reflow Temperature Moisture Sensitivity Level 3 (MSL3) ³	260°C
Continuous Power Dissipation, P_{DISS} ($T_A = 85^\circ\text{C}$, Derate 151.5 mW/°C Above 85°C)	21.21 W
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model	Class 1B, passed 500 V

¹ When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the absolute maximum rating is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

² Restricted by maximum power dissipation.

³ See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
CG-32-2 ¹	6.6	°C/W

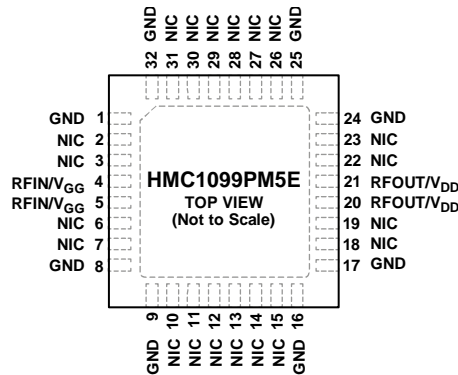
¹ Thermal resistance (θ_{JC}) was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground paddle, to the PCB, and the ground paddle is held constant at the operating temperature of 85°C.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.
 2. NO INTERNAL CONNECTION. THESE PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, ALL DATA WAS MEASURED WITH THESE PINS CONNECTED TO RF AND DC GROUND EXTERNALLY.

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 17, 24, 25, 32	GND	Ground. These pins must be connected to RF and dc ground. See Figure 3 for the GND interface schematic.
2, 3, 6, 7, 10 to 15, 18, 19, 22, 23, 26 to 31	NIC	No Internal Connection. These pins are not connected internally. However, all data was measured with these pins connected to RF and dc ground externally.
4, 5	RFIN/V _{GG}	RF Input/Gate Bias Control Voltage. This pin is a multifunction pin. The RFIN/V _{GG} pin is dc-coupled with internal prematching and requires external matching to 50 Ω, as shown in Figure 49. See Figure 4 for the RFIN/V _{GG} interface schematic.
20, 21	RFOUT/V _{DD}	RF Output/Supply Voltage. This pin is a multifunction pin. The RFOUT/V _{DD} pin is dc-coupled and requires external matching to 50 Ω, as shown in Figure 49. See Figure 4 for the RFOUT/V _{DD} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface

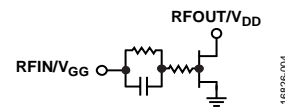


Figure 4. RFIN/V_{GG} and RFOUT/V_{DD} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

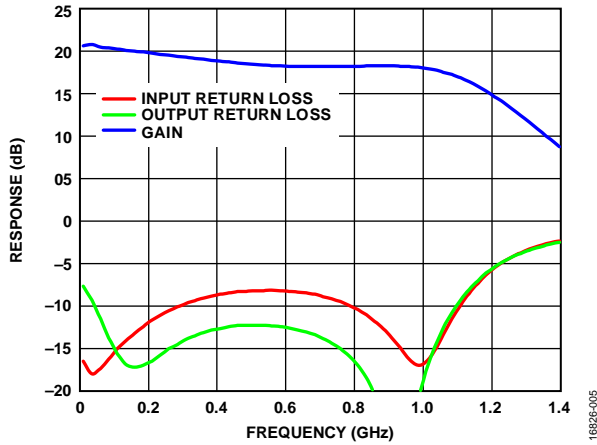


Figure 5. Response vs. Frequency, Broadband Gain and Return Loss

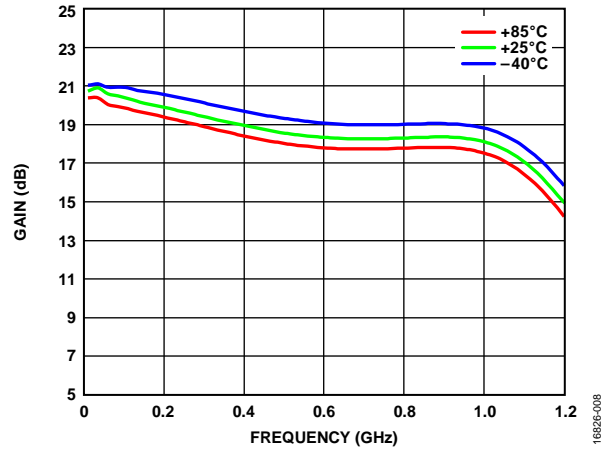


Figure 8. Gain vs. Frequency at Various Temperatures

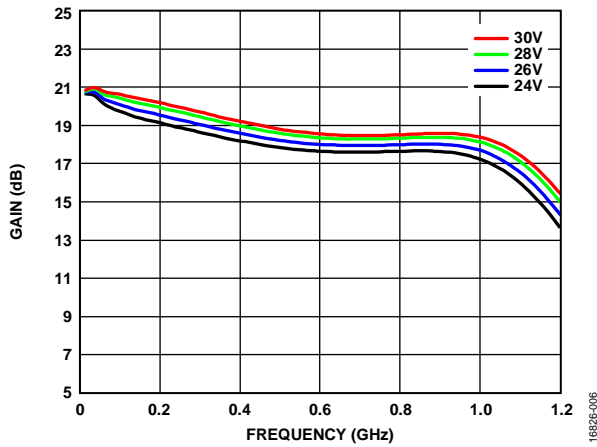


Figure 6. Gain vs. Frequency at Various Supply Voltages

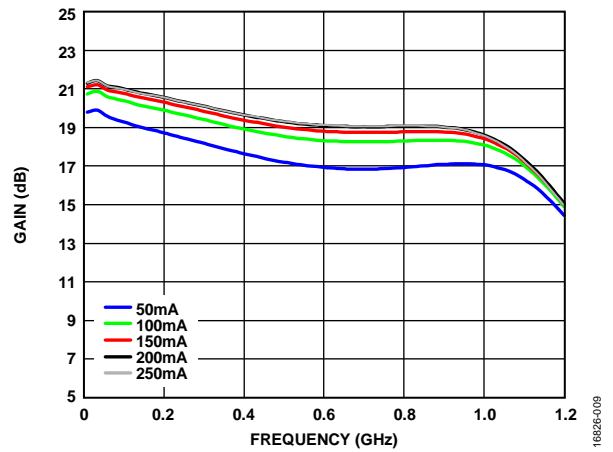


Figure 9. Gain vs. Frequency at Various Quiescent Currents

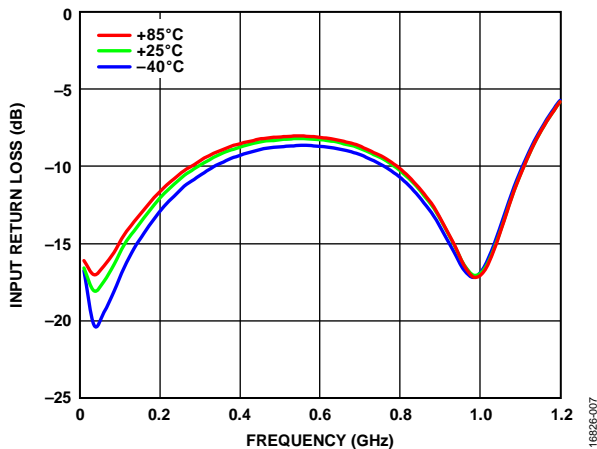


Figure 7. Input Return Loss vs. Frequency at Various Temperatures

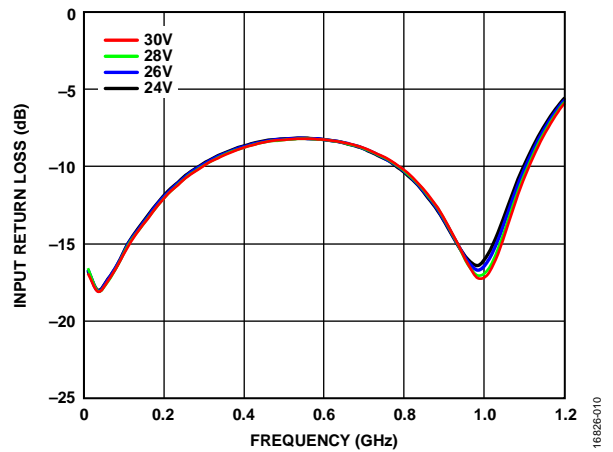


Figure 10. Input Return Loss vs. Frequency at Various Supply Voltages

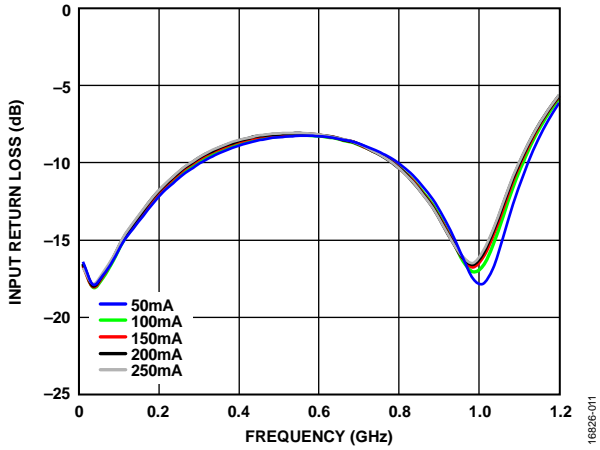


Figure 11. Input Return Loss vs. Frequency at Various Quiescent Currents

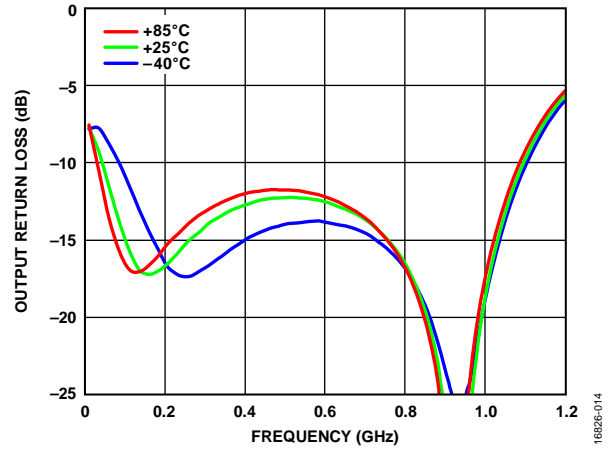


Figure 14. Output Return Loss vs. Frequency at Various Temperatures

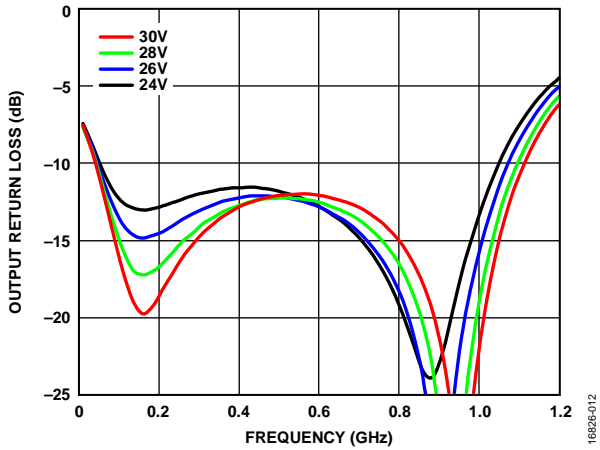


Figure 12. Output Return Loss vs. Frequency at Various Supply Voltages

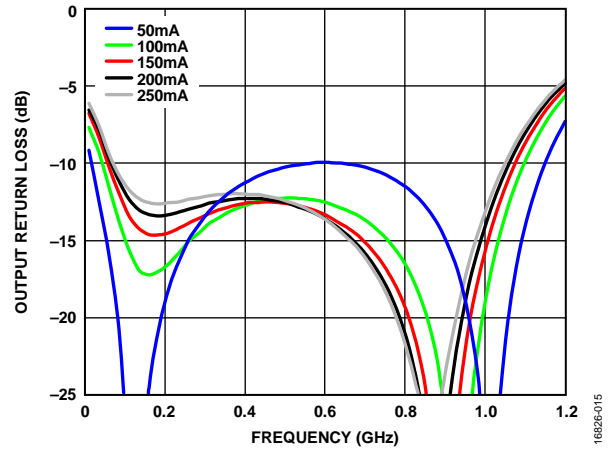


Figure 15. Output Return Loss vs. Frequency at Various Quiescent Currents

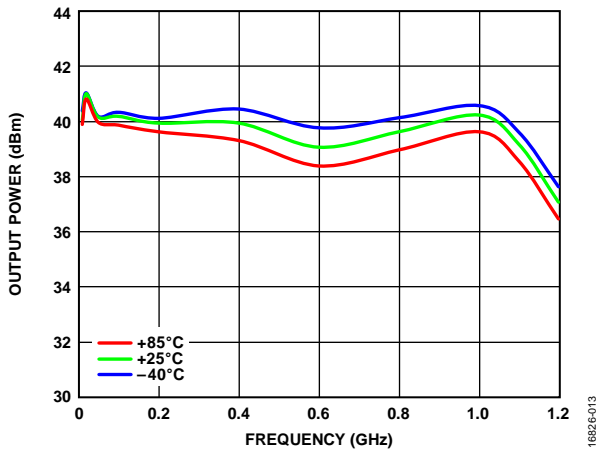


Figure 13. Output Power vs. Frequency at Various Temperatures, $P_{IN} = 25$ dBm

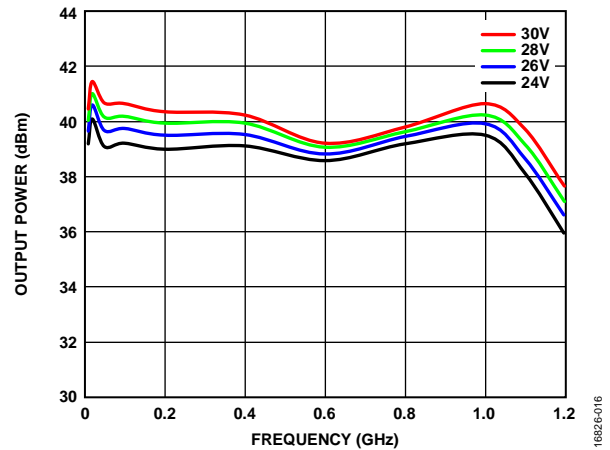


Figure 16. Output Power vs. Frequency at Various Supply Voltages, $P_{IN} = 25$ dBm

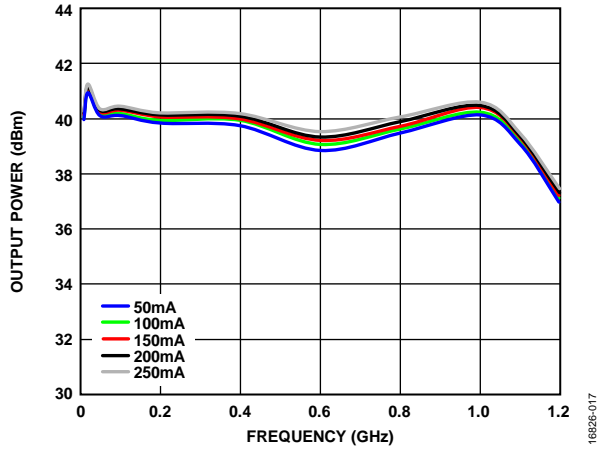


Figure 17. Output Power vs. Frequency at Various Quiescent Currents, $P_{IN} = 25$ dBm

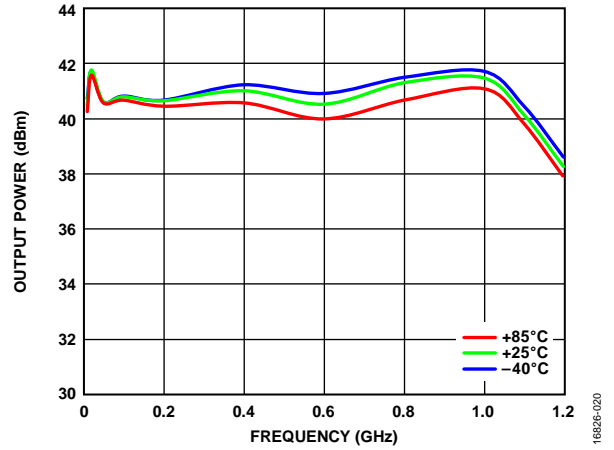


Figure 20. Output Power vs. Frequency at Various Temperatures, $P_{IN} = 27$ dBm

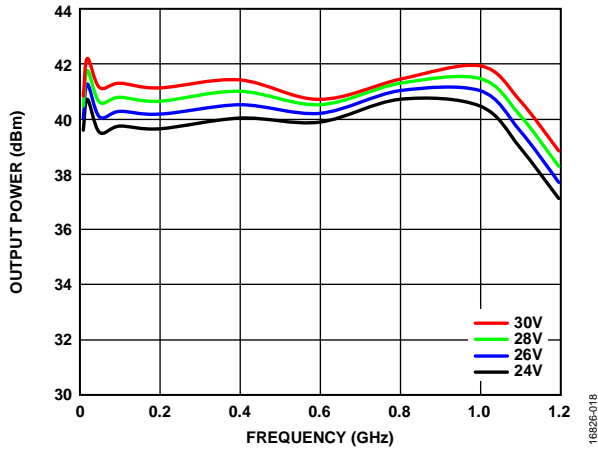


Figure 18. Output Power vs. Frequency at Various Supply Voltages, $P_{IN} = 27$ dBm

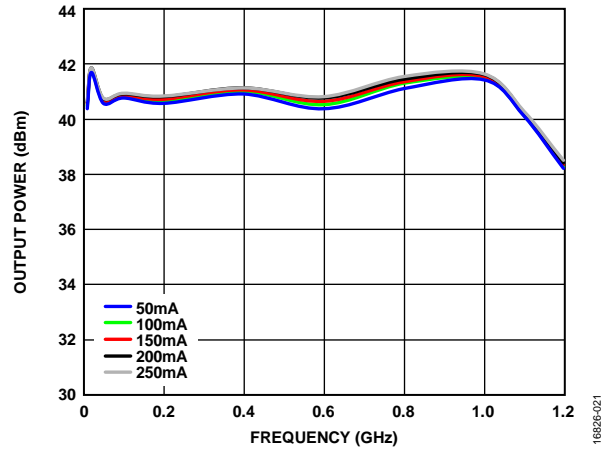


Figure 21. Output Power vs. Frequency at Various Quiescent Currents, $P_{IN} = 27$ dBm

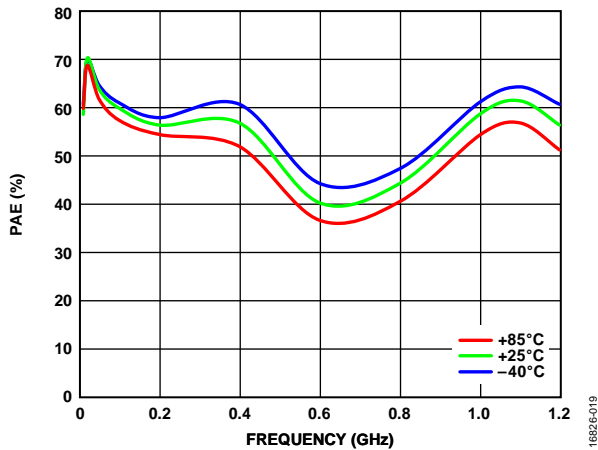


Figure 19. PAE vs. Frequency at Various Temperatures, $P_{IN} = 25$ dBm

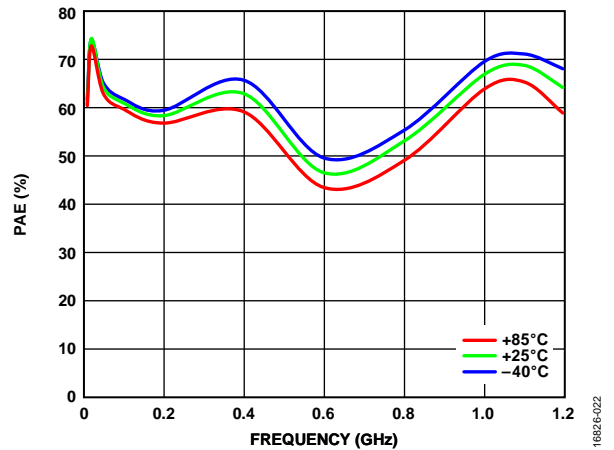


Figure 22. PAE vs. Frequency at Various Temperatures, $P_{IN} = 27$ dBm

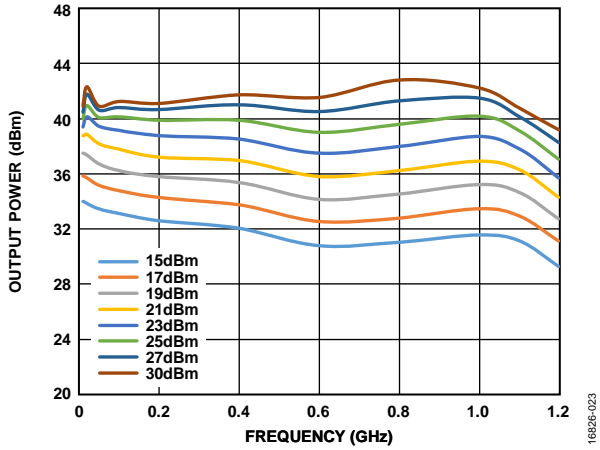


Figure 23. Output Power vs. Frequency at Various Input Powers

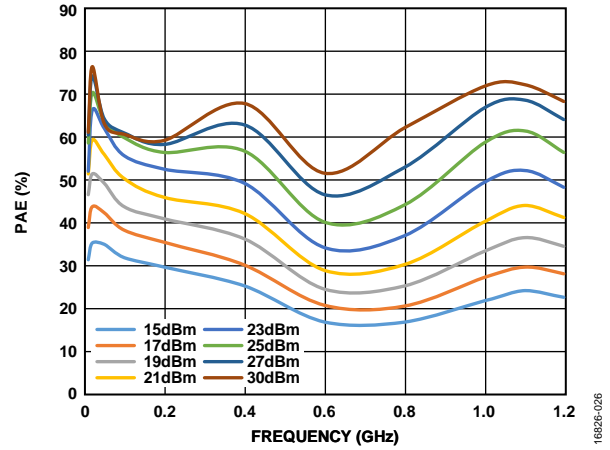


Figure 26. PAE vs. Frequency at Various Input Powers

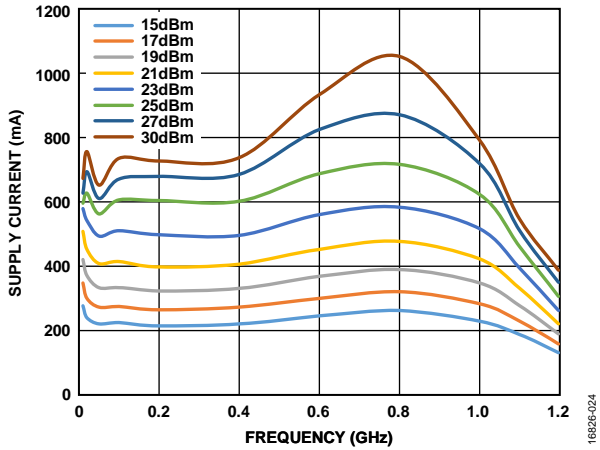


Figure 24. Supply Current (I_{DD}) vs. Frequency at Various Input Powers

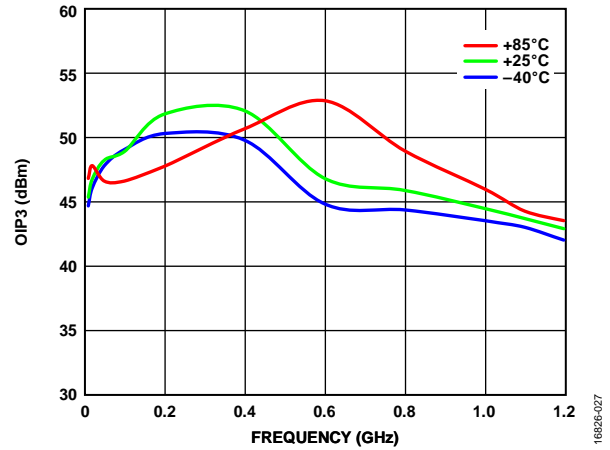


Figure 27. OIP3 vs. Frequency at Various Temperatures, P_{OUT} per Tone = 30 dBm

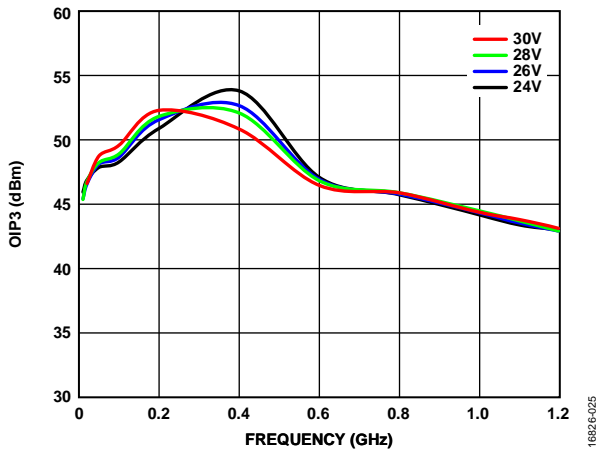


Figure 25. OIP3 vs. Frequency at Various Supply Voltages, P_{OUT} per Tone = 30 dBm

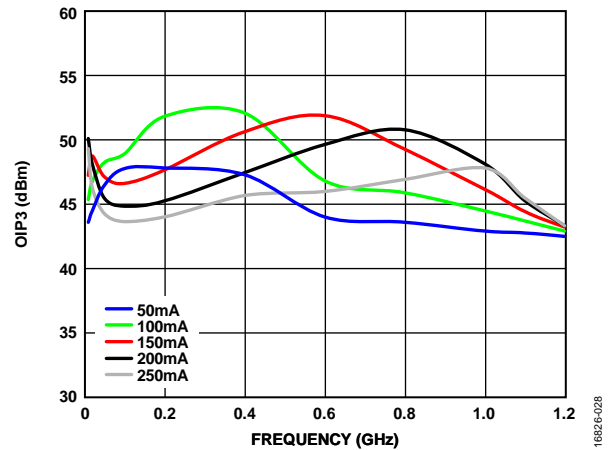


Figure 28. OIP3 vs. Frequency at Various Quiescent Currents, P_{OUT} per Tone = 30 dBm

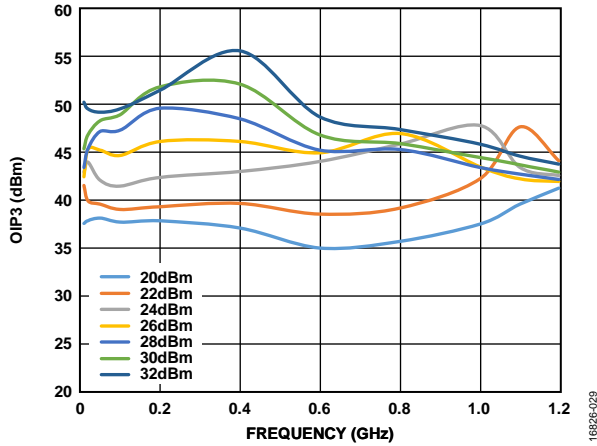


Figure 29. OIP3 vs. Frequency at Various P_{OUT} per Tone

16826-029

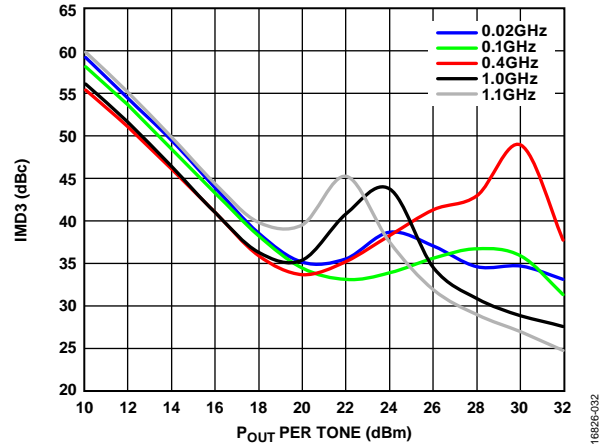


Figure 32. IMD3 vs. P_{OUT} per Tone, $V_{DD} = 24 V$

16826-032

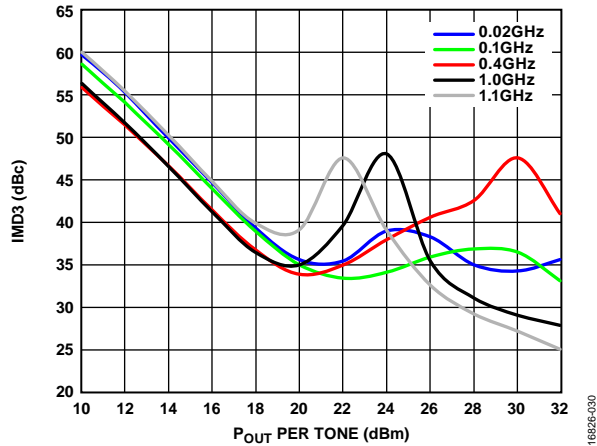


Figure 30. Output Third-Order Intermodulation (IMD3) vs. P_{OUT} per Tone, $V_{DD} = 26 V$

16826-030

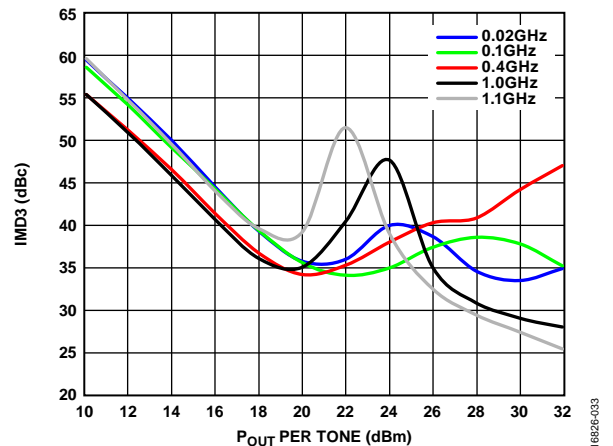


Figure 33. IMD3 vs. P_{OUT} per Tone, $V_{DD} = 28 V$

16826-033

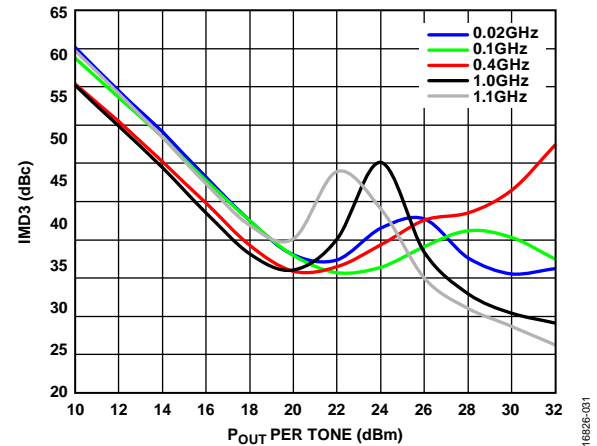


Figure 31. IMD3 vs. P_{OUT} per Tone, $V_{DD} = 30 V$

16826-031

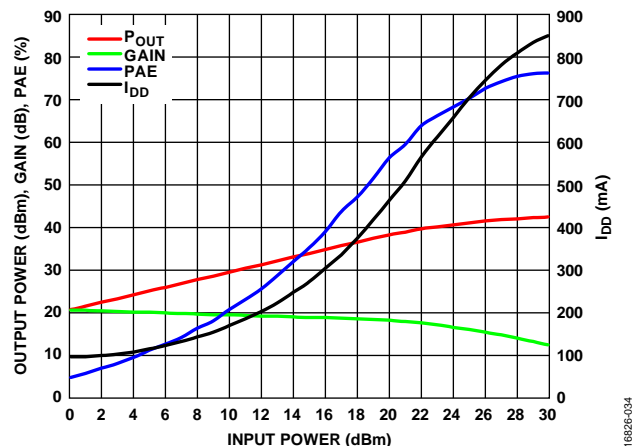


Figure 34. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 0.02 GHz

16826-034

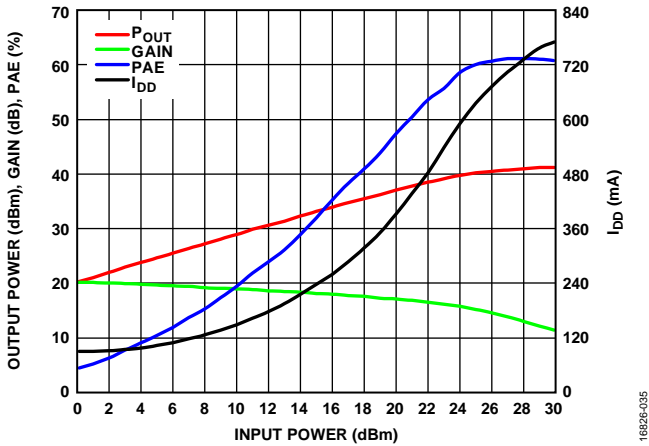


Figure 35. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 0.1 GHz

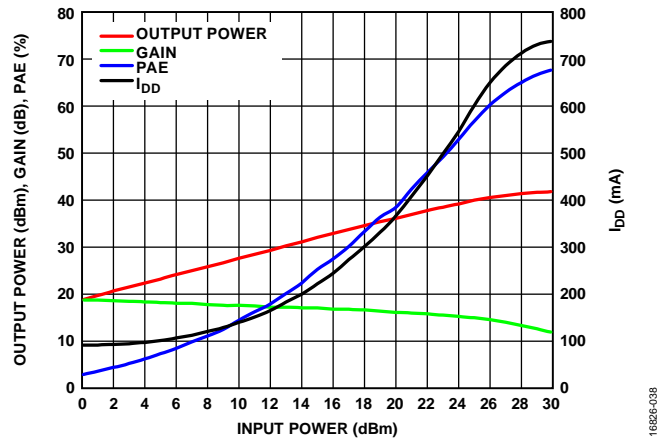


Figure 38. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 0.4 GHz

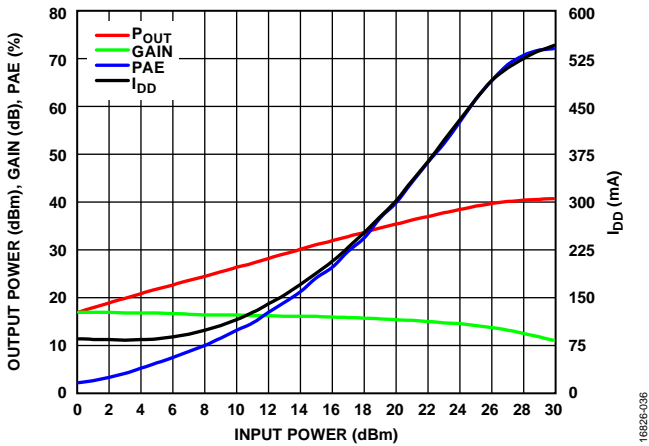


Figure 36. Output Power, Gain, PAE, and I_{DD} vs. Input Power at 1.1 GHz

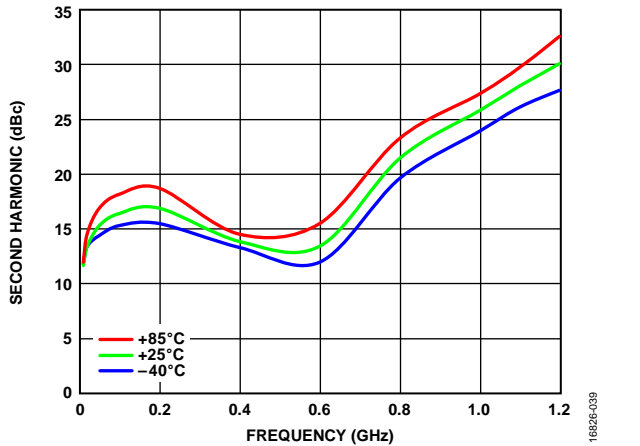


Figure 39. Second Harmonic vs. Frequency at Various Temperatures, $P_{IN} = 15$ dBm

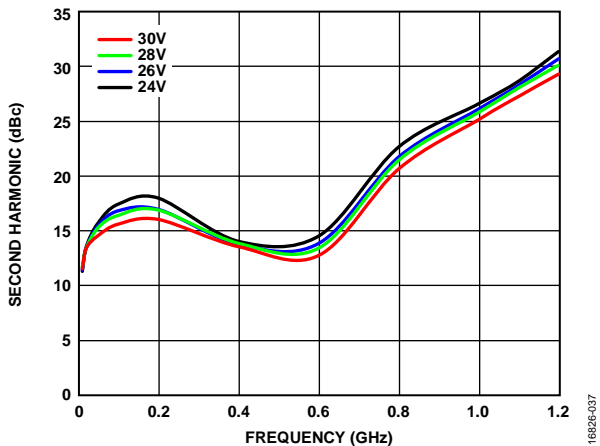


Figure 37. Second Harmonic vs. Frequency at Various Supply Voltages, $P_{IN} = 15$ dBm

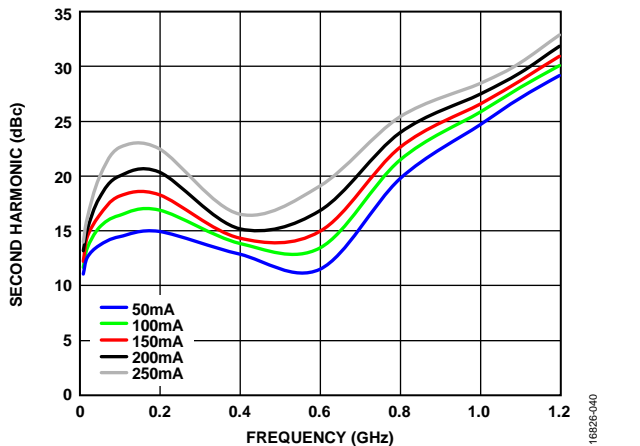


Figure 40. Second Harmonic vs. Frequency at Various Quiescent Currents, $P_{IN} = 15$ dBm

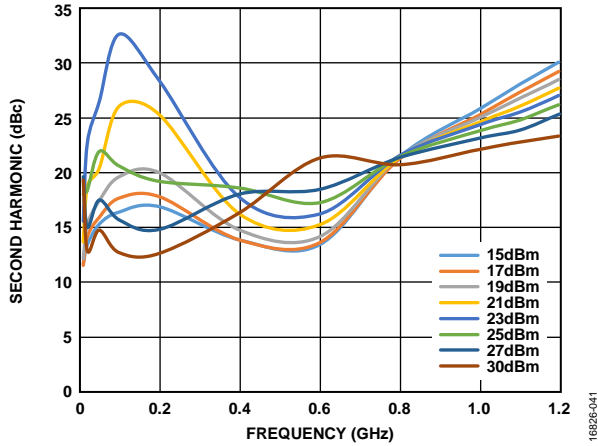


Figure 41. Second Harmonic vs. Frequency at Various Input Powers

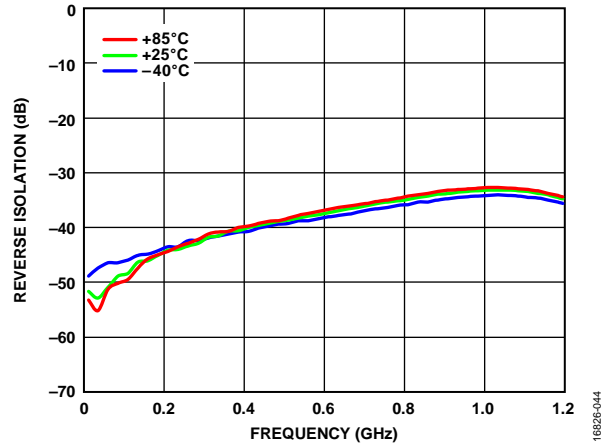


Figure 44. Reverse Isolation vs. Frequency at Various Temperatures

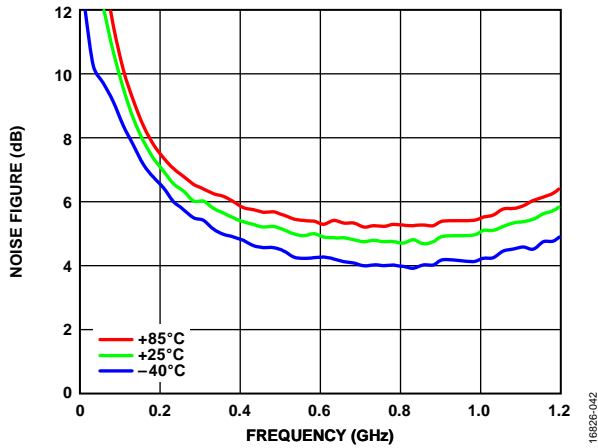


Figure 42. Noise Figure vs. Frequency at Various Temperatures

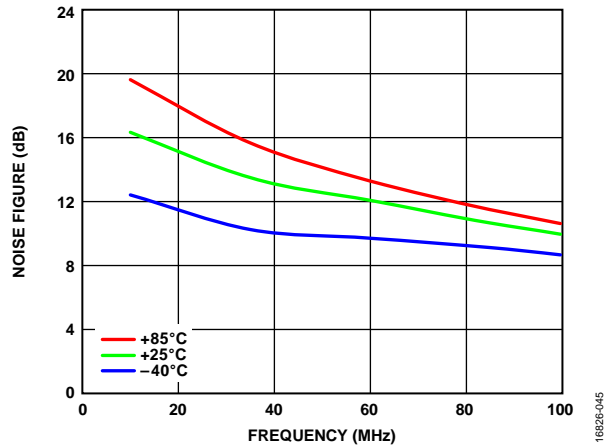


Figure 45. Noise Figure vs. Frequency at Various Temperatures, Low Frequency

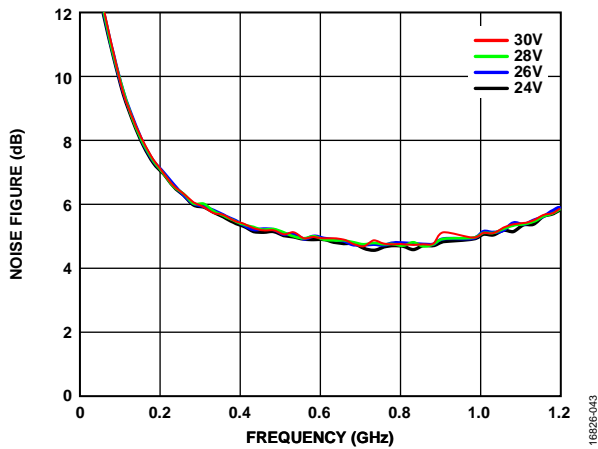


Figure 43. Noise Figure vs. Frequency at Various Supply Voltages

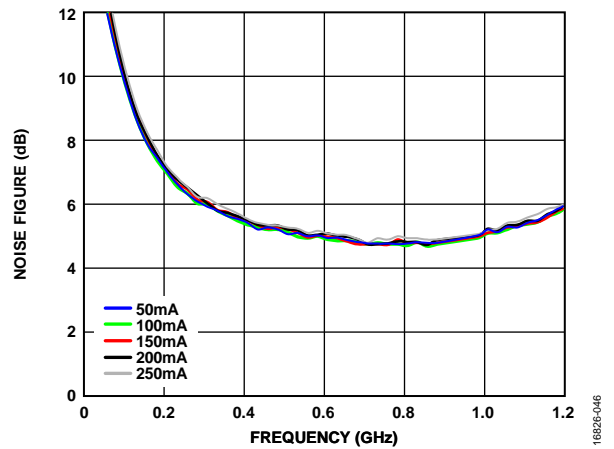


Figure 46. Noise Figure vs. Frequency at Various Quiescent Currents

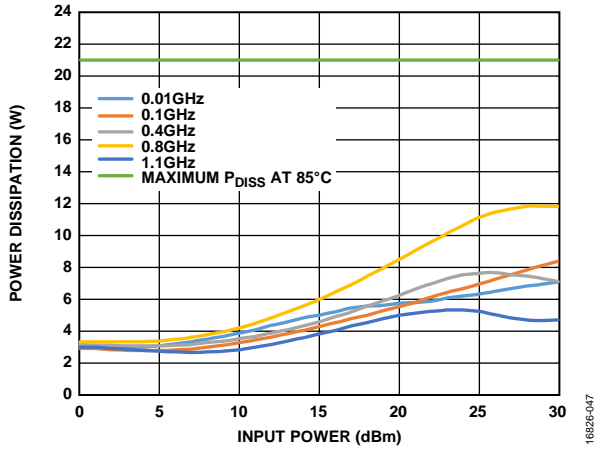


Figure 47. Power Dissipation vs. Input Power at Various Frequencies, $T_A = 85^\circ\text{C}$

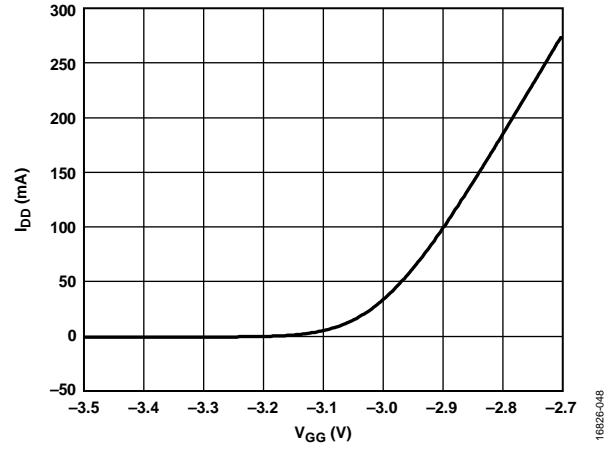


Figure 48. I_{DD} vs. V_{GG} at $V_{DD} = 28\text{ V}$, Representative of a Typical Device

THEORY OF OPERATION

The HMC1099PM5E is a 10 W (40 dBm), gallium nitride (GaN), power amplifier that consists of a single gain stage that effectively operates like a single field effect transistor (FET). The device is internally prematched so that a simple, external matching network optimizes the performance across the entire

operating frequency range. The recommended dc bias conditions put the device in Class AB operation, resulting in high output power (41.5 dBm typical at $P_{IN} = 27$ dBm) at improved levels of power efficiency (60% typical at $P_{IN} = 27$ dBm).

APPLICATIONS INFORMATION

The supply voltage is applied through the RFOUT/ V_{DD} pin, and the gate bias voltage is applied through the RFIN/ V_{GG} pin. For operation of a single application circuit across the entire frequency range, it is recommended to use the external matching components specified in the typical application circuit (L1, C1, L3, and C8) shown in Figure 49. If operation is only required across a narrower frequency range, performance may be optimized additionally through the implementation of alternate matching networks. Capacitive bypassing of V_{DD} and V_{GG} is recommended.

The recommended power-up bias sequence follows:

1. Connect the power supply ground to the circuit ground.
2. Set V_{GG} to -8 V to pinch off the drain current.
3. Set V_{DD} to 28 V to pinch off the drain current.
4. Adjust V_{GG} between -3 V and -2.5 V until a quiescent current of $I_{DDQ} = 100$ mA is obtained.
5. Apply the RF signal.

The recommended power-down bias sequence follows:

1. Turn off the RF signal.
2. Set V_{GG} to -8 V to pinch off the drain current.
3. Set V_{DD} to 0 V.
4. Set V_{GG} to 0 V.

All measurements for this device were taken using the typical application circuit, configured as shown in the typical application circuit (see Figure 49). The bias conditions shown in the electrical specifications table (see Table 1 to Table 3) are the recommended operating points to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the HMC1099PM5E under other bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section.

The evaluation PCB provides the HMC1099PM5E in its typical application circuit, allowing easy operation using standard dc power supplies and $50\ \Omega$ RF test equipment.

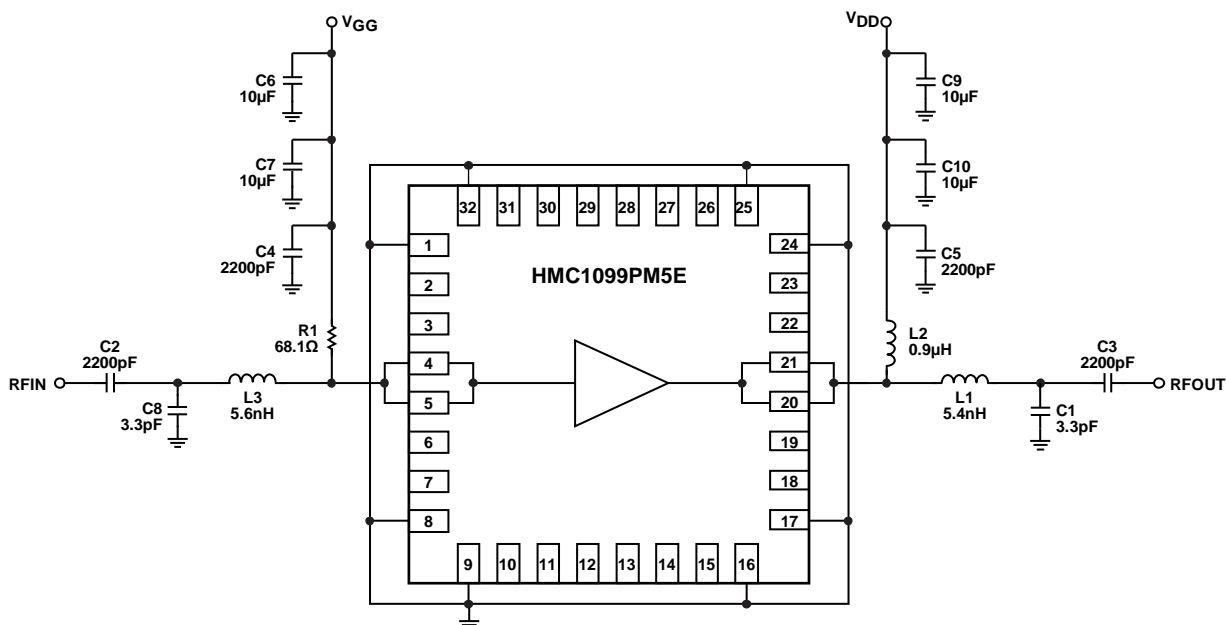


Figure 49. Typical Application Circuit

16826-019

EVALUATION PCB

Use RF circuit design techniques for the PCB used in the device. Provide a 50 Ω impedance for the signal lines and directly connect the package ground leads and exposed pad to the ground plane, similar to that shown in Figure 50. Use a

sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 50 is available from Analog Devices, Inc., upon request.

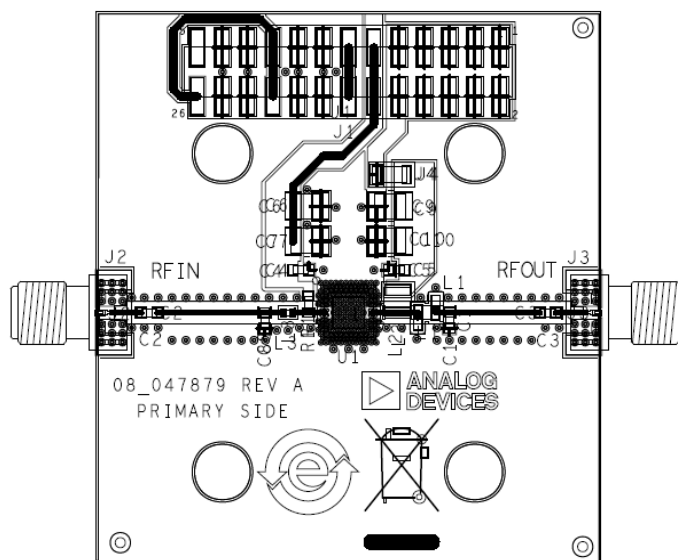


Figure 50. Evaluation PCB

Table 8. Bill of Materials for Evaluation PCB EV1HMC1099PM5

Item	Description
J1	DC pin
J2, J3	SMA connectors, 25-146-1000-92
J4	Preform jumper
C1, C8	3.3 pF capacitors, 0603 package
C2 to C5	2200 pF capacitors, 0603 package
C6, C7, C9, C10	10 μF capacitors, 1210 package
L1	5.4 nH inductor, 0906 package
L2	0.9 μH inductor, 1008 package
L3	5.6 nH inductor, 0402 package
R1	68.1 Ω resistor, 0603 package
U1	HMC1099PM5E amplifier
Heat Sink	Used for thermal transfer from the HMC1099PM5E amplifier
PCB	EV1HMC1099PM5 PCB, circuit board material: Rogers 4350 or Arlon 25FR

OUTLINE DIMENSIONS

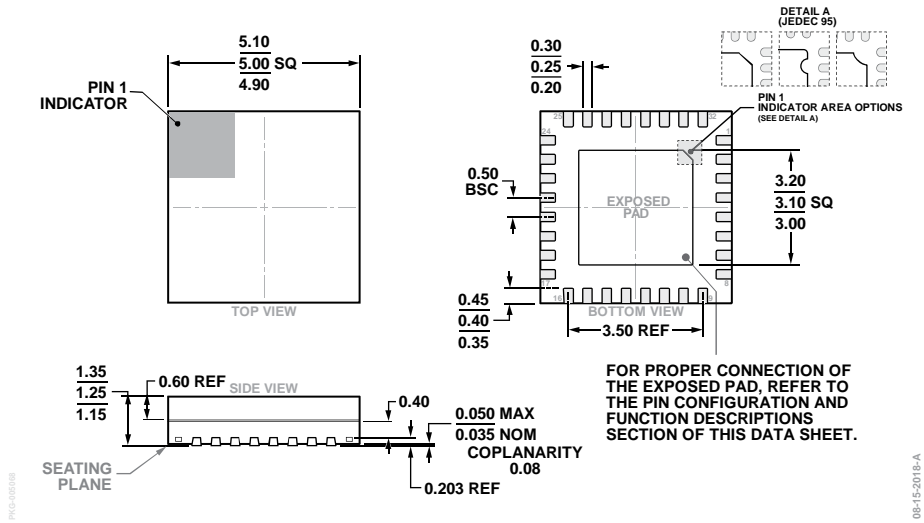


Figure 51. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
 5 mm × 5 mm Body and 1.25 mm Package Height
 (CG-32-2)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1,2}	Temperature Range	MSL Rating ³	Description ⁴	Package Option
HMC1099PM5E	-40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
HMC1099PM5ETR	-40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
EV1HMC1099PM5			Evaluation Board	

¹ All models are RoHS compliant.
² When ordering the evaluation board only, reference the model number, [EV1HMC1099PM5](#).
³ See the Absolute Maximum Ratings section for additional information.
⁴ The lead finish of the HMC1099PM5E and the HMC1099PM5ETR are nickel palladium gold (NiPdAu).

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