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APPLICATION NOTE

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Using the ADN8831 TEC Controller Evaluation Board

by Gang Liu and Dongfeng Zhao

INTRODUCTION

The ADN8831 is a thermoelectric cooler (TEC) controller that drives medium power TECs (<4 A current) with excellent temperature control resolution, stability, and high power efficiency. The ADN8831 integrates two high performance amplifiers dedicated to temperature sensing and thermal loop compensation, allowing direct interface to a thermistor, a resistive temperature device (RTD), or other temperature sensors.

When used in conjunction with the ADN8831 data sheet, this application note describes how to configure the EVAL-ADN8831 evaluation board (Version. 3.1), and how to develop a real TEC control circuit with an ADN8831. The ADN8831 data sheet provides the detailed technical specifications and internal functional block diagrams, as well as the application design guidelines.

Important layout design guidelines are available in the Evaluation Board Layout section of this application note.

EVALUATION BOARD DESCRIPTION

The ADN8831 evaluation board offers a configurable design platform to work with various TECs and thermistors. On the evaluation board, the ADN8831 delivers and controls a bidirectional TEC current using two pairs of complementary MOSFETs in an H-bridge configuration.

With the on-board, adjustable components, the evaluation board provides configurability of temperature setpoint, temperature setpoint range, TEC current and/or voltage limits, and a PID compensation network. The temperature setpoint range (factory default) circuit, optimized to work with 10 kΩ negative temperature coefficient thermistors, can also work with other types of temperature sensors. The tunable PID compensation network allows the characteristic matching between the control circuit and the thermal load for achieving the fastest response time and temperature control stability. A green LED illuminates when the TEMOUT voltage is within ±100 mV of the TEMPSET setpoint voltage.

FUNCTIONAL BLOCK DIAGRAM

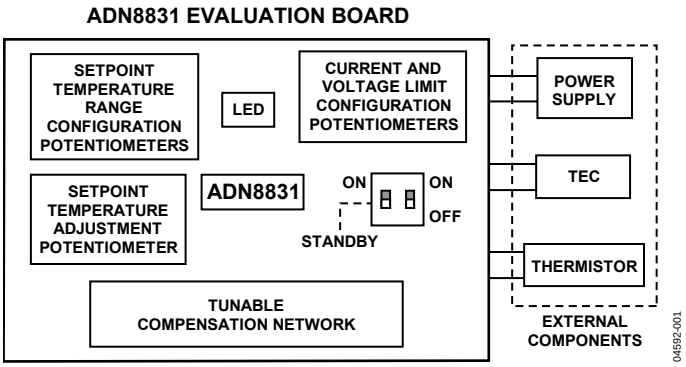

Figure 1. Functional Block Diagram of ADN8831 Evaluation Board

TABLE OF CONTENTS

Introduction 1
Evaluation Board Description 1
Functional Block Diagram 1
Getting Started 3
Switches and Potentiometers 3
Quick Start 4
Configure Setpoint Temperature Range 4
Configure the Setpoint Temperature 5
Set the Output Current Limits 5
Set the Output Voltage Limit 6
Monitor the TEC Voltage 6
Monitor the TEC Current 6
Temperature Compensation 6
Adjust the PWM Switching Frequency 7
Multiple Unit Evaluation 7
Evaluation Board Layout 8
Evaluation Board Schematic and Artwork 9

GETTING STARTED

The EVAL-ADN8831, shown in Figure 2, is set by factory default to deliver about 2 A bidirectional TEC current while working with a 10 kΩ thermistor at 25°C.

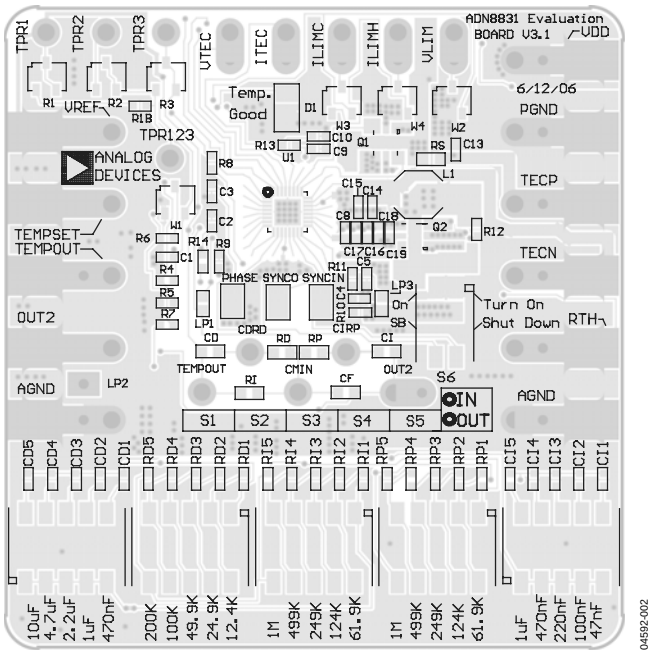

Figure 2. Top View of the Evaluation Board

The factory default setting determines the on-board component values of the temperature-to-voltage converter circuit and the PID circuit shown in Figure 3. With the on-board switches and potentiometers, the circuits in Figure 3 can be adapted to work with most TEC and thermistors used in telecommunications.

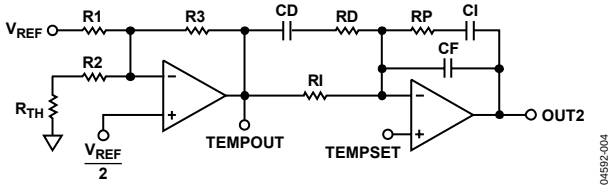

Figure 3. Temperature and Compensation Network Circuits

Referring to Figure 3, note that TEMPOUT refers to voltage signal outputs from Pin 4 (OUT1) and TEMPSET, a voltage signal, applied to Pin 5 (IN2P). These terms are used throughout this application note.

SWITCHES AND POTENTIOMETERS

Table 1. Switch Settings

Switch	Function	Default
S1	CD	1 uF
S2	RD	24.9 kΩ
S3	RI	249 kΩ
S4	RP	249 kΩ
S5	CI	470 nF
S6	Standby/shutdown	Up/up

Switch S6, Left Hand Side: Standby Control

The ADN8831 is placed in standby mode when Switch S6 (the left hand side knob) is down. When the knob is up (default), the ADN8831 is released from standby mode. In standby mode, all circuits, with the exception of the V_{REF} and SYNCO outputs of the ADN8831, are powered off.

Switch S6, Right Hand Side: Shutdown Control

The ADN8831 is in shutdown mode when Switch S6 (the right hand side knob) is down. When the knob is up (default), the ADN8831 is released from shutdown mode. In shutdown mode, the ADN8831 is powered off.

Switches S1, S2, S3, S4, and S5: Adjustable Components for an Optimal PID Compensation Network

Switches S1, S2, S3, S4, and S5 provide PID network component adjustability for CD, RD, RI, RP, and CI as shown in Figure 3. After connecting one TEC to an EVAL-ADN8831, a thermal oscillation may occur. To squelch the oscillation, optimize the system settling time, and to control the TEC temperature precisely, PID network component tuning is necessary.

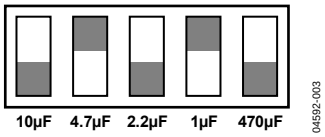

Figure 4. Switch Position for Switch S1

When a switch knob is in the up position, the value listed below the switch knob is an increment to the component. For example, Switch S1 determines the CD value in Figure 3 and Figure 9. Switch S1 shows the up knobs for the 4.7 µF and the 1 µF (note that these knobs are set to the upper position). In this example, the value of CD is

$$4.7\ \mu F + 1\ \mu F = 5.7\ \mu F$$

The same principle applies to Switches S1, S2, S3, S4, and S5.

On-Board Potentiometers

The EVAL-ADN8831 has the following on-board potentiometers to adjust the component values (shown in Figure 3) and to configure the TEC current limitation at both cooling and heating modes.

The default settings are shown in Table 2.

Table 2. Potentiometer Settings

Potentiometer	Function	Default
R1	Temperature compensation network	17.5 kΩ
R2	Temperature compensation network	7.5 kΩ
R3	Temperature compensation network	81.3 kΩ
W1	TEMPSET	20 kΩ
W2	V_{LIM}	20 kΩ
W3	V_{ILIMC}, V_{ILIMH}	20 kΩ
W4	V_{ILIMC}, V_{ILIMH}	20 kΩ

QUICK START

Connect the power supply, the TEC module, and the thermistor to an EVAL-ADN8831 as shown in Figure 5 and as described in Step 1 through Step 6.

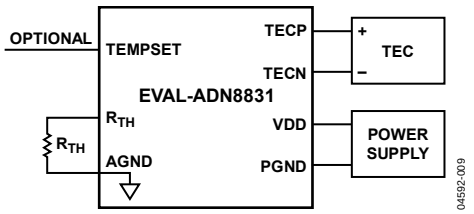

Figure 5. EVAL-ADN8831 Quick Start Block Diagram

1. Verify that the on-board switches are set to the defaults.
2. Connect the thermistor between the board pads labeled R_{TH} and AGND.
3. Connect the positive terminal of a thermoelectric cooler to the TECP board pad and connect the negative terminal to TECN.
4. Verify the on-board potentiometer default settings.
5. Ensure that the power supply is powered off and then connect it to board pads VDD and PGND. Maintain the power supply between 3.0 V and 5.5 V for proper operation.
6. Turn on the power supply.

The thermistor temperature-dependent voltage, TEMPOUT, locks to the programmed setpoint voltage, TEMPSET. The green LED illuminates within several seconds, indicating successful temperature lock.

CONFIGURE SETPOINT TEMPERATURE RANGE

The default values for Resistor R1, R2, and R3, listed in Table 2, are optimal for a 10 kΩ, β = 3450 (at 25°C) thermistor to lock a TEC temperature at 25°C. The sections that follow describe how to configure potentiometers for different negative temperature coefficient (NTC) thermistors.

Thermistor Values

Determine the three thermistor resistance values: R_{HIGH}, R_{MID}, and R_{LOW}. To do this, refer to the termistor R-T table in the appropriate thermistor data sheet. This is based on required TEC thermal control resolution and the target controllable temperature range.

These resistor values correspond to the high, middle, and low setpoint temperatures (T_{HIGH}, T_{MID}, and T_{LOW}). {T_{HIGH}, T_{LOW}} is the TEC system controllable setpoint temperature range.

$$T_{MID} = \frac{T_{HIGH} + T_{LOW}}{2}$$

T_{MID} is the average temperature, between T_{HIGH} and T_{LOW}. $V_{TEMPOUT}$, is the voltage output at the TEMPOUT pin. It is R_{TH} resistance dependent. $V_{TEMPOUT}$ is a function of R_{TH}, R1, R2, and R3 as

$$V_{TEMPOUT} = 0.5 \times V_{REF} \times R_3 \times \left[\frac{1}{R_3} - \frac{1}{R_1} + \frac{1}{R_2 + R_{TH}} \right]$$

In a design, let $V_{TEMPOUT}$ equal the following values at the three thermistor resistances:

$R_{TH} = R_{HIGH}$(at T_{HIGH}): $V_{TEMPOUT} = V_{REF}$

$R_{TH} = R_{MID}$(at T_{MID}): $V_{TEMPOUT} = 0.5 \times V_{REF}$

$R_{TH} = R_{LOW}$(at T_{LOW}): $V_{TEMPOUT} = 0$ V

In this example, V_{REF} equals about 2.5 V and is a reference voltage at Pin 8 of the ADN8831.

Resistor Values

To achieve the required $V_{TEMPOUT}$ outputs at the three different setting point temperatures, use the equation

$$R1 = R_{MID} + \frac{R_{MID}(R_{LOW} + R_{HIGH}) - 2R_{HIGH}R_{LOW}}{R_{HIGH} + R_{LOW} - 2R_{MID}} \quad (1)$$

$$R2 = R1 - R_{MID} \quad (2)$$

$$R3 = \frac{R_1(R_1 + R_{LOW} - R_{MID})}{R_{LOW} - R_{MID}} \quad (3)$$

For example, setting the high setpoint temperature at 35°C and the low setpoint temperature at 15°C results in a middle setpoint temperature (35 + 15)/2 = 25°C. Using the R-T table of a thermistor,

R_{HIGH} = 6.9 kΩ
R_{MID} = 10 kΩ
R_{LOW} = 14.8 kΩ

Note that Equation 1 to Equation 3 result in

R1 = 17.5 kΩ
R2 = 7.5 kΩ
R3 = 81.3 kΩ

Adjusting the Potentiometers R1, R2, and R3

To adjust on-board potentiometers to get the proper R1, R2, and R3 values, turn off the power supply and then measure the resistance between

- TPR1 and TPR123, and adjust Potentiometer R1 to *R1* = 17.5 kΩ.
- TPR2 and TPR123, and adjust PotentiometerR2 to *R2* = 7.5 kΩ.
- Between TPR3 and TPR123, and adjust Potentiometer R3 to *R3* = 81.3 kΩ.

Because these potentiometers connect to the active components inside the ADN8831, the measured result is not accurate if the internal components conduct a significant leakage current. These components have a turn on voltage of ~0.8 V.

After R1, R2, and R3 are configured, the output voltage of the first amplifier, $V_{TEMPOUT}$, equals

$$V_{TEMPOUT} = 0.5 \times V_{REF} \times R_3 \times \left[\frac{1}{R_3} - \frac{1}{R_1} + \frac{1}{R_2 + R_{TH}}\right]$$

where:
R_{TH} is the thermistor resistance within the setpoint temperature range.
V_{REF} is the voltage reference value of the ADN8831, nominally 2.5 V.

When the setpoint temperature range is narrow, such as <20°C, the relationship between the thermistor temperature and the temperature voltage, $V_{TEMPOUT}$, is almost linear, and the error is less than 0.15%. The linear equations is

$$V_{TEMPOUT} = V_{REF} \times \left[\frac{T_{SET} - T_{LOW}}{T_{HIGH} - T_{LOW}}\right]$$

where:
T_{HIGH} is the upper temperature limit in °C.
T_{LOW} is the lower temperature limit in °C.
T_{SET} is the setpoint temperature value in °C.

In the case where the second part of Equation 1 is negative, that is

$$\frac{R_{MID}(R_{LOW} + R_{HIGH}) - 2R_{HIGH}R_{LOW}}{R_{HIGH} + R_{LOW} - 2R_{MID}} \leq 0$$

Set $R1 = R_{MID}$ and $R2 = 0$.

For some applications, the setpoint temperature is not a range, but a single point temperature. In this case, set the single point temperature to be the midpoint temperature, T_{MID}, and set $T_{HIGH} = T_{MID} + 5°C$, and $T_{LOW} = T_{MID} - 5°C$. At the same time, set $R1 = R_{MID}$ and $R2 = 0$. Because the setpoint temperature is a single point, there is no need to linearize the $V_{TEMPOUT}$ vs. temperature response curve. After calculating R3, check to see if the gain of the first stage is between 10 and 30. The gain calculates as

$$GAIN = 2 \times R3/R_{MID}$$

If the gain is too high, increase the span between T_{HIGH} and T_{LOW}, otherwise, decrease the span.

Note that the lower limit on the TEMPOUT pin cannot be 0 V. The minimum output voltage is 50 mV. Configure the setpoint temperature range so that some margin exists in the lower limit. For example, for a temperature range of 35°C to 15°C, use 14.5°C (2% lower than the 15°C limit) as the lower limit.

CONFIGURE THE SETPOINT TEMPERATURE

The $V_{TEMPSET}$ voltage corresponds to a TEC setpoint temperature. Configure the $V_{TEMPSET}$ using Potentiometer W1. There are two cases in which to use Equation 4. In the first case, the setpoint temperature is known. Use the R-T table in the thermistor data sheet to find the specific value of R_{TH}, then solve for $V_{TEMPSET}$. Apply $V_{TEMPSET}$ to the TEMPSET pin.

In the second case, the voltage at Pin TEMPOUT is known. Solve the equation for R_{TH} and use the R-T table in the thermistor data sheet to find the setpoint temperature.

$$V_{TEMPSET} = 0.5 \times V_{REF} \times R_3 \times \left[\frac{1}{R_3} - \frac{1}{R_1} + \frac{1}{R_2 + R_{TH}}\right] \quad (4)$$

where:
R_{TH} is the thermistor resistance at the setpoint temperature.
V_{REF} is the voltage reference value of the ADN8831, nominally 2.5 V.

An alternative method is to assume that there is a linear relationship between temperature and voltage; this is similar to the linear relationship described for the TEMPOUT pin. When the setpoint temperature range is narrow, such as <20°C, the relationship between the thermistor temperature and the temperature voltage, $V_{TEMPOUT}$, is almost linear, and the error is less than 0.15%. It is possible to derive the setpoint temperature by the upper and lower temperatures and the voltage limit. The equation is

$$V_{TEMPSET} = V_{REF} \times \frac{T_{SET} - T_{LOW}}{T_{HIGH} - T_{LOW}}$$

where:
T_{HIGH} is the upper temperature limit in °C.
T_{LOW} is the lower temperature limit in °C.
T_{SET} is the setpoint temperature value in °C.

SET THE OUTPUT CURRENT LIMITS

Use Potentiometers W3 and W4 to determine the TEC current limits at cooling and heating modes. Then, use Equation 5 and Equation 6 to determine the required voltage levels applied to the ILIMC and ILIMH pins.

$$V_{ILIMC} = \frac{V_{REF}}{2} + 25 \times I_{TCMAX} \times R_S \quad (5)$$

$$V_{ILIMH} = \frac{V_{REF}}{2} - 25 \times I_{THMAX} \times R_S \quad (6)$$

where:
V_{ILIMC} is the voltage applied to Pin ILIMC.
V_{ILIMH} is the voltage applied to Pin ILIMH.
I_{TCMAX} is the maximum TEC current for cooling.
I_{THMAX} is the maximum TEC current for heating.
R_S is the resistance value of a current sense resistor. In Figure 9, $R_S = 0.02\ \Omega$.
V_{REF} is the reference voltage. When taken from the ADN8831, $V_{REF} = 2.5$ V.

For example, to set I_{TCMAX} and I_{THMAX} equal to 2 A and 1.5 A, respectively, use the following equations:

$$V_{ILIMC} = \frac{2.5}{2} + 25 \times 2 \times 0.02 = 2.25 \text{ V}$$

$$V_{ILIMH} = \frac{2.5}{2} - 25 \times 1.5 \times 0.02 = 0.5 \text{ V}$$

Turn Potentiometer W3 while measuring the voltage at Pin 1 (ILIMC); set this value to be equal to 2.25 V. Turn W4 while measuring the voltage at Pin 32 (ILIMH); set this value to equal 0.5 V.

SET THE OUTPUT VOLTAGE LIMIT

To protect the TEC from being overdriven, adjust W2 to set up the V_{LIM} voltage. The maximum voltage applied across the TEC can be limited by setting the voltage on Pin 31 (VLIM). This voltage is

$$V_{VLIM} = V_{TMAX}/5$$

where:
V_{VLIM} is the voltage set at the VLIM pin.
V_{TMAX} is the maximum voltage across the TEC.

For example, to set a maximum TEC voltage equal to 4 V, use the following equation:

$$V_{VLIM} = 4/5 = 0.8 \text{ V}$$

MONITOR THE TEC VOLTAGE

The voltage across the TEC, V_{TEC}, is monitored in real time by measuring the voltage V_{VTEC} from Pin 30 (VTEC).

$$V_{TEC} = V_{LFB} - V_{SFB} = (V_{VTEC} - 0.5 \times V_{REF}) \times 4$$

where:
V_{TEC} is the voltage across the TEC.
V_{LFB} is the voltage measured at the LFB pin.
V_{SFB} is the voltage measured at the SFB pin.
V_{VTEC} is the voltage measured at the VTEC pin.
V_{REF} is the reference voltage. When taken from the ADN8831, V_{REF} = 2.5 V.

Alternatively, measuring the voltage difference between the LFB and SFB pins also results in the voltage across the TEC (V_{TEC}). Typically, the LFB pin connects to the positive terminal of the TEC, and the SFB pin connects to the negative terminal of the TEC. The definition of the TEC voltage is the voltage difference between the TEC positive and negative terminals.

V_{TEC} can be positive or negative. When V_{TEC} is positive, the TEC is in cooling mode. When V_{TEC} is negative, the TEC is in heating mode.

When the ADN8831 is set to standby mode, knowing the voltage across the TEC is useful. This voltage, called the Seebeck voltage, is generated by the temperature difference between the two TEC plates. This measurement is useful for determining the condition of the TEC and/or the TEC working status for high end systems.

MONITOR THE TEC CURRENT

The TEC current is monitored in real time by measuring the voltage, V_{ITEC}, on the ITEC pin (Pin 29). To calculate the TEC current from the ITEC pin voltage, use the following equation:

$$I_{TEC} = \frac{V_{ITEC} - 0.5 \times V_{REF}}{25 \times R_S}$$

where:
I_{TEC} is the TEC current; defined as the current flowing in through the TEC positive terminal (TECP) and out the TEC negative terminal (TECN).
R_S is the current sense resistor value, set to 0.02 Ω on the evaluation board.

TEMPERATURE COMPENSATION

Temperature stability and settling time are control loop gain and bandwidth dependent. This includes the gain of the ADN8831 and the TEC/thermistor feedback. To achieve the highest dc precision, the control loop uses a proportional integral differential (PID) compensation network. Because thermal loads can vary widely from TEC to TEC, a tunable compensation network is available on the evaluation board.

To tune the PID compensation network, apply a low frequency square wave to the LP2 solder pad and monitor the OUT2 test point using an oscilloscope.

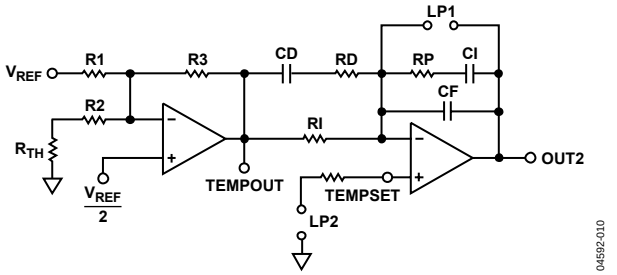

Figure 6. Tunable Compensation Network

Before doing this, connect a TEC to the evaluation board TECP and TECN pads and connect the thermistor attached to the TEC to the evaluation board RTH and AGND pads. The low frequency square wave equates to sending a step function to TEMPSET. An alternative method to the square wave is to use a pair of tweezers to short-circuit the LP2 solder pad with the AGND test point. Observe the waveform at OUT2 to determine if the compensation network matches the thermal load. The ideal response at OUT2 has the fastest possible rise time and settling time with little or no overshoot. Use the following steps to tune the network:

1. Set CI to 1 µF, RI and RP to 249 kΩ, RD to 100 kΩ, and CD to 470 nF. Make sure that the loop is stable. If not, increase CI and decrease RP. This has the effect of increasing the time constant of the loop, allowing it to become stable. The effect of this increased time constant is a slower response time in the compensation network.

2. When the compensation loop is stable, it is possible to adjust the component values in the network to decrease the overall loop response time. This is accomplished by slowly decreasing CI, increasing RP, decreasing RD, increasing CD, and decreasing RI. Adjust these such that the output at Pin OUT2 has a fast rise and fall time with little or no overshoot. In applications where fast response time is critical, allow for a small amount of overshoot (10% to 20%).
3. After tuning the compensation network to satisfactory values, it is recommended to replace the tunable compensation network components with the discrete components to be used in the future system and repeat the test. After soldering the discrete components, turn off the tunable compensation network components by placing all the switches into the lower position.
4. The capacitors used in the compensation network should be multilayer ceramic capacitors of X7R material. This type of capacitor maintains a stable capacitance over temperature and bias drifts. X7R type capacitors also have a very low leakage current and low noise.

Typical performance for a butterfly-packaged laser with a settling time of 1°C change in setpoint temperature is approximately 0.2 second to 1 second; for a large mass laser head of 1 W to 3 W, the settling time is about 5 seconds to 20 seconds. For more details of the temperature compensation network, see the ADN8831 data sheet.

ADJUST THE PWM SWITCHING FREQUENCY

The ADN8831 evaluation board is default set to a free-run PWM clock at 1 MHz. To modify R_{FREQ}, adjust the PWM switching frequency (see Figure 7). Reducing the frequency of the PWM switching frequency improves the system power efficiency, but requires the use of a large physical size LC filter inductor and capacitors.

For telecommunication applications, the recommended setting (default) is 1 MHz for the switching frequency. However, for applications where efficiency is critical, a 500 kHz clock is an option.

Table 3. Switching Frequencies vs. R_{FREQ}

f_{SWITCH}	R_{FREQ}
250 kHz	484 kΩ
500 kHz	249 kΩ
750 kHz	168 kΩ
1 MHz	118 kΩ

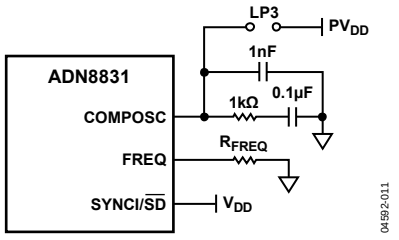

Figure 7. Switching Frequencies

MULTIPLE UNIT EVALUATION

The ADN8831 can drive one TEC or, in a multiple unit configuration, can drive multiple TECs. Details for connecting multiple devices together are available in the ADN8831 data sheet. Access to the connection pins for synchronizations and phase assignment is available through the PHASE, SYNCO, and SYNCIN solder pads located in the center of the evaluation board.

If the system noise is significant, change the 1 MΩ resistors of the slaves to 15% (136 kΩ) higher than the 118 kΩ recommended for the master ADN8831. For details, contact your local Analog Devices, Inc. sales office.

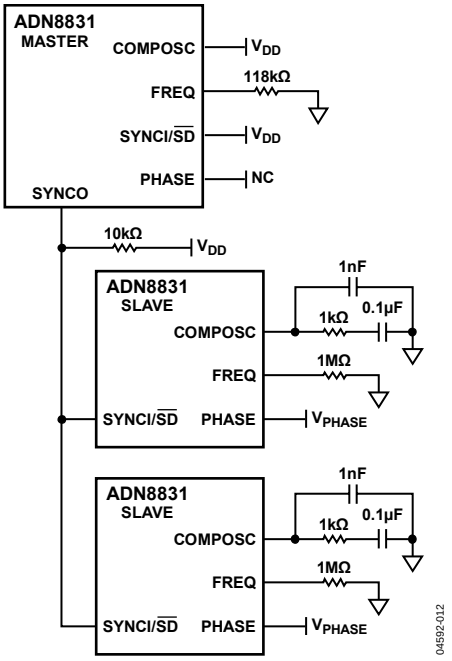

Figure 8. Multiple Unit Configuration

EVALUATION BOARD LAYOUT

Figure 10 through Figure 12 show the layout of the ADN8831 evaluation board.

Seven important guidelines are helpful when designing an ADN8831 evaluation board layout. Refer to Figure 9 for the part numbers listed here.

1. The ground terminals of decoupling capacitors from the PVDD to PGND and the PWM LC output filter capacitors must be tied together to reduce the power rail ripple. Using PCB traces or a ground plane (with long current paths) to connect these two components may generate, rather than reduce, the power rail ripple (supply pumping).
2. The two source terminals of the PWM MOSFETs must be connected directly or through a thick trace (>1 mm) to the terminals of the power supply decoupling capacitors (C16 and C19).
3. It is not necessary to use a 4-layer PCB for the circuit; 2-layer boards are sufficient (EVAL-ADN8831 uses a 2-layer PCB layout). Several recommendations to consider when using a 4-layer PCB follow.
    - Use one internal layer as the ground plane, the other internal layer for signal traces. Use both top and bottom layers as heat sinks for the ADN8831 IC, the output filter inductor, and the output MOSFETs (both on the linear and on the PWM sides).
    - Avoid conducting high current on the ground plane.
    - Always differentially run the PCB traces for critical signal paths. For example, run a dedicated parallel trace for the analog ground (AGND) with the R2 Pin 1 trace; both are for connecting the two terminals of the thermistor. This ensures that any interference coupled on the thermistor traces can cancel each other.
    - The low frequency temperature control circuit can be degraded easily by high frequency interference due to the rectifier effect. This effect refers to the phenomenon that occurs when a high frequency signal interferes with a low frequency circuit; the interference signal is rectified, or coupled, onto dc or lower frequency signals, thus affecting the operation of the circuit. When high frequency interference is unavoidable, use a small capacitor of up to 100 nF con-nected across the thermistor and mounted close to the controller to decouple the high frequency interference.
4. Ensure that the power supply decoupling capacitors have a total value of >40 µF. SMT multilayer ceramic capacitors of type X5R or X7R are the recommended capacitors. These types of capacitors have stable capacitance over temperature and very low equivalent series resistance (ESR).
5. The resistor placed between AVDD and PVDD is 1 Ω to 10 Ω in value.
6. Design the AGND and PGND carefully and connect both grounds at where the lowest current density exists on the PCB.
7. Because the ADN8831 and the MOSFETs take huge amounts of current, heat can build up quickly. For stable component performance, a metal heat sink design can relieve the component heat dissipation problem, especially at the PWM MOSFET side. When designing your layout, it is good practice to leave adequate space between the components. To ensure that your heat sink design is adequate, contact Analog Devices for design review support of your layout before fabricating the PCB.

EVALUATION BOARD SCHEMATIC AND ARTWORK

Figure 9 shows the schematic of the ADN8831 evaluation board (Version 3.1). Note that THPAD, shown as Pin 33 in this schematic, refers to the exposed thermal pad underneath the chip set. Connect THPAD to AGND to dissipate heat.

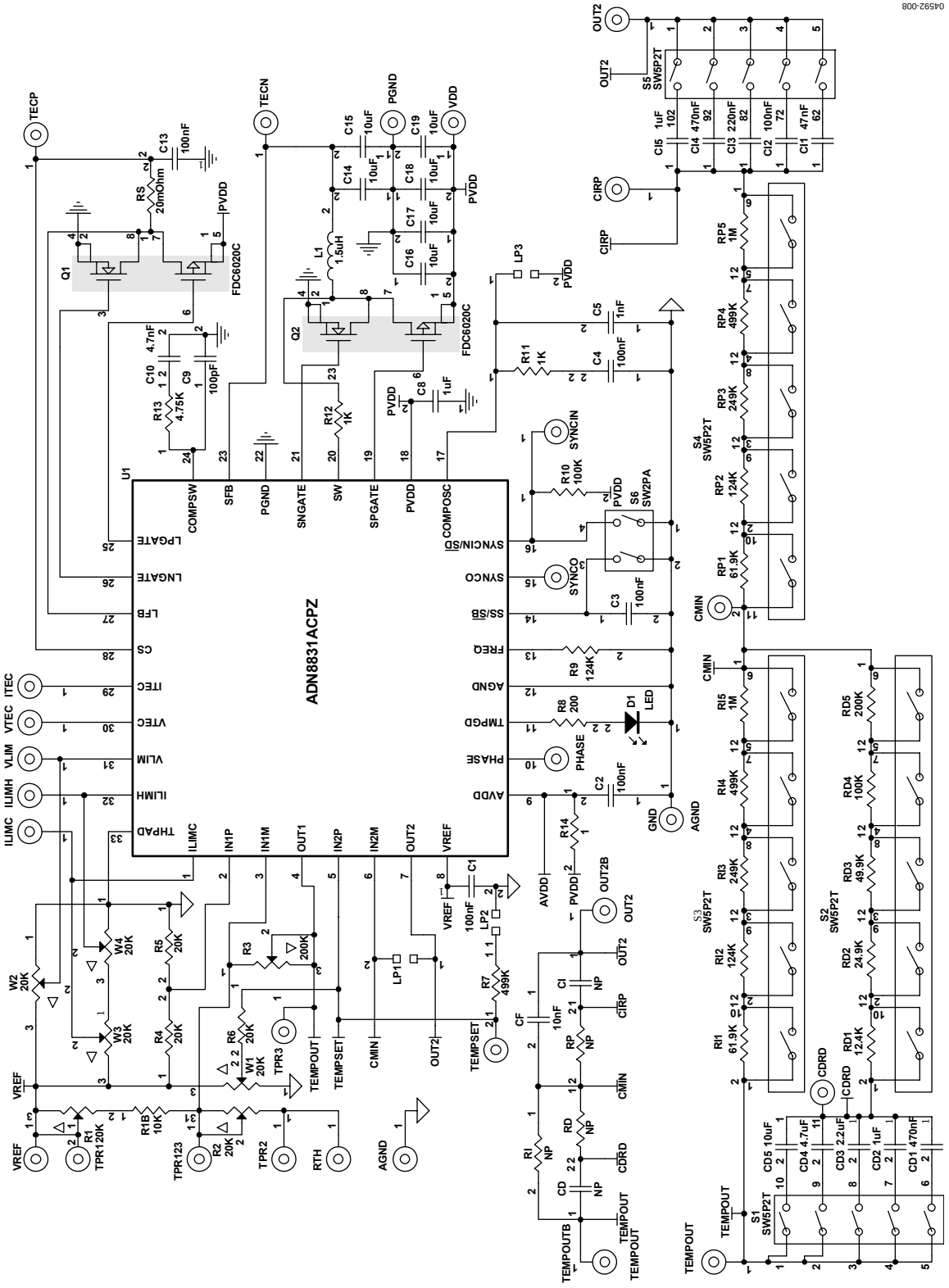

Figure 9. ADN8831 Evaluation Board Schematic

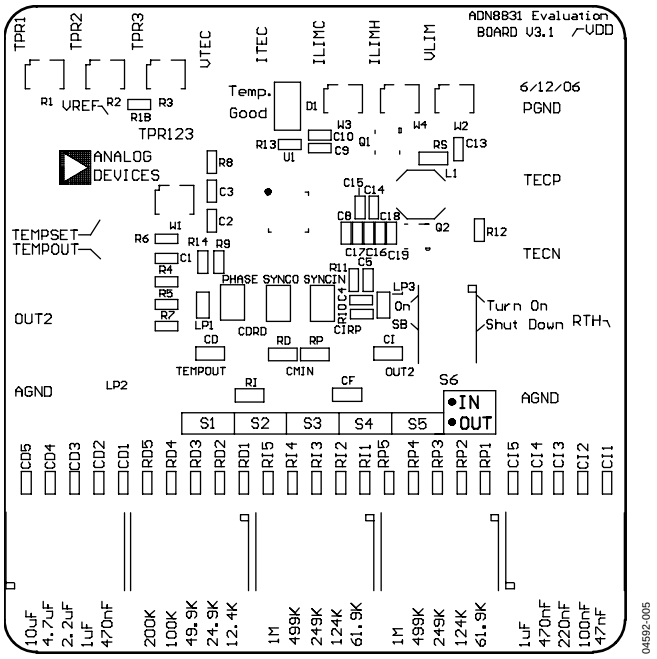

Figure 10. Top Layer Silkscreen

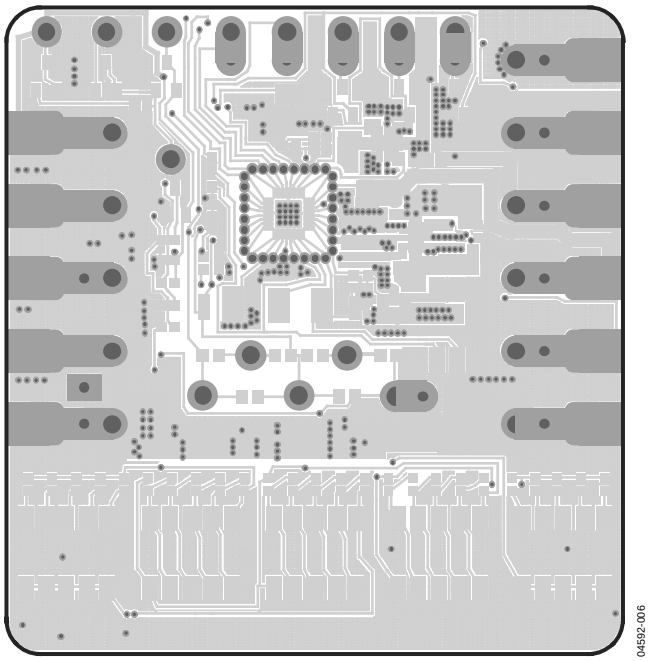

Figure 11. Top Layer Layout

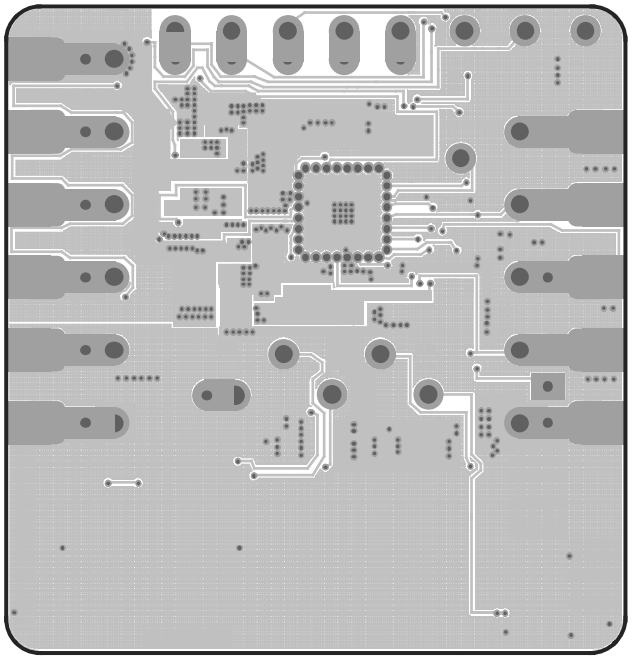

Figure 12. Bottom Layer Layout (Mirrored)

NOTES

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