



THE DATASHEET OF EPC9030



DESCRIPTION

The development board is in a half bridge topology with onboard gate drives, featuring the EPC8000 family of high frequency enhancement mode (eGaN[®]) field effect transistors (FETs). The purpose of these development boards is to simplify the evaluation process of the EPC8000 family of eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The development board is 2" x 1.5" and contains two eGaN FETs in a half bridge configuration using the Texas Instruments LM5113 gate driver.

For more information on the EPC8000 family of eGaN FETs, please refer to the datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

| SYMBOL | PARAMETER | CONDITIONS | | UNITS |
|------------------|--------------------------------------|--|---|-------|
| | | MIN | MAX | |
| V _{DD} | Gate Drive Input Supply Range | 7 | 12 | V |
| V _{IN} | Bus Input Voltage Range | 40 V devices; EPC9024, EPC9027, EPC9028 65 V devices; EPC9022, EPC9025, EPC9029 | 45* | V |
| V _{OUT} | Switch Node Output Voltage | 100 V devices; EPC9023, EPC9030 40 V devices; EPC9024, EPC9027, EPC9028 65 V devices; EPC9022, EPC9025, EPC9029 | 100 | V |
| I _{OUT} | Switch Node Output Current | 40 V device EPC9024 40 V device EPC9027 40 V device EPC9028 65 V device EPC9022 65 V device EPC9025 65 V device EPC9029 | 3.5* 3.5* 2.2* 2.2* 1.6* A | A |
| V _{PM} | PWM Logic Input Voltage Threshold | Input High 100 V device EPC9030 | 3.5 | V |
| F _{MIN} | Minimum Switching Frequency | Bootstrap Capacitor Limited | 500 | KHz |
| | Minimum High State Input Pulse Width | | 20 | ns |
| | Minimum Low State Input Pulse Width | | 50† | ns |

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermal.
† Limited by time needed to refresh high side bootstrap supply voltage.

THERMAL CONSIDERATIONS

The development board showcases the EPC8000 family of eGaN FET. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The development board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE: The development board does not have any current or thermal protection on board.

Quick Start Procedure

The development board is easy to set up to evaluate the performance of the eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

- With power off, connect the input power supply bus to +V_{IN} (J5, J6) and ground / return to -V_{IN} (J7, J8).
- With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
- With power off, connect the gate drive input to +V_{DD} (J1, Pin-1) and ground return to -V_{DD} (J1, Pin-2).
- With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
- Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
- Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage on V_{OUT} as indicated in the table below:

| | | |
|-------------------|------------------|-------------------|
| a. EPC9022, 65 V | d. EPC9025, 65 V | g. EPC9029, 65 V |
| b. EPC9023, 100 V | e. EPC9027, 40 V | h. EPC9030, 100 V |
| c. EPC9024, 40 V | f. EPC9028, 40 V | |
- Turn on the controller / PWM input source and probe switching node to see switching operation.
- Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
- For shutdown, please follow steps in reverse.

NOTE: When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

Demonstration Board
EPC9022/23/24/25/27/28/29/30
Quick Start Guide
Half Bridge with Gate Drive for EPC8000 Family

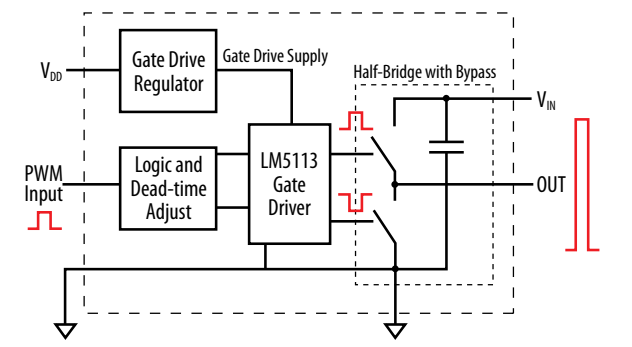


Figure 1: Block Diagram of Development Board



Figure 4: Typical Waveforms for VIN = 28 V to 3.3 V/4 A (5 MHz) Buck converter
CH2: (V_{OUT}) Switch node voltage — CH4: V_{PM} Input voltage

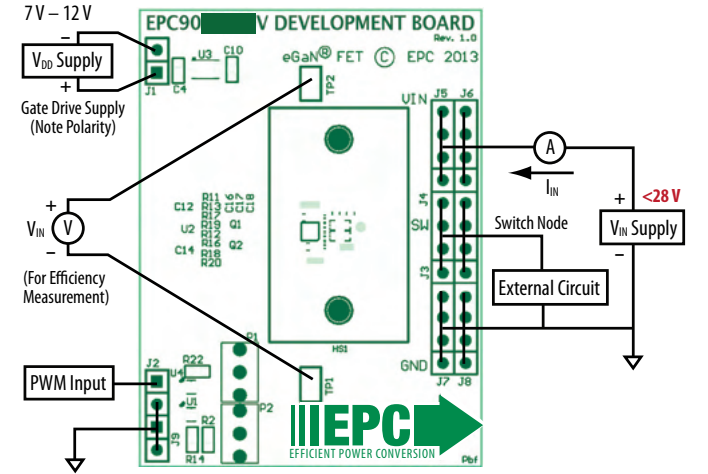


Figure 2: Proper Connection and Measurement Setup

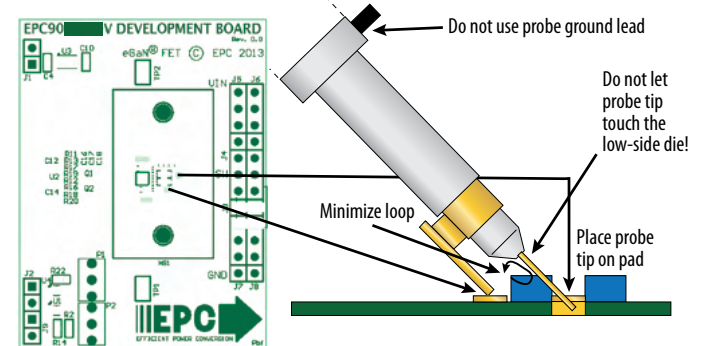


Figure 3: Proper Measurement of Switch Node – OUT

Demonstration Board
EPC9022/23/24/25/27/28/29/30
Quick Start Guide

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DESCRIPTION

Table 1: Performance Summary (TA = 25°C)

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|------------------|-----------------------------------|--|------|-----|-------|
| V _{co} | Gate Drive Input Supply Range | When using 40 V devices; EPC8004, EPC8007, EPC8008 | 28* | 12 | V |
| V _{in} | Bus Input Voltage Range | When using 40 V devices; EPC8004, EPC8007, EPC8008 | 45* | 70* | V |
| | | When using 55 V devices; EPC8002, EPC8005, EPC8009 | 40 | 65 | V |
| | | When using 100 V devices; EPC8003, EPC8010 | 40 | 100 | V |
| V _{out} | Switch Node Output Voltage | When using 100 V devices; EPC8003, EPC8010 | 4.4 | | V |
| | | When using 40 V device EPC8004 | | | V |
| | | When using 40 V device EPC8007 | 3.5* | | V |
| | | When using 40 V device EPC8008 | 2.2* | | V |
| | | When using 40 V device EPC8009 | 2.2* | | V |
| | | When using 40 V device EPC8005 | 1.6* | | V |
| | | When using 55 V device EPC8002 | 2.2* | | V |
| | | When using 55 V device EPC8005 | 2.2* | | V |
| | | When using 55 V device EPC8009 | 3.5* | | V |
| | | When using 100 V device EPC8003 | 2.2* | | V |
| | | When using 100 V device EPC8010 | 3.2* | | V |
| V _{pm} | PWM Logic Input Voltage Threshold | Input 'High' | 3.5 | 6 | V |
| | | Input 'Low' | 0 | 1.5 | V |
| | | Minimum 'High' State Input Pulse Width | 20 | | ns |
| | | Minimum 'Low' State Input Pulse Width | 50† | | ns |

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with subject to switching frequency, bus voltage and thermal.
 † Limited by time needed to refresh high side bootstrap supply voltage.

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- With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
- Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
- Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage on V_{OUT} as indicated in the table below:

| | | |
|-------------------|------------------|-------------------|
| a. EPC9022, 65 V | d. EPC9025, 65 V | g. EPC9029, 65 V |
| b. EPC9023, 100 V | e. EPC9027, 40 V | h. EPC9030, 100 V |
| c. EPC9024, 40 V | f. EPC9028, 40 V | |
- Turn on the controller / PWM input source and probe switching node to see switching operation.
- Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
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NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

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Demonstration Board EPC9022/23/24/25/27/28/29/30 Quick Start Guide Half Bridge with Gate Drive for EPC8000 Family

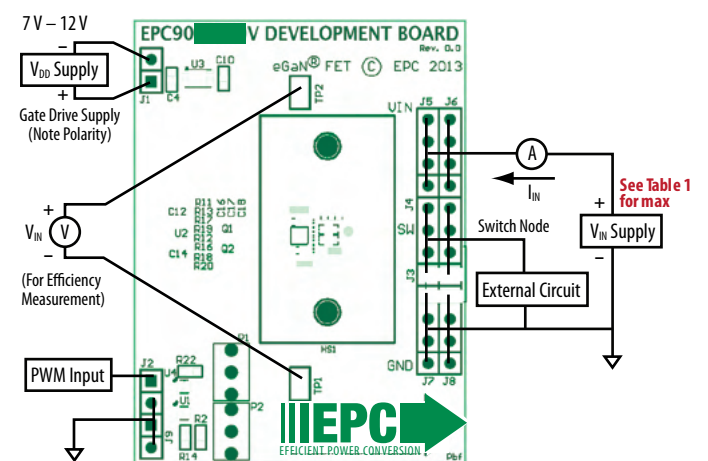


Figure 2: Proper Connection and Measurement Setup

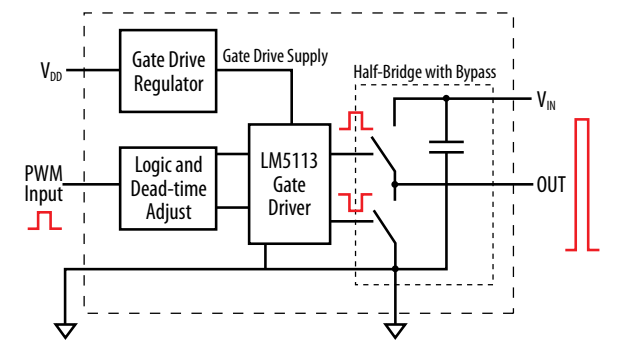


Figure 1: Block Diagram of Development Board

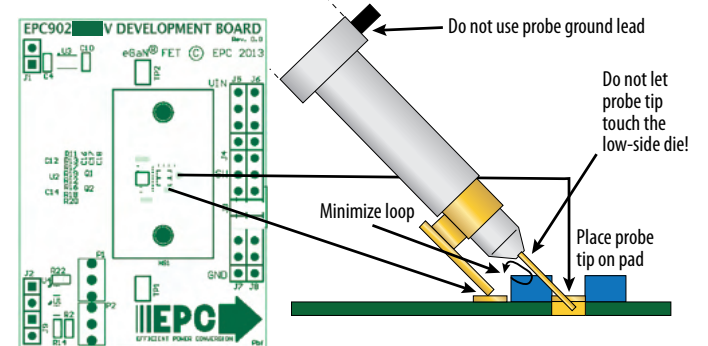


Figure 3: Proper Measurement of Switch Node – OUT

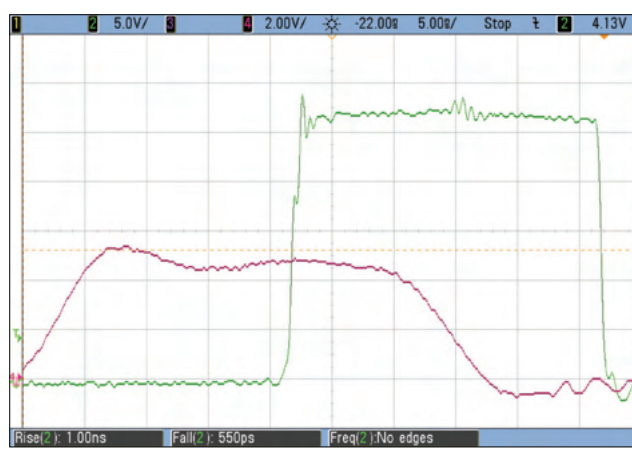


Figure 4: Typical Waveforms for V_{IN} = 28 V to 3.3 V/4 A (5 MHz) Buck converter
 CH2: (V_{OUT}) Switch node voltage — CH4: V_{PWM} Input voltage

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| V _{IN} | Bus Input Voltage Range | 40 V devices; EPC9024, EPC9027, EPC9028 65 V devices; EPC9022, EPC9025, EPC9029 100 V devices; EPC9023, EPC9030 | 40 | 70* | V |
| V _{OUT} | Switch Node Output Voltage | 40 V devices; EPC9024, EPC9027, EPC9028 65 V devices; EPC9022, EPC9025, EPC9029 100 V devices; EPC9023, EPC9030 | 65 | 100 | V |
| I _{OUT} | Switch Node Output Current | 40 V device EPC9027 40 V device EPC9024 40 V device EPC9028 65 V device EPC9022 65 V device EPC9025 65 V device EPC9029 100 V device EPC9023 | 3.5* | 4.4* | A |
| V _{PWM} | PWM Logic Input Voltage Threshold | Input High 100 V device EPC9029 | 3.5 | 6 | V |
| F _{MIN} | Minimum Switching Frequency | Bootstrap Capacitor Limited | 500 | | KHz |
| | Minimum High State Input Pulse Width | | 20 | | ns |
| | Minimum Low State Input Pulse Width | | 50† | | ns |

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Demonstration Board

Quick Start Guide

EPC9022/23/24/25/27/28/29/30

Half Bridge with Gate Drive for EPC8000 Family

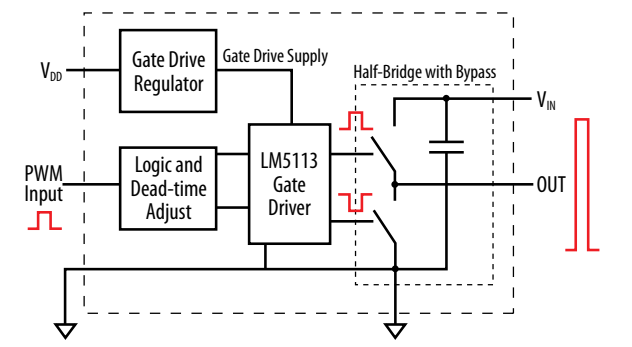


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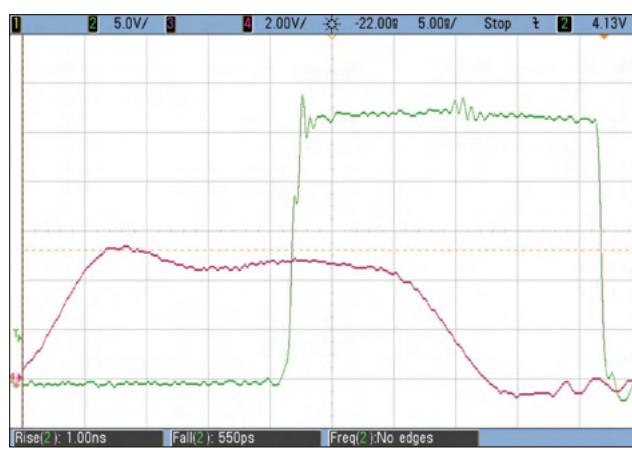


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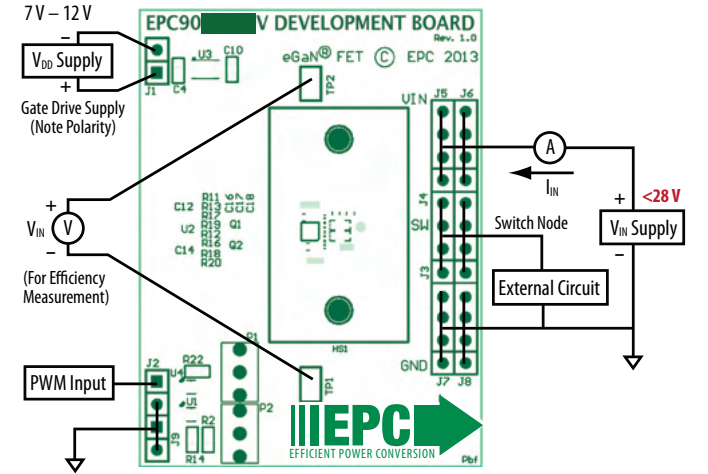


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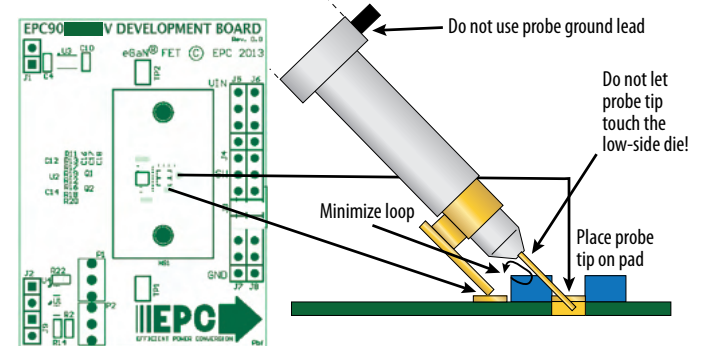


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Table 2 : Bill of Material

| Item | Qty | Reference | Part Description | Manufacturer / Part # |
|------|-----|------------------------|---------------------------------|------------------------------|
| 1 | 3 | C4, C10, C11 | Capacitor, 1uF, 10%, 25V, X5R | Murata, GRM188R61E105KA12D |
| 2 | 2 | C6, C7 | Capacitor, 100pF, 5%, 50V, NP0 | Kemet, C0402C101K5GACTU |
| 3 | 1 | C12 | Capacitor, 22nF, 10%, 25V, X5R | TDK, C1005X5R1E223K050BA |
| 4 | 1 | C14 | Capacitor, 0.1uF, 10%, 25V, X5R | TDK, C1005X5R1E104K |
| 5 | 3 | C16, C17, C18 | Capacitor, - SEE TABLE 3 | SEE TABLE 3 |
| 6 | 1 | C13 | Capacitor, 1uF, 10%, 25V, X5R | Murata, GRM188R61E105KA12D |
| 7 | 1 | C21 | Capacitor, - SEE TABLE 3 | SEE TABLE 3 |
| 8 | 2 | D1, D2 | Schottky Diode, 30V | Diodes Inc., SDM03U40-7 |
| 9 | 3 | J1, J2, J9 | Connector | 2pins of Tyco, 4-103185-0 |
| 10 | 6 | J3, J4, J5, J6, J7, J8 | Connector | FCI, 68602-224HLF |
| 11 | 2 | Q1, Q2 | eGaN® FET - SEE TABLE 3 | SEE TABLE 3 |
| 12 | 1 | R1 | Resistor, 10.0K, 5%, 1/8W | Stackpole, RMCF0603FT10K0 |
| 13 | 2 | R2, R15 | Resistor, 0 Ohm, 1/8W | Stackpole, RMCF0603ZTOR00 |
| 14 | 2 | R4, R5 | Resistor, 7.5 Ohm, 5%, 1/16W | Stackpole, RMCF0603JT7R50 |
| 15 | 2 | TP1, TP2 | Test Point | Keystone Elect, 5015 |
| 16 | 1 | U1 | I.C., Logic | Fairchild, NC7SZ00L6X |
| 17 | 1 | U2 | I.C., Gate driver | Texas Instruments, LM5113 |
| 18 | 1 | U3 | I.C., Regulator | Microchip, MCP1703T-5002E/MC |
| 19 | 1 | U4 | I.C., Logic | Fairchild, NC7SZ08L6X |
| 20 | 0 | HS1 | Optional Heatsink | HeatSink15mmX15mm |
| 21 | 0 | R14, R22 | Optional Resistor | |
| 22 | 0 | P1, P2 | Optional Potentiometer | PV37Y |

Table 3: Variable BOM Components

| Board Number | Item | Qty | Reference | Part Description | Manufacturer / Part # |
|--------------|------|-----|---------------|-----------------------------------|--------------------------|
| EPC9022 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X7R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8002 |
| EPC9023 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X7R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8003 |
| EPC9024 | 5 | 3 | C16, C17, C18 | Capacitor, 0.1uF, 20%, 50V, X5R | TDK, C1005X5R1H104K050BB |
| | 7 | 1 | C21 | Capacitor, 4.7uF, 10%, 50V, X5R | TDK, C2012X5R1H475K125AB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8004 |
| EPC9025 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X7R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8005 |
| EPC9027 | 5 | 3 | C16, C17, C18 | Capacitor, 0.1uF, 20%, 50V, X5R | TDK, C1005X5R1H104K050BB |
| | 7 | 1 | C21 | Capacitor, 4.7uF, 10%, 50V, X5R | TDK, C2012X5R1H475K125AB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8007 |
| EPC9028 | 5 | 3 | C16, C17, C18 | Capacitor, 0.1uF, 20%, 50V, X5R | TDK, C1005X5R1H104K050BB |
| | 7 | 1 | C21 | Capacitor, 4.7uF, 10%, 50V, X5R | TDK, C2012X5R1H475K125AB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8008 |
| EPC9029 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X7R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8009 |
| EPC9030 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X7R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8010 |

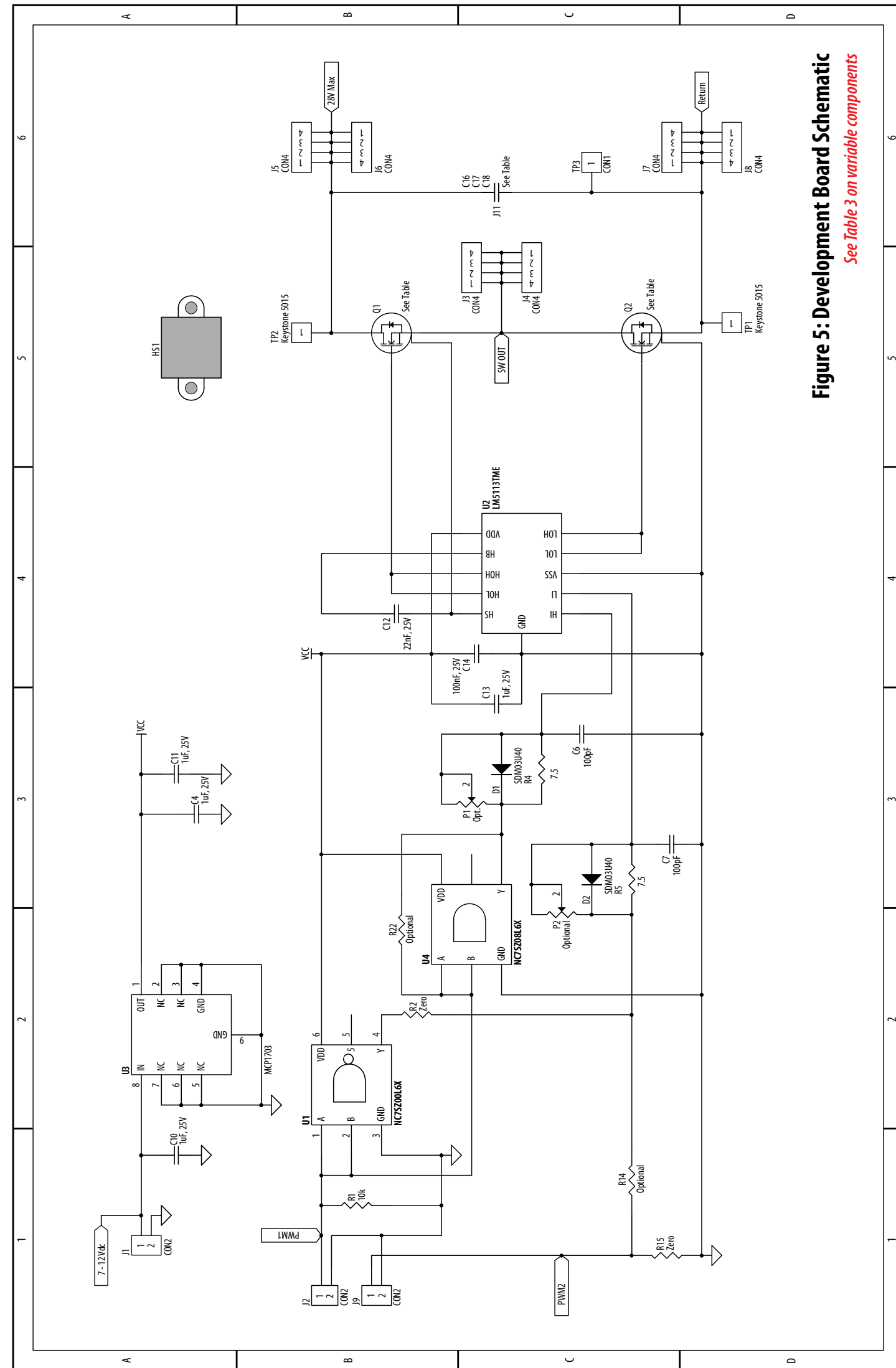
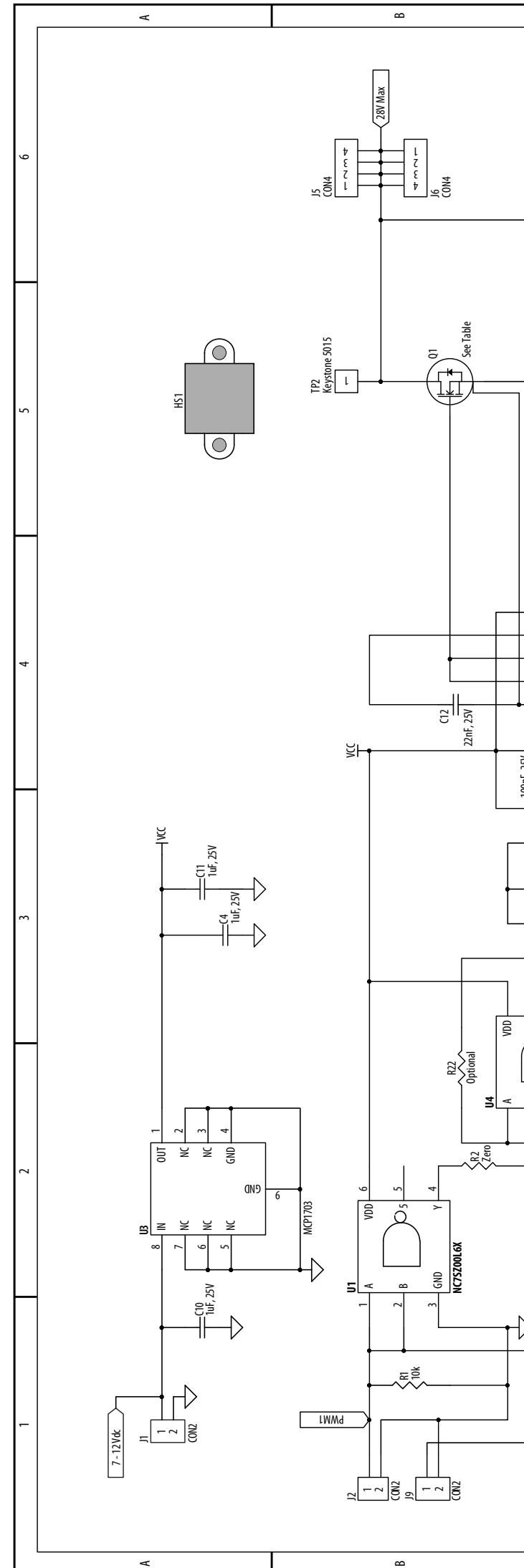


Table 2 : Bill of Material

| Item | Qty | Reference | Part Description | Manufacturer / Part # |
|------|-----|------------------------|---------------------------------|------------------------------|
| 1 | 3 | C4, C10, C11 | Capacitor, 1uF, 10%, 25V, X5R | Murata, GRM188R61E105KA12D |
| 2 | 2 | C6, C7 | Capacitor, 100pF, 5%, 50V, NP0 | Kemet, C0402C101K5GACTU |
| 3 | 1 | C12 | Capacitor, 22nF, 10%, 25V, X5R | TDK, C1005X5R1E223K050BA |
| 4 | 1 | C14 | Capacitor, 0.1uF, 10%, 25V, X5R | TDK, C1005X5R1E104K |
| 5 | 3 | C16, C17, C18 | Capacitor, - SEE TABLE 3 | SEE TABLE 3 |
| 6 | 1 | C13 | Capacitor, 1uF, 10%, 25V, X5R | Murata, GRM188R61E105KA12D |
| 7 | 1 | C21 | Capacitor, - SEE TABLE 3 | SEE TABLE 3 |
| 8 | 2 | D1, D2 | Schottky Diode, 30V | Diodes Inc., SDM03U40-7 |
| 9 | 3 | J1, J2, J9 | Connector | 2pins of Tyco, 4-103185-0 |
| 10 | 6 | J3, J4, J5, J6, J7, J8 | Connector | FCI, 68602-224HLF |
| 11 | 2 | Q1, Q2 | eGaN® FET - SEE TABLE 3 | SEE TABLE 3 |
| 12 | 1 | R1 | Resistor, 10.0K, 5%, 1/8W | Stackpole, RMCF0603FT10K0 |
| 13 | 2 | R2, R15 | Resistor, 0 Ohm, 1/8W | Stackpole, RMCF0603ZT0R00 |
| 14 | 2 | R4, R5 | Resistor, 7.5 Ohm, 5%, 1/16W | Stackpole, RMCF0603JT7R50 |
| 15 | 2 | TP1, TP2 | Test Point | Keystone Elect, 5015 |
| 16 | 1 | U1 | I.C., Logic | Fairchild, NC7SZ00L6X |
| 17 | 1 | U2 | I.C., Gate driver | Texas Instruments, LM5113 |
| 18 | 1 | U3 | I.C., Regulator | Microchip, MCP1703T-5002E/MC |
| 19 | 1 | U4 | I.C., Logic | Fairchild, NC7SZ08L6X |
| 20 | 0 | HS1 | Optional Heatsink | HeatSink15mmX15mm |
| 21 | 0 | R14, R22 | Optional Resistor | |
| 22 | 0 | P1, P2 | Optional Potentiometer | PV37Y |

Table 3: Variable BOM Components

| Board Number | Item | Qty | Reference | Part Description | Manufacturer / Part # |
|--------------|------|-----|---------------|-----------------------------------|--------------------------|
| EPC9022 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X5R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, C1005X5R1H104K050BB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8002 |
| EPC9023 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X5R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8003 |
| EPC9024 | 5 | 3 | C16, C17, C18 | Capacitor, 0.1uF, 20%, 50V, X5R | TDK, C1005X5R1H104K050BB |
| | 7 | 1 | C21 | Capacitor, 4.7uF, 10%, 50V, X5R | TDK, C2012X5R1H475K125AB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8004 |
| EPC9025 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X5R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8005 |
| EPC9027 | 5 | 3 | C16, C17, C18 | Capacitor, 0.1uF, 20%, 50V, X5R | TDK, C1005X5R1H104K050BB |
| | 7 | 1 | C21 | Capacitor, 4.7uF, 10%, 50V, X5R | TDK, C2012X5R1H475K125AB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8007 |
| EPC9028 | 5 | 3 | C16, C17, C18 | Capacitor, 0.1uF, 20%, 50V, X5R | TDK, C1005X5R1H104K050BB |
| | 7 | 1 | C21 | Capacitor, 4.7uF, 10%, 50V, X5R | TDK, C2012X5R1H475K125AB |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8008 |
| EPC9029 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X5R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8009 |
| EPC9030 | 5 | 3 | C16, C17, C18 | Capacitor, 0.01uF, 20%, 100V, X5R | TDK, C1005X7S2A103M050BB |
| | 7 | 1 | C21 | Capacitor, 1uF, 10%, 100V, X7R | TDK, CGA4J3X7S2A105K125A |
| | 11 | 2 | Q1, Q2 | eGaN® FET | EPC8010 |



DESCRIPTION

Table 1: Performance Summary (TA = 25°C)

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|-----------|--|---|------|-----|-------|
| V_{CO} | Gate Drive Input Supply Range | | 7 | 12 | V |
| V_{IN} | Bus Input Voltage Range | When using 40 V devices; EPC8004, EPC8007, EPC8008 When using 55 V devices; EPC8002, EPC8005, EPC8009 When using 100 V devices; EPC8003, EPC8010 | 40 | 70* | V |
| V_{OUT} | Switch Node Output Voltage | When using 40 V devices; EPC8004, EPC8007, EPC8008 When using 55 V devices; EPC8002, EPC8005, EPC8009 When using 100 V devices; EPC8003, EPC8010 | 40 | 65 | V |
| I_{OUT} | Switch Node Output Current | When using 40 V device EPC8007 When using 40 V device EPC8008 When using 55 V device EPC8002 When using 55 V device EPC8005 When using 55 V device EPC8009 When using 100 V device EPC8010 | 3.5* | 4.4 | A |
| V_{PWM} | PWM Logic Input Voltage Threshold | | 3.5 | 6 | V |
| | Minimum 'High' State Input Pulse Width | | 20 | | ns |
| | Minimum 'Low' State Input Pulse Width | | 50† | | ns |

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with subject to switching frequency, bus voltage and thermal.
† Limited by time needed to refresh high side bootstrap supply voltage.

The development board is in a half bridge topology with onboard gate drives, featuring the EPC8000 family of high frequency enhancement mode (eGaN®) field effect transistors (FETs). The purpose of these development boards is to simplify the evaluation process of the EPC8000 family of eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The development board is 2" x 1.5" and contains two eGaN FETs in a half bridge configuration using the Texas Instruments LM5113 gate driver.

For more information on the EPC8000 family of eGaN FETs, please refer to the datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Quick Start Procedure

The development board is easy to set up to evaluate the performance of the eGaN FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

- With power off, connect the input power supply bus to + V_{IN} (J5, J6) and ground / return to - V_{IN} (J7, J8).
- With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
- With power off, connect the gate drive input to + V_{DD} (J1, Pin-1) and ground return to - V_{DD} (J1, Pin-2).
- With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
- Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
- Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage on V_{OUT} as indicated in the table below:

| | | |
|-------------------|------------------|-------------------|
| a. EPC9022, 65 V | d. EPC9025, 65 V | g. EPC9029, 65 V |
| b. EPC9023, 100 V | e. EPC9027, 40 V | h. EPC9030, 100 V |
| c. EPC9024, 40 V | f. EPC9028, 40 V | |
- Turn on the controller / PWM input source and probe switching node to see switching operation.
- Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
- For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The development board showcases the EPC8000 family of eGaN FET. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The development board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The development board does not have any current or thermal protection on board.

Demonstration Board

Quick Start Guide

EPC9022/23/24/25/27/28/29/30

Half Bridge with Gate Drive for EPC8000 Family



Demonstration Board Notification

The EPC boards are intended for product evaluation purposes only and is not intended for commercial use. As an evaluation tool, it is not designed for compliance with the European Union directives on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not EPC compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant. No license are implied or granted under any patent right or other intellectual property whatsoever. EPC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind. EPC reserves the right at any time, without notice, to change said circuitry and specifications.

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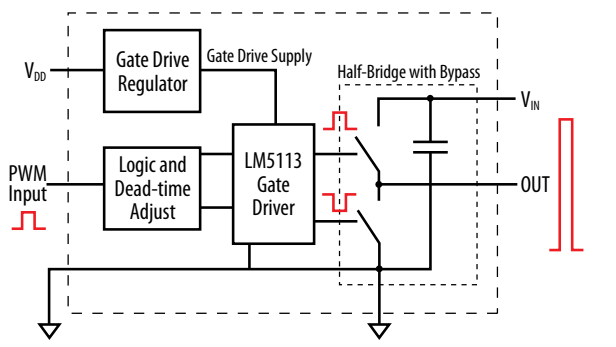


Figure 1: Block Diagram of Development Board



Figure 4: Typical Waveforms for $V_{IN} = 28\text{ V}$ to 3.3 V/4 A (5 MHz) Buck converter
CH2: (V_{OUT}) Switch node voltage — CH4: V_{PWM} Input voltage

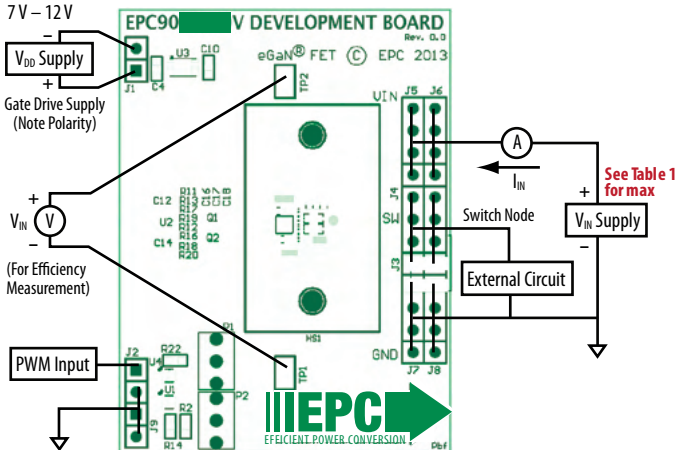


Figure 2: Proper Connection and Measurement Setup

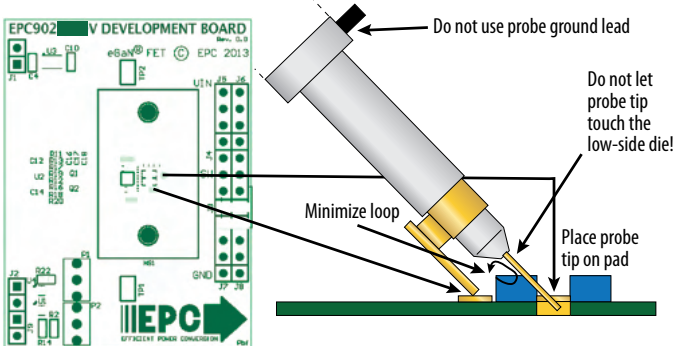



Figure 3: Proper Measurement of Switch Node – OUT

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