



**THE DATASHEET OF
IS64WV12816EDBLL-10CTLA3**



IS61WV12816EDBLL IS64WV12816EDBLL



128K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM WITH ECC

MAY 2020

FEATURES

- High-speed access time: 8, 10 ns
- Low Active Power: 85 mW (typical)
- Low Standby Power: 7 mW (typical) CMOS standby
- Single power supply
 - V_{DD} 2.4V to 3.6V (10 ns)
 - V_{DD} 3.3V \pm 10% (8 ns)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Automotive temperature support
- Lead-free available
- Error Detection and Error Correction

DESCRIPTION

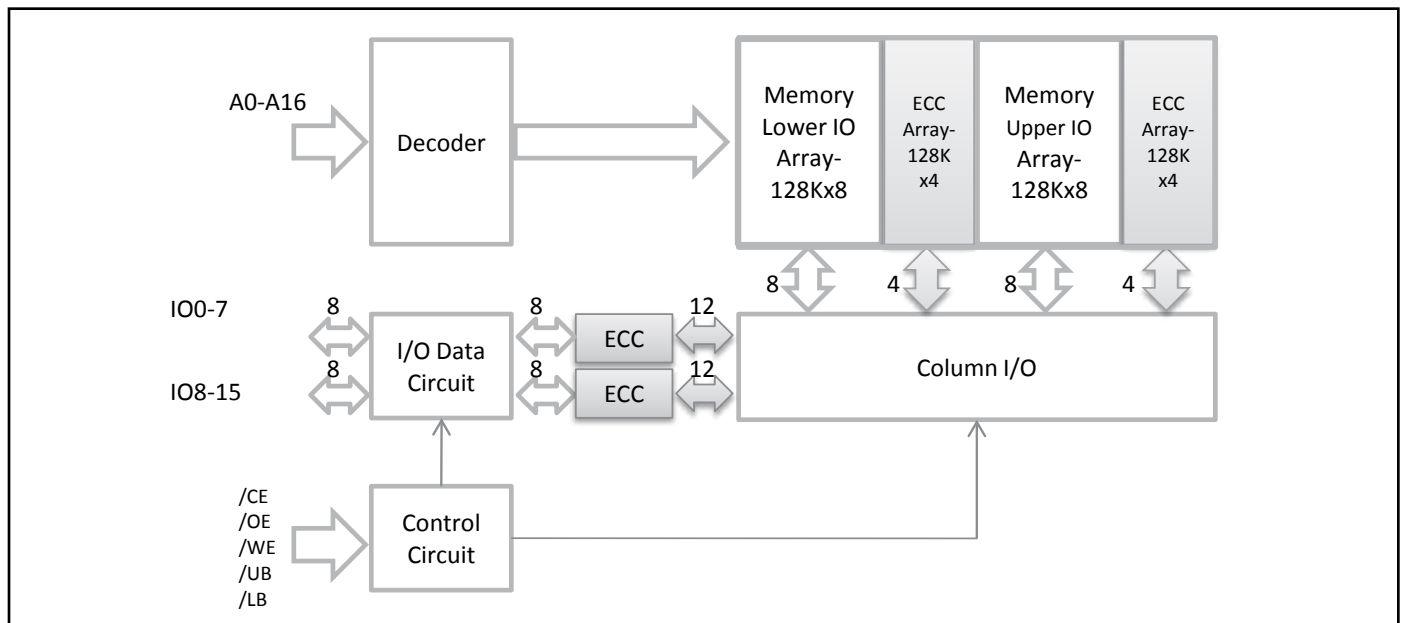
The *ISSI* IS61/64WV12816EDBLL is a high-speed, 2,097,152-bit static RAMs organized as 131,072 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS61/64WV12816EDBLL is packaged in the JEDEC standard 44-pin TSOP-II and 48-pin Mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM



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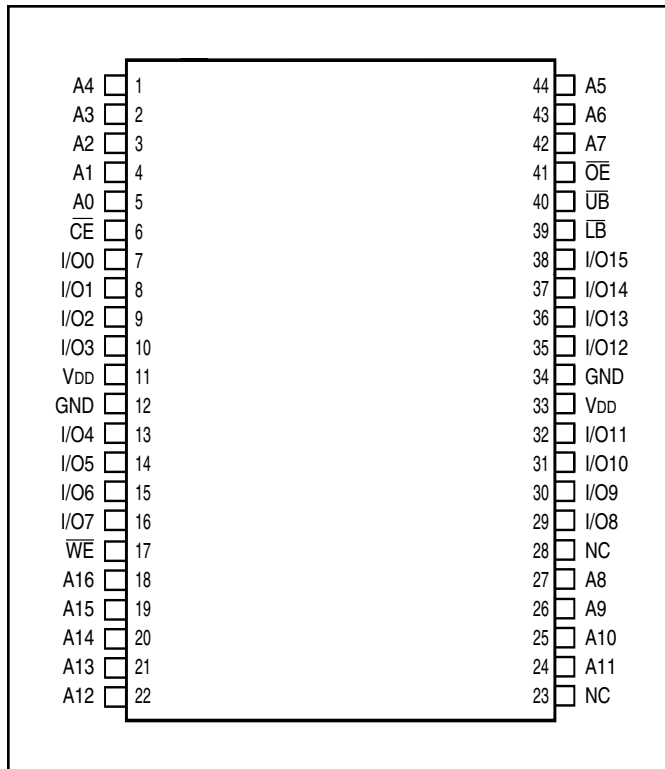
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | \overline{LB} | \overline{UB} | I/O PIN | | V_{DD} Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------|------------|--------------------|
| | | | | | | I/O0-I/O7 | I/O8-I/O15 | |
| Not Selected | X | H | X | X | X | High-Z | High-Z | I_{SB1}, I_{SB2} |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | I_{CC} |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | DOUT | High-Z | I_{CC} |
| | H | L | L | H | L | High-Z | DOUT | |
| | H | L | L | L | L | DOUT | DOUT | |
| Write | L | L | X | L | H | DIN | High-Z | I_{CC} |
| | L | L | X | H | L | High-Z | DIN | |
| | L | L | X | L | L | DIN | DIN | |

PIN CONFIGURATION
44-Pin TSOP (Type II) (T)

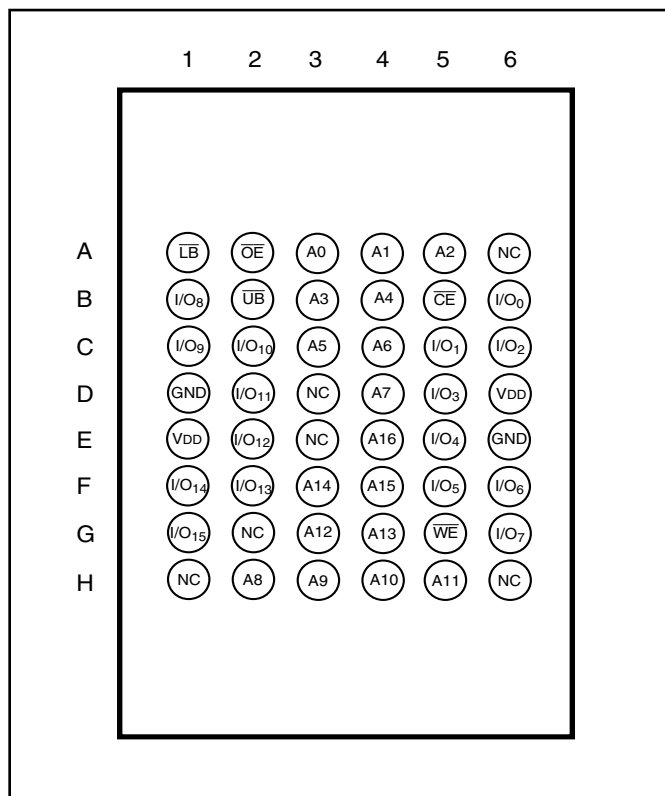


PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A16 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| V_{DD} | Power |
| GND | Ground |

PIN CONFIGURATION

48-Pin mini BGA (B)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A16 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| V _{DD} | Power |
| GND | Ground |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | V _{DD} Relates to GND | -0.3 to 4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC with hamming code for each byte
- Detect and correct one bit error per byte
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

OPERATING RANGE (V_{DD})¹

| Range | Ambient Temperature | IS61WV12816EDBLL V _{DD} (8, 10ns) | IS64WV12816EDBLL V _{DD} (10ns) |
|-----------------|---------------------|---|--|
| Industrial | -40°C to +85°C | 2.4V-3.6V (10ns) 3.3V ± 10% (8ns) | — |
| Automotive (A1) | -40°C to +85°C | — | 2.4V-3.6V |
| Automotive (A3) | -40°C to +125°C | — | 2.4V-3.6V |

Note:

1. Contact SRAM@issi.com for 1.8V option

IS61/64WV12816EDBLL

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 3.3V \pm 10\%$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------|----------------------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{DD} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | — | V |
| V_{OL} | Output LOW Voltage | $V_{DD} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
 V_{IH} (max.) = $V_{DD} + 0.3V$ DC; V_{IH} (max.) = $V_{DD} + 2.0V$ AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 2.4V-3.6V$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------|----------------------------------|---|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$ | 1.8 | — | V |
| V_{OL} | Output LOW Voltage | $V_{DD} = \text{Min.}, I_{OL} = 1.0 \text{ mA}$ | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.0 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
 V_{IH} (max.) = $V_{DD} + 0.3V$ DC; V_{IH} (max.) = $V_{DD} + 2.0V$ AC (pulse width < 10 ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | -8 | | -10 | | -20 | | Unit | |
|-----------|---|--|---------------------|------|------|------|------|------|------|----|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| I_{CC} | V_{DD} Dynamic Operating Supply Current | $V_{DD} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX}$ | Com. | — | 40 | — | 30 | — | 25 | mA |
| | | | Ind. | — | 45 | — | 35 | — | 30 | |
| | | | Auto. | — | — | — | 50 | — | 45 | |
| | | | typ. ⁽²⁾ | 21 | 21 | | | | | |
| I_{CC1} | Operating Supply Current | $V_{DD} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = 0$ | Com. | — | 20 | — | 20 | — | 20 | mA |
| | | | Ind. | — | 25 | — | 25 | — | 25 | |
| | | | Auto. | — | — | — | 40 | — | 40 | |
| I_{SB1} | TTL Standby Current (TTL Inputs) | $V_{DD} = \text{Max.}, V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH}, f = 0$ | Com. | — | 10 | — | 10 | — | 10 | mA |
| | | | Ind. | — | 15 | — | 15 | — | 15 | |
| | | | Auto. | — | — | — | 30 | — | 30 | |
| I_{SB2} | CMOS Standby Current (CMOS Inputs) | $V_{DD} = \text{Max.}, \overline{CE} \geq V_{DD} - 0.2V, V_{IN} \geq V_{DD} - 0.2V, \text{ or } V_{IN} \leq 0.2V, f = 0$ | Com. | — | 5 | — | 5 | — | 5 | mA |
| | | | Ind. | — | 6 | — | 6 | — | 6 | |
| | | | Auto. | — | — | — | 15 | — | 15 | |
| | | | typ. ⁽²⁾ | 1.5 | 1.5 | | | | | |

Note:

- At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, $f = 0$ means no input lines change.
- Typical values are measured at $V_{DD} = 3.0V, T_A = 25^\circ\text{C}$ and not 100% tested.

AC TEST CONDITIONS

| Parameter | Unit (2.4V-3.6V) |
|---|-----------------------|
| Input Pulse Level | 0.4V to $V_{DD}-0.3V$ |
| Input Rise and Fall Times | 1V/ ns |
| Input and Output Timing and Reference Level (V_{Ref}) | $V_{DD}/2$ |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

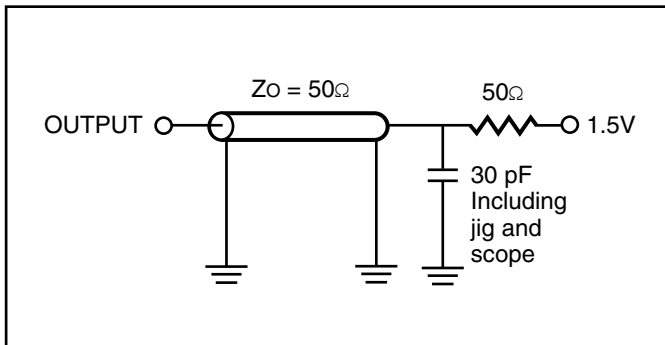


Figure 1.

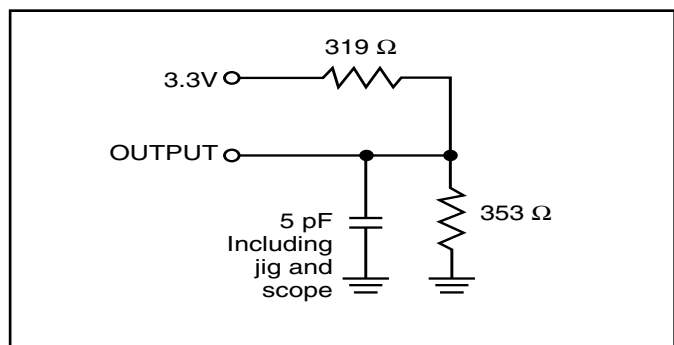


Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

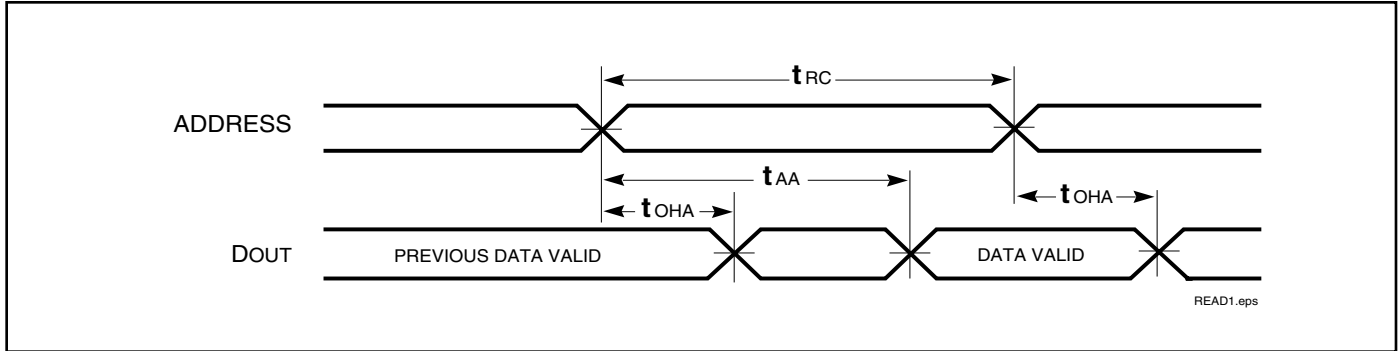
| Symbol | Parameter | -8 | | -10 | | -20 | | Unit |
|----------------------------------|--|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | 20 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | — | 20 | ns |
| t _{OHA} | Output Hold Time | 2.0 | — | 2.0 | — | 2.5 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 8 | — | 10 | — | 20 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 4.5 | — | 4.5 | — | 8 | ns |
| t _{HZOE} ⁽²⁾ | \overline{OE} to High-Z Output | — | 3 | — | 4 | 0 | 8 | ns |
| t _{LZOE} ⁽²⁾ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |
| t _{HZCE} ⁽²⁾ | \overline{CE} to High-Z Output | 0 | 3 | 0 | 4 | 0 | 8 | ns |
| t _{LZCE} ⁽²⁾ | \overline{CE} to Low-Z Output | 3 | — | 3 | — | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 5.5 | — | 6.5 | — | 8 | ns |
| t _{HZB} ⁽²⁾ | \overline{LB} , \overline{UB} to High-Z Output | 0 | 3 | 0 | 3 | 0 | 8 | ns |
| t _{LZB} ⁽²⁾ | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | 0 | — | 0 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 8 | — | 10 | — | 20 | ns |

Notes:

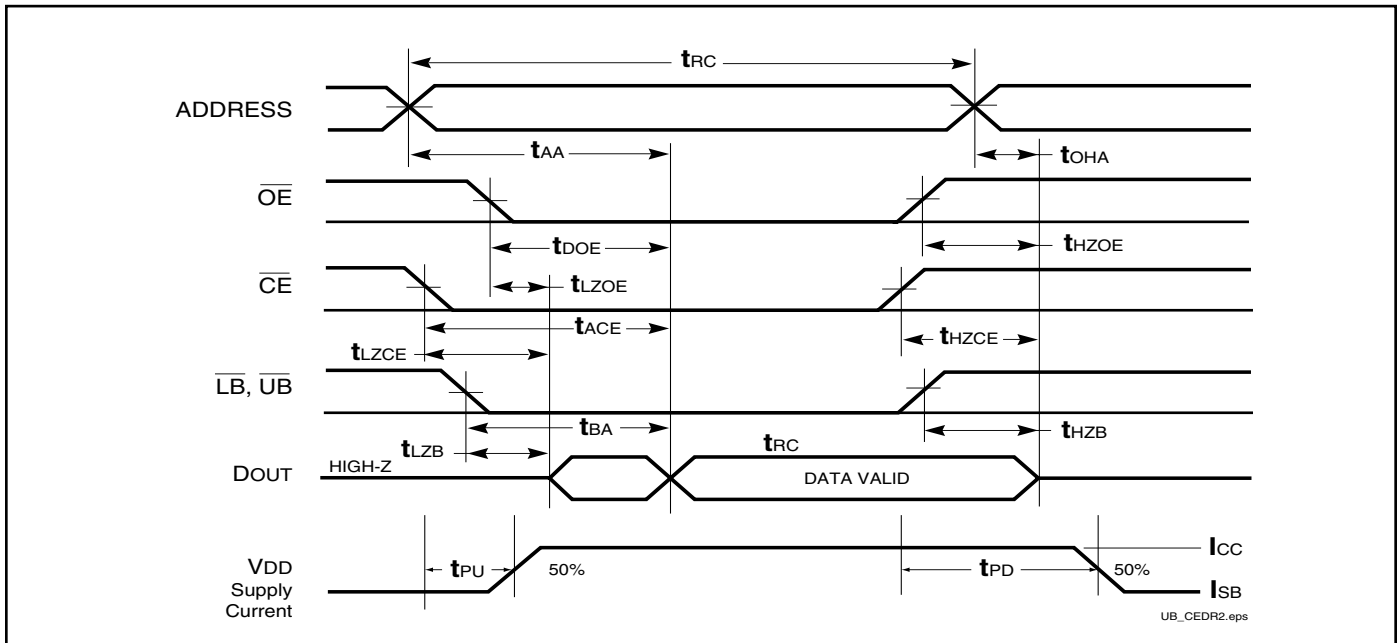
- Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
- Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

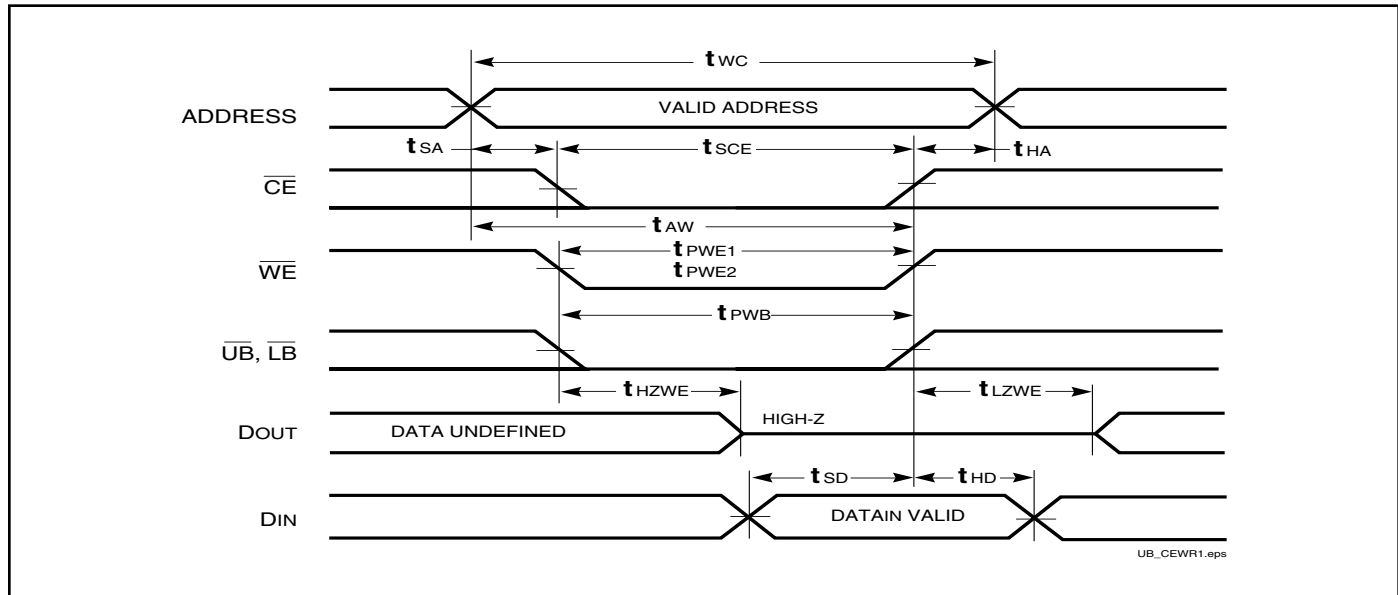
| Symbol | Parameter | -8 | | -10 | | -20 | | Unit |
|---------------------------------|---------------------------------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | 20 | — | ns |
| t _{SCE} | CE to Write End | 6.5 | — | 8 | — | 12 | — | ns |
| t _{AW} | Address Setup Time to Write End | 6.5 | — | 8 | — | 12 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | ns |
| t _{PWB} | LB, UB Valid to End of Write | 6.5 | — | 8 | — | 12 | — | ns |
| t _{PWE1} | WE Pulse Width | 6.5 | — | 8 | — | 12 | — | ns |
| t _{PWE2} | WE Pulse Width (OE = LOW) | 8 | — | 10 | — | 17 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | 9 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | ns |
| t _{HZWE⁽²⁾} | WE LOW to High-Z Output | — | 3.5 | — | 5 | — | 9 | ns |
| t _{LZWE⁽²⁾} | WE HIGH to Low-Z Output | 2 | — | 2 | — | 3 | — | ns |

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and UB or LB, and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

AC WAVEFORMS

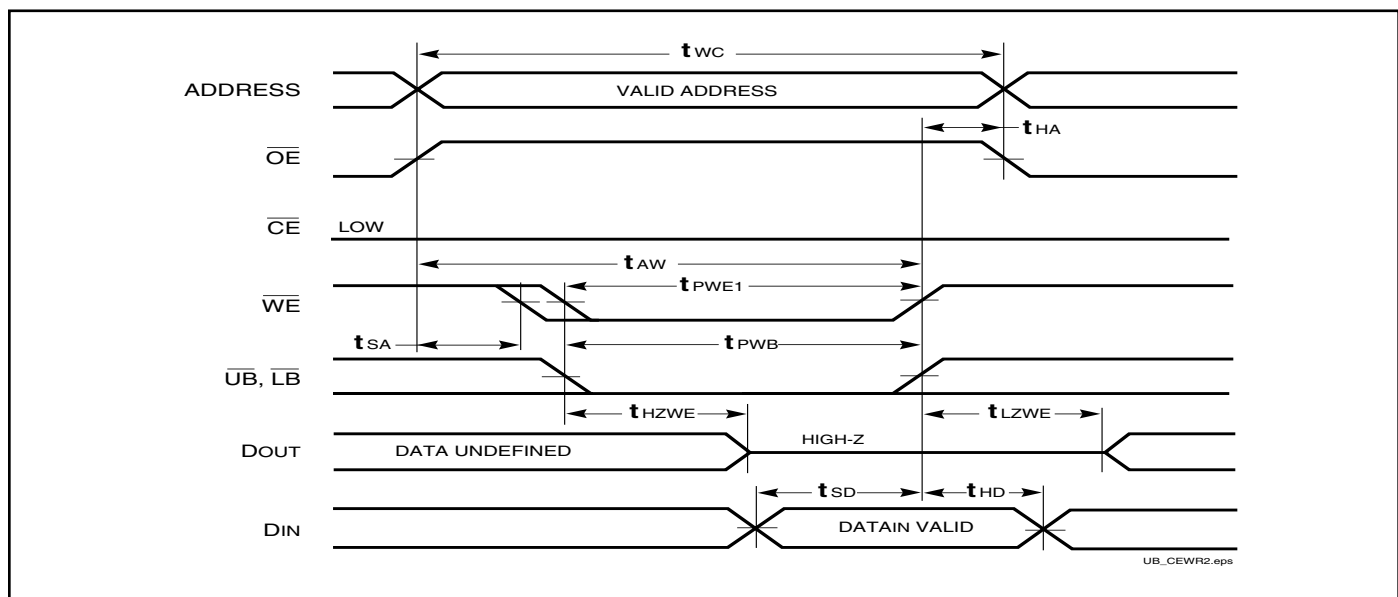
WRITE CYCLE NO. 1 (\overline{CE} Controlled, \overline{OE} is HIGH or LOW) ⁽¹⁾



Notes:

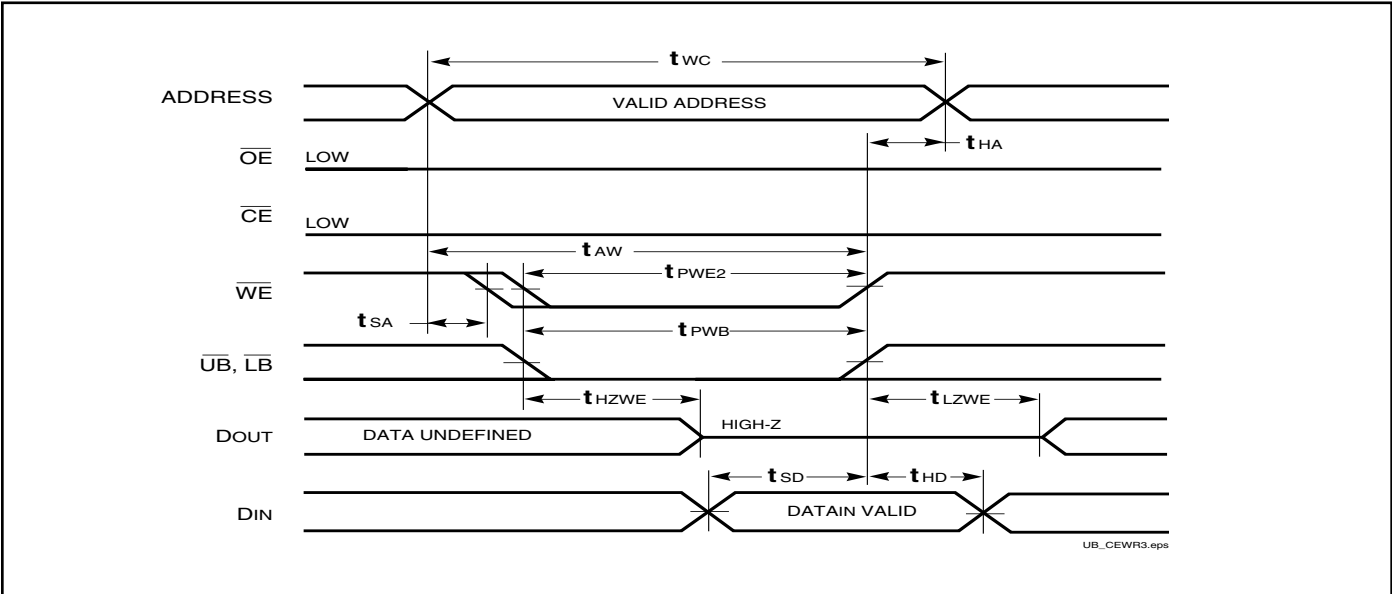
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. WRITE = (CE) [(LB) = (UB)] (WE).

WRITE CYCLE NO. 2 (\overline{WE} Controlled. \overline{OE} is HIGH During Write Cycle) ^(1,2)

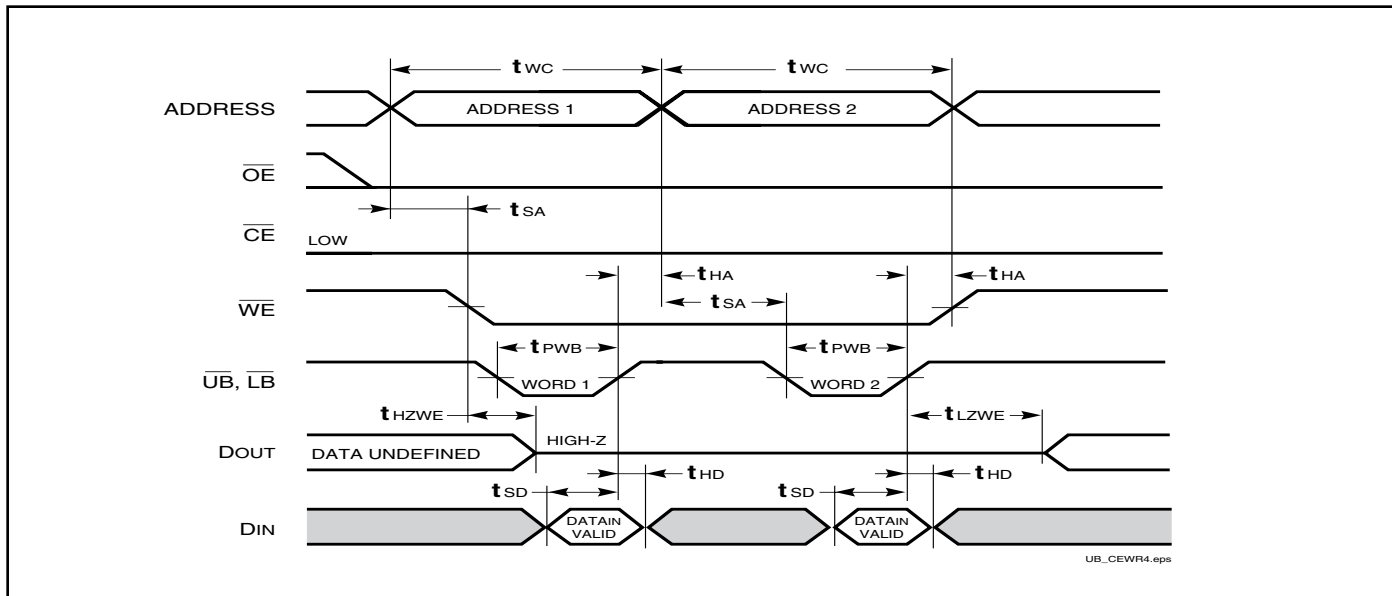


AC WAVEFORMS

WRITE CYCLE NO. 3 (\overline{WE} Controlled, \overline{OE} is LOW During Write Cycle) ⁽¹⁾



WRITE CYCLE NO. 4 (\overline{LB} , \overline{UB} Controlled, Back-to-Back Write) ^(1,3)



Notes:

1. The internal Write time is defined by the overlap of $\overline{CE} = \text{LOW}$, \overline{UB} and/or $\overline{LB} = \text{LOW}$, and $\overline{WE} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with \overline{OE} HIGH for a minimum of 4 ns before $\overline{WE} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. \overline{WE} may be held LOW across many address cycles and the \overline{LB} , \overline{UB} pins can be used to control the Write function.

IS61/64WV12816EDBLL

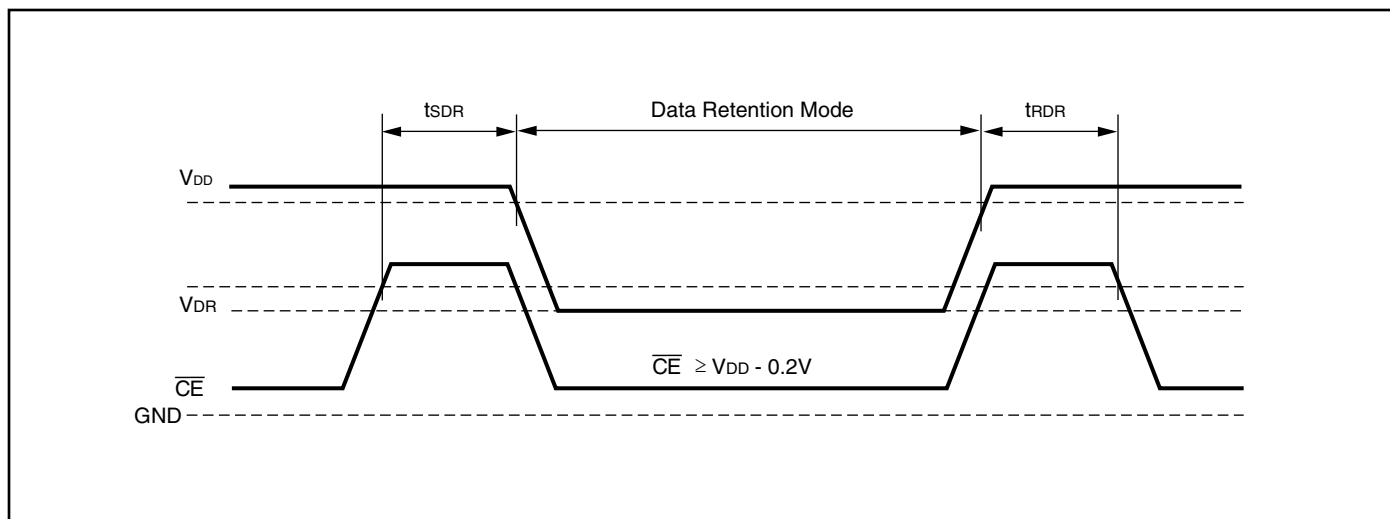
HIGH SPEED (IS61/64WV12816EDBLL)

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|-----------|-----------------------------|---|-----------------------|----------|---------------------|--------------|------|
| V_{DR} | V_{DD} for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| I_{DR} | Data Retention Current | $V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$ | Com. Ind. Auto. | — | 0.5 | 5 6 15 | mA |
| t_{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t_{RDR} | Recovery Time | See Data Retention Waveform | | t_{RC} | — | — | ns |

Note 1: Typical values are measured at $V_{DD} = V_{DR}(\text{min})$, $T_A = 25^\circ\text{C}$ and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



IS61/64WV12816EDBLL

ORDERING INFORMATION (HIGH SPEED)

Industrial Range: -40°C to +85°C

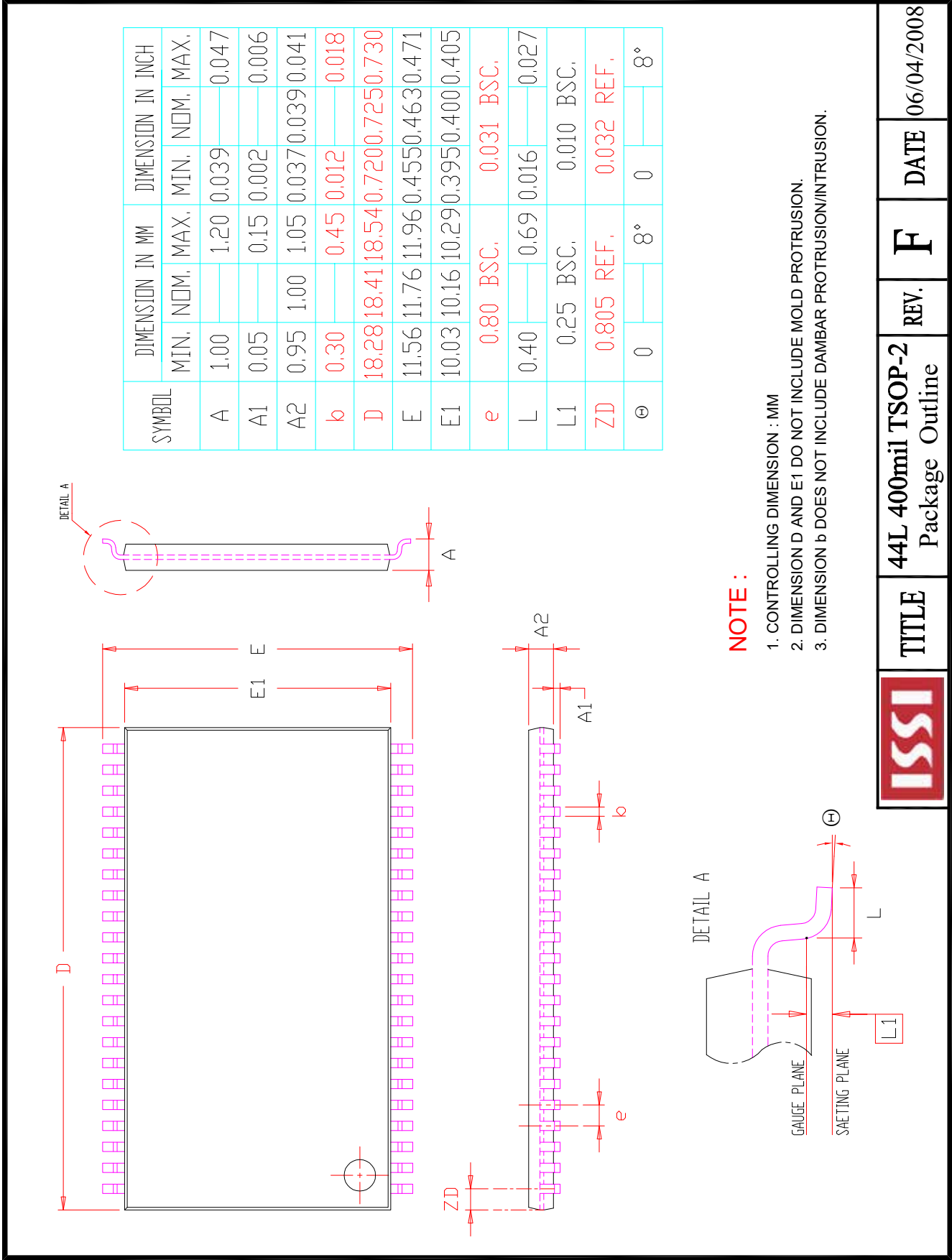
| Speed (ns) | Order Part No. | Package |
|------------|------------------------|------------------------------------|
| 8 | IS61WV12816EDBLL-8BLI | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS61WV12816EDBLL-8TLI | TSOP (Type II), Lead-free |
| 10 | IS61WV12816EDBLL-10BLI | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS61WV12816EDBLL-10TLI | TSOP (Type II), Lead-free |

Industrial Range: -40°C to +85°C

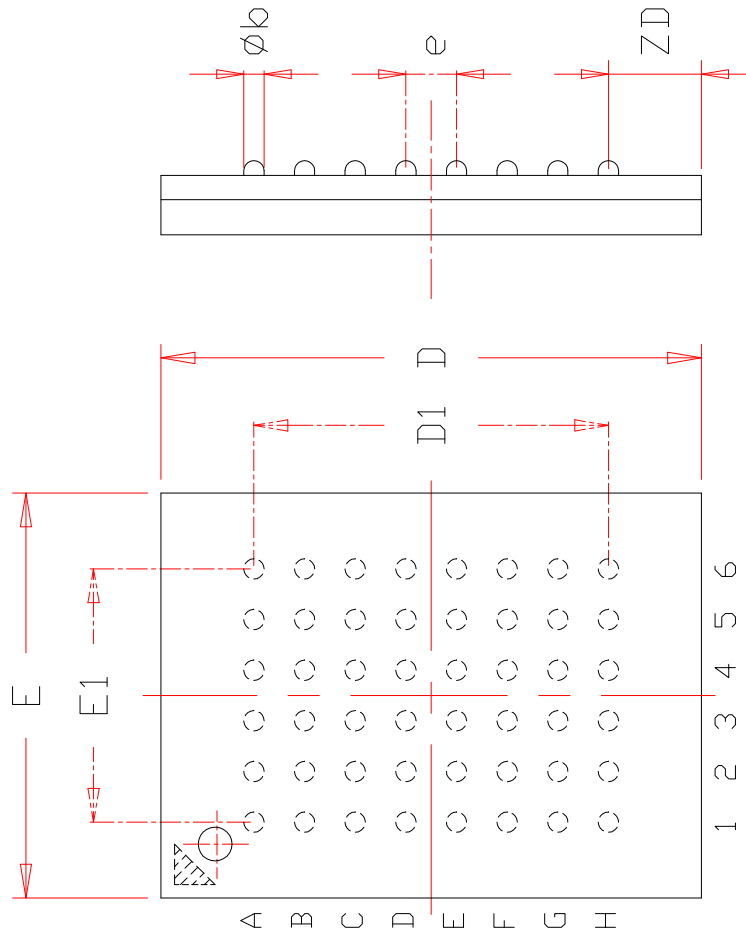
| Speed (ns) | Order Part No. | Package |
|------------|--------------------------|---|
| 10 | IS64WV12816EDBLL-10BLA1 | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS64WV12816EDBLL-10CTLA1 | TSOP (Type II), Lead-free, Copper Leadframe |

Automotive Range: -40°C to +125°C

| Speed (ns) | Order Part No. | Package |
|------------|--------------------------|---|
| 10 | IS64WV12816EDBLL-10BLA3 | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS64WV12816EDBLL-10CTLA3 | TSOP (Type II), Lead-free, Copper Leadframe |



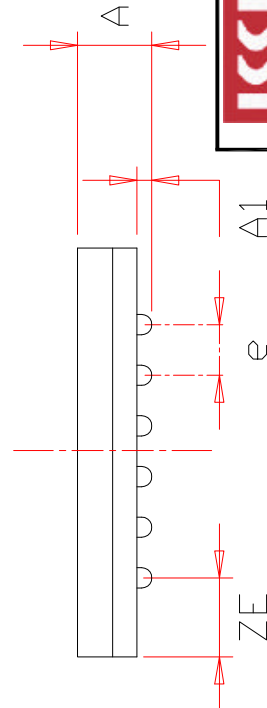
TOP VIEW



NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|----------|-----------------|-------|------|-------------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.20 | | 0.30 | 0.008 | | 0.012 |
| ϕb | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | 5.25 | BSC | | 0.207 | BSC | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | 3.75 | BSC | | 0.148 | BSC | |
| e | | 0.75 | BSC, | | 0.030 | BSC, |
| ZD | | 1.375 | REF. | | 0.054 | REF. |
| ZE | | 1.125 | REF. | | 0.044 | REF. |



| | | | | | | |
|--|-------|-------------------------------------|------|---|------|------------|
| | TITLE | 48L 6x8mm TF-BGA Package Outline | REV. | C | DATE | 08/12/2008 |
|--|-------|-------------------------------------|------|---|------|------------|

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- ⊖ [ISSI, Integrated Silicon Solution Inc Information](#)

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- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management