# THE DATASHEET OF

# 8N4SV76LC-0162CDI8

www.win-source.net 0086-755-83957316

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## General Description

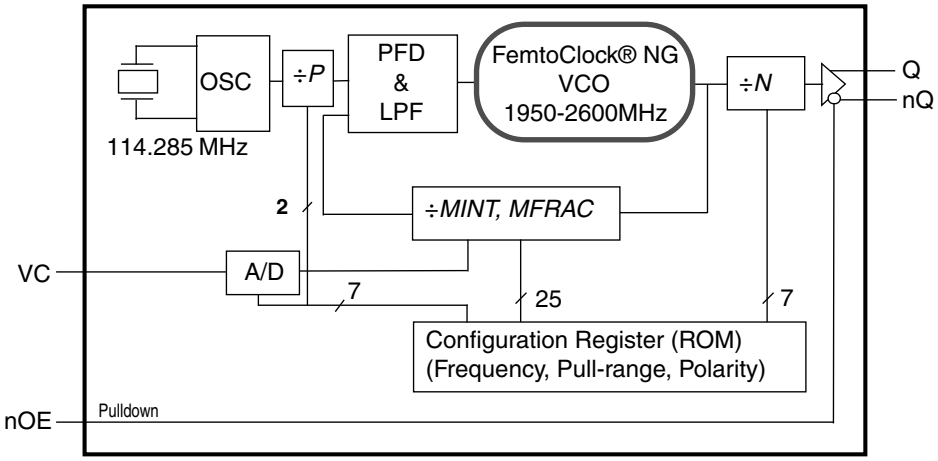
The IDT8N4SV76 is an LVDS Frequency-Programmable VCXO with very flexible frequency and pull-range programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device can be factory-programmed to any frequency in the range of 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz to the very high degree of frequency precision of 218Hz or better. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

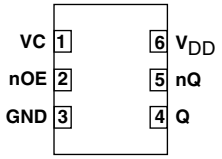
## Features

- Fourth generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Frequency programming resolution is 218Hz and better
- Factory-programmable VCXO pull range and control voltage polarity
- Absolute pull-range (APR) programmable from ±4.5 to ±754.5ppm
- One 2.5V or 3.3V LVDS clock output
- Output enable control input, LVCMOS/LVTTL compatible
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.53ps (typical)
- 2.5V or 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package

## Block Diagram




## Pin Assignment




**IDT8N4SV76**
**6-lead ceramic 5mm x 7mm x 1.55mm package body**
**CD Package**
**Top View**

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# Pin Description and Characteristic Tables

### Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | VC | Input | | VCXO Control Voltage input. |
| 2 | nOE | Input | Pulldown | Output enable pin. See Table 3A for function. LVCMOS/LVTTL interface levels. |
| 3 | GND | Power | | Power supply ground. |
| 4, 5 | Q, nQ | Output | | Differential clock output pair. LVDS interface levels. |
| 6 | $V_{DD}$ | Power | | Power supply pin. |

NOTE: *Pulldown* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

### Table 2. Pin Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | nOE | | | 5.5 | | pF |
| | | VC | | | 10 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 50 | | kΩ |

# Function Tables

### Table 3A. nOE Configuration

| Input | |
|---|---|
| **nOE** | **Output Enable** |
| 0 (default) | Outputs are enabled. |
| 1 | Outputs Q, nQ are in high-impedance state. |

.

### Table 3B. Output Frequency Range

| |
|---|
| 15.476MHz to 866.67MHz |
| 975MHz to 1,300MHz |

NOTE: Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz or better.

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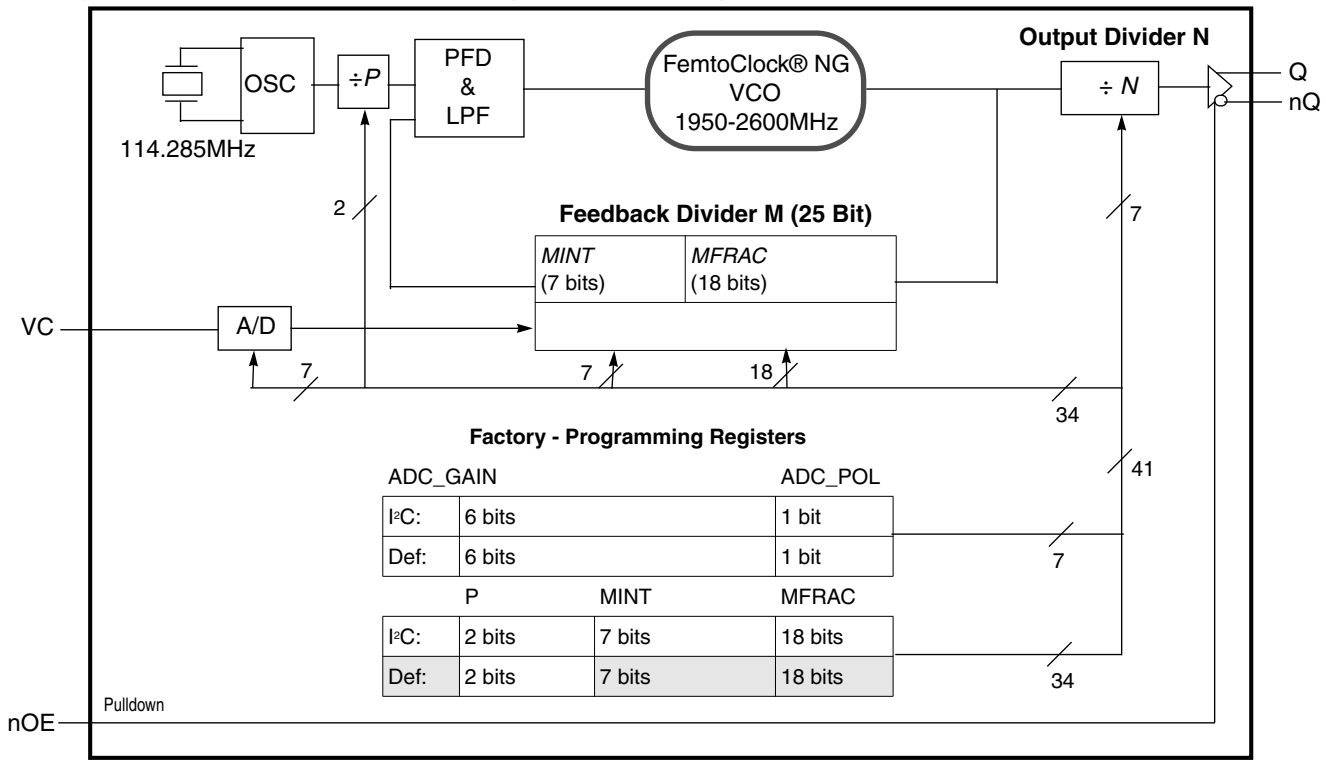
## Block Diagram with Factory-Configuration Registers

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# Principles of Operation

The block diagram consists of the internal 3rd overtone crystal and oscillator which provide the reference clock $f_{XTAL}$ of 114.285MHz. The PLL includes the FemtoClock® VCO along with the Pre-divider (*P*), the feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the $f_{XTAL}$ reference. The feedback divider is fractional supporting a huge number of output frequencies. Internal registers are used to hold up the factory pre-set configuration setting. The *P*, *M*, and *N* frequency configurations support an output frequency range 15.476MHz to 866.67MHz and 975MHz to 1,300MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator. The output frequency is determined by the 2-bit pre-divider (*P*), the feedback divider (M) and the 7-bit post divider (*N*). The feedback divider (*M*) consists of both a 7-bit integer portion (*MINT*) and an 18-bit fractional portion (*MFRAC*) and provides the means for high-resolution frequency generation. The output frequency $f_{OUT}$ is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[ MINT + \frac{MFRAC + 0.5}{2^{18}} \right]$$

## Frequency Configuration

An order code is assigned to each frequency configuration and the VCXO pull-range programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information Section in this document. For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information on programming capabilities of the device for custom frequency and pull-range configurations, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide.*

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## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 3.63V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$ (LVDS)<br>Continuous Current<br>Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 49.4°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | 140 | 175 | mA |

**Table 4B. Power Supply DC Characteristics,** $V_{DD}$ = 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{DD}$ | Power Supply Current | | | 135 | 170 | mA |

**Table 4C. LVCMOS/LVTTL DC Characteristic,** $V_{DD}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{DD}$ = 3.3V | 2 | | $V_{DD}$ + 0.3 | V |
| | | | $V_{DD}$ = 2.5V | 1.7 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ = 3.3V | -0.3 | | 0.8 | V |
| | | | $V_{DD}$ = 2.5V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | nOE | $V_{DD}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | nOE | $V_{DD}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |

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**Table 4D. LVDS DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 247 | 330 | 454 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.14 | 1.23 | 1.31 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

**Table 4E. LVDS DC Characteristics,** $V_{DD}$ = 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 247 | 320 | 454 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.13 | 1.22 | 1.30 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

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## AC Electrical Characteristics

**Table 5A. AC Characteristics,** $V_{DD}$ = 3.3V ± 5% or 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency Q, nQ | | 15.476 | | 866.67 | MHz |
| | | | 975 | | 1,300 | MHz |
| $f_I$ | Initial Accuracy | Measured @ 25°C, $V_C = V_{DD}/2$ | | | ±10 | ppm |
| $f_S$ | Temperature Stability | Option code = A or B | | | ±100 | ppm |
| | | Option code = E or F | | | ±50 | ppm |
| | | Option code = K or L | | | ±20 | ppm |
| $f_A$ | Aging | Frequency drift over 10 year life | | | ±3 | ppm |
| | | Frequency drift over 15 year life | | | ±5 | ppm |
| $f_T$ | Total Stability | Option code A, B (10 year life) | | | ±113 | ppm |
| | | Option code E, F (10 year life) | | | ±63 | ppm |
| | | Option code K, L (10 year life) | | | ±33 | ppm |
| tjit(cc) | Cycle-to-Cycle Jitter; NOTE 1 | | | 6 | 14 | ps |
| tjit(per) | Period Jitter; NOTE 1 | | | 4 | 6 | ps |
| tjit(Ø) | RMS Phase Jitter (Random); NOTE 2,3 | 156.25MHz, Integration Range: 12kHz - 20MHz | | 0.53 | 0.73 | ps |
| tjit(Ø) | RMS Phase Jitter (Random); NOTE 2,3 $f_{XTAL}$ = 114.285mhz | 500MHz < $f_{OUT}$ ≤ 1300MHz | | 0.46 | 0.67 | ps |
| | | 100MHz < $f_{OUT}$ ≤ 500MHz | | 0.48 | 0.63 | ps |
| | | 15MHz ≤ $f_{OUT}$ ≤ 100MHz | | 0.76 | 1.4 | ps |
| $\Phi_N(100)$ | Single-side Band Phase Noise, 100Hz from Carrier | 156.25MHz | | -67 | | dBc/Hz |
| $\Phi_N(1k)$ | Single-side Band Phase Noise, 1kHz from Carrier | 156.25MHz | | -89 | | dBc/Hz |
| $\Phi_N(10k)$ | Single-side Band Phase Noise, 10kHz from Carrier | 156.25MHz | | -113 | | dBc/Hz |
| $\Phi_N(100k)$ | Single-side Band Phase Noise, 100kHz from Carrier | 156.25MHz | | -118 | | dBc/Hz |
| $\Phi_N(1M)$ | Single-side Band Phase Noise, 1MHz from Carrier | 156.25MHz | | -127 | | dBc/Hz |
| $\Phi_N(10M)$ | Single-side Band Phase Noise, 10MHz from Carrier | 156.25MHz | | -137 | | dBc/Hz |
| PSNR | Power Supply Noise Rejection | 50mV Sinusoidal Noise 1kHz - 50MHz | | -58.7 | | dBc |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 80 | | 500 | ps |
| odc | Output Duty Cycle | | 45 | | 55 | % |
| $t_{STARTUP}$ | Device Startup Time after Power-up | | | | 15 | ms |

*Notes are continued on next page.*

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NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
Notes continued on next page.
NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.
NOTE: Characterized with $V_C = V_{DD}/2$.
NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Please refer to the phase noise plots.
NOTE 3: Please see the FemtoClock NG Ceramic 5x7 Modules Programming guide for more information on PLL feedback modes and the optimum configuration for phase noise.

**Table 5B. VCXO Control Voltage Input ($V_C$) Characteristics,** $V_{DD}$ = 3.3V ± 5% or 2.5V ± 5, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $K_V$ | Oscillator Gain, NOTE 1, 2, 3 | $V_{DD}$ = 3.3V | 7.57 | | 477.27 | ppm/V |
| | Oscillator Gain, NOTE 1, 2, 3 | $V_{DD}$ = 2.5V | 10 | | 630 | ppm/V |
| $L_{VC}$ | Control Voltage Linearity; NOTE 4 | BSL Variation | -1 | ±0.1 | +1 | % |
| BW | Modulation Bandwidth | | | 100 | | kHz |
| $Z_{VC}$ | VC Input Impedance | | | 500 | | kΩ |
| $VC_{NOM}$ | Nominal Control Voltage | | | $V_{DD}/2$ | | V |
| $V_C$ | Control Voltage Tuning Range; NOTE 4 | | 0 | | $V_{DD}$ | V |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: $V_C$ = 10% to 90% of $V_{DD}$.
NOTE 2: Nominal oscillator gain: Pull range divided by the control voltage tuning range of 3.3V. E.g. for ADC_GAIN [6:0] = 000001 the pull range is ± 12.5ppm, resulting in an oscillator gain of 25ppm ÷ 3.3V = 7.57ppm/V.
NOTE 3: For best phase noise performance, use the lowest $K_V$ that meets the requirements of the application.
NOTE 4: BSL = Best Straight Line Fit: Variation of the output frequency vs. control voltage $V_C$, in percent. $V_C$ ranges from 10% to 90% $V_{DD}$.

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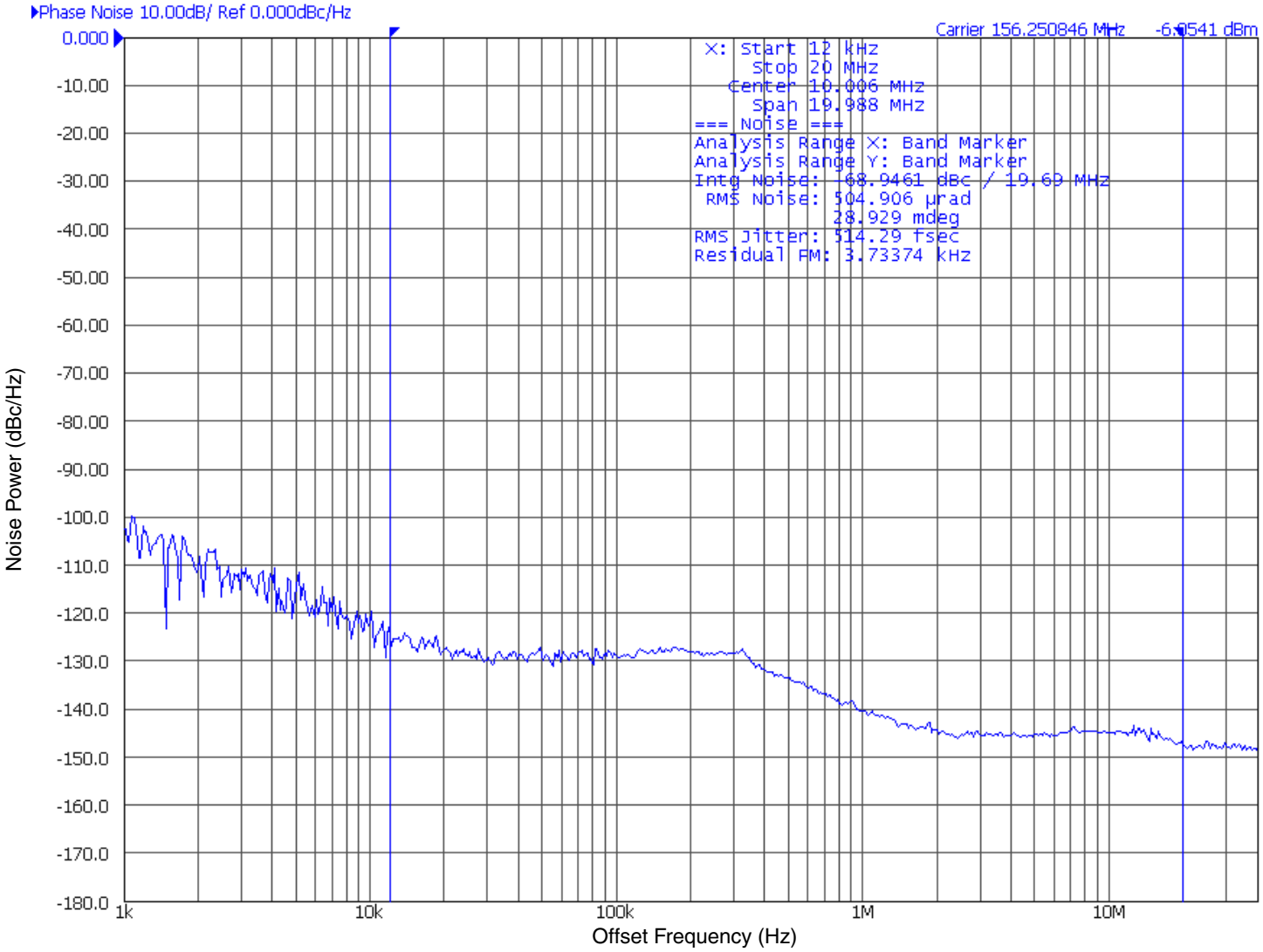
## Typical Phase Noise at 156.25MHz (12kHz - 20MHz)

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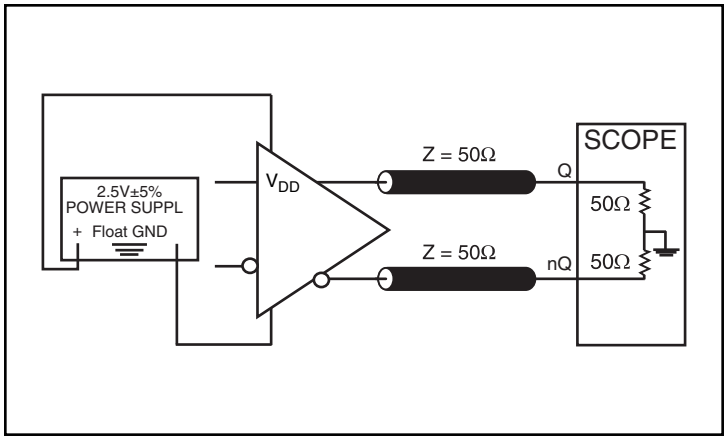
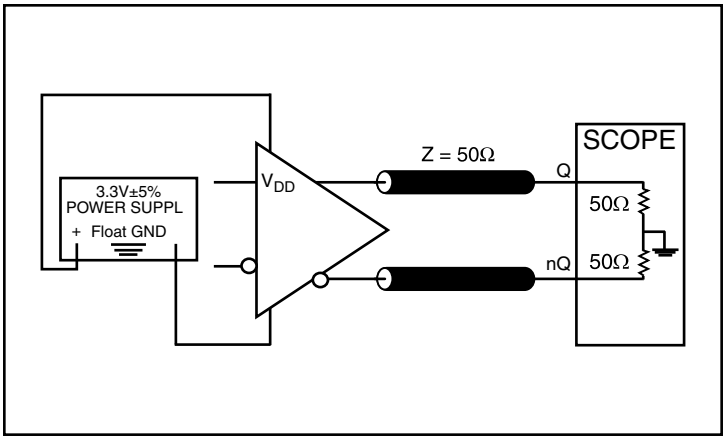
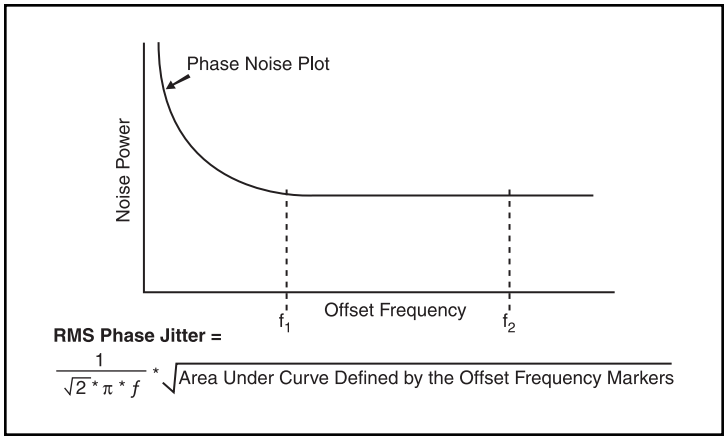
## Parameter Measurement Information



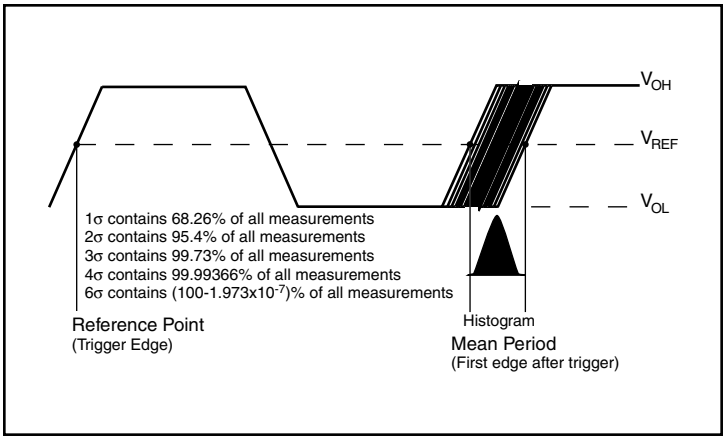

**2.5V LVDS Output Load AC Test Circuit**



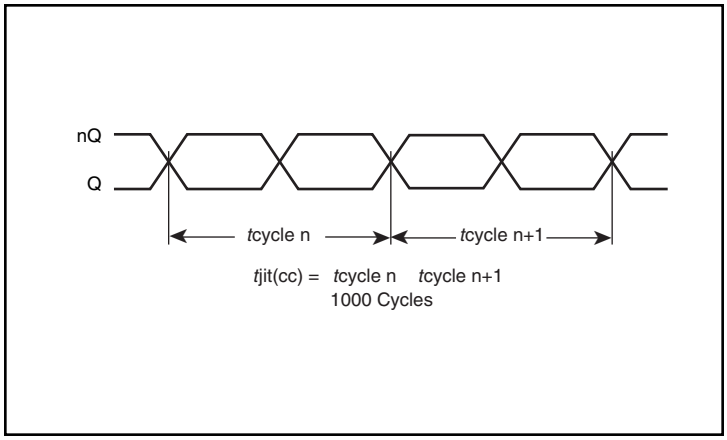

**3.3V LVDS Output Load AC Test Circuit**



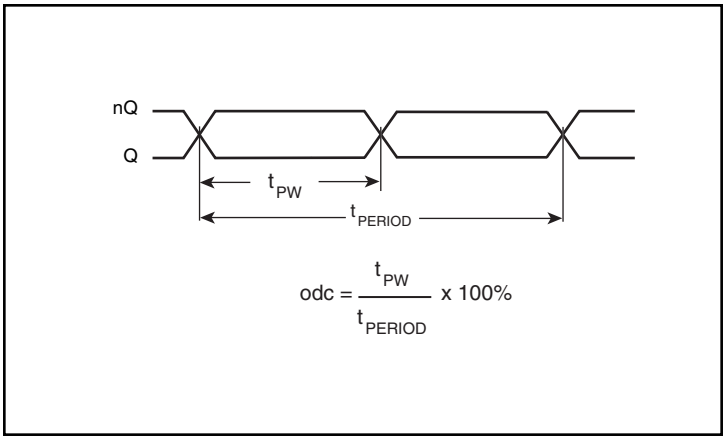

**RMS Phase Jitter**




**Period Jitter**




**Cycle-to-Cycle Jitter**




**Output Duty Cycle/Pulse Width/Period**

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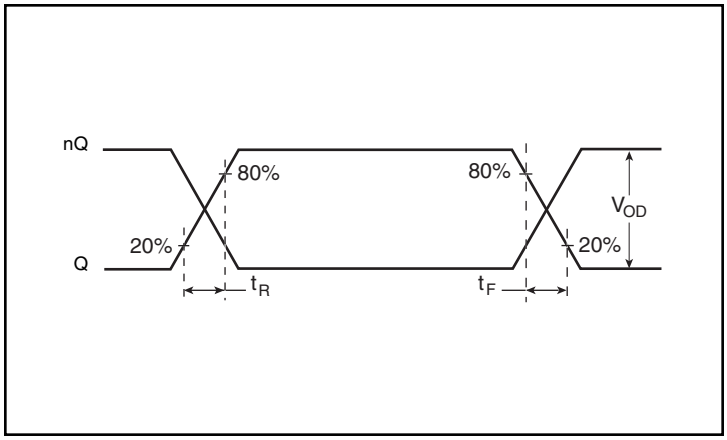
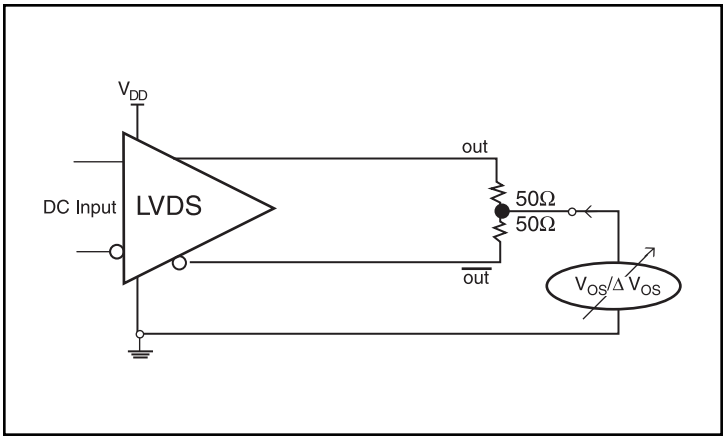
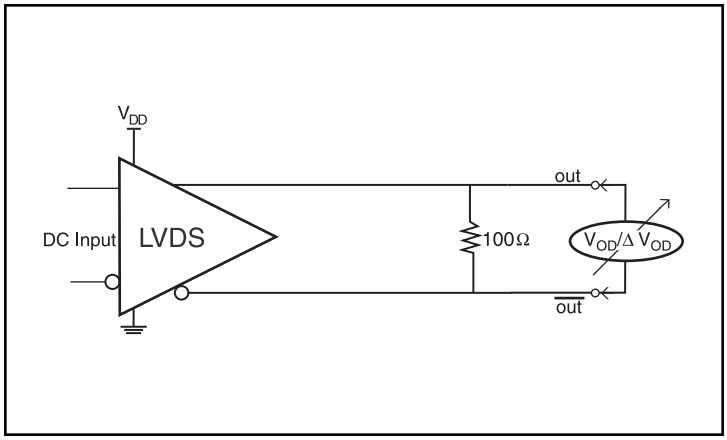
## Parameter Measurement Information, continued




**Output Rise/Fall Time**




**Offset Voltage Setup**




**Differential Output Voltage Setup**

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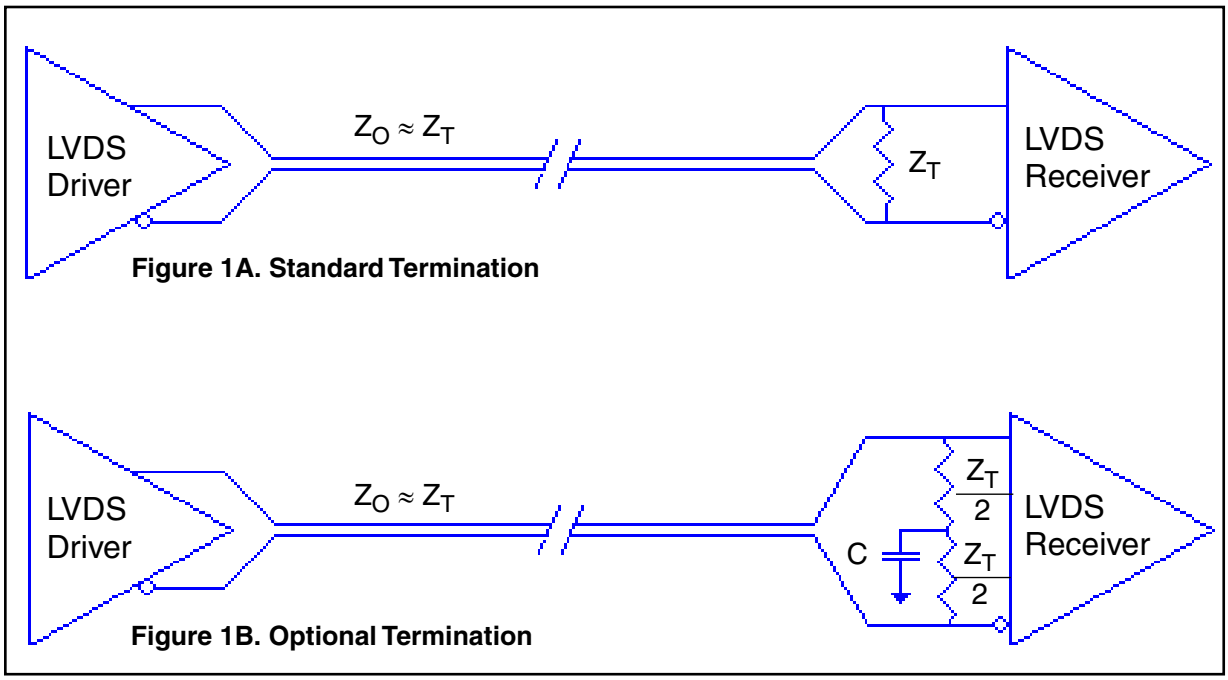
# Applications Information

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 1A* can be used with either type of output structure. *Figure 1B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.




**LVDS Termination**

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## Schematic Layout

Figure 2 shows an example of IDT8N4SV76 application schematic. In this example, the device is operated at $V_{DD}$ = 3.3V. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added.

Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

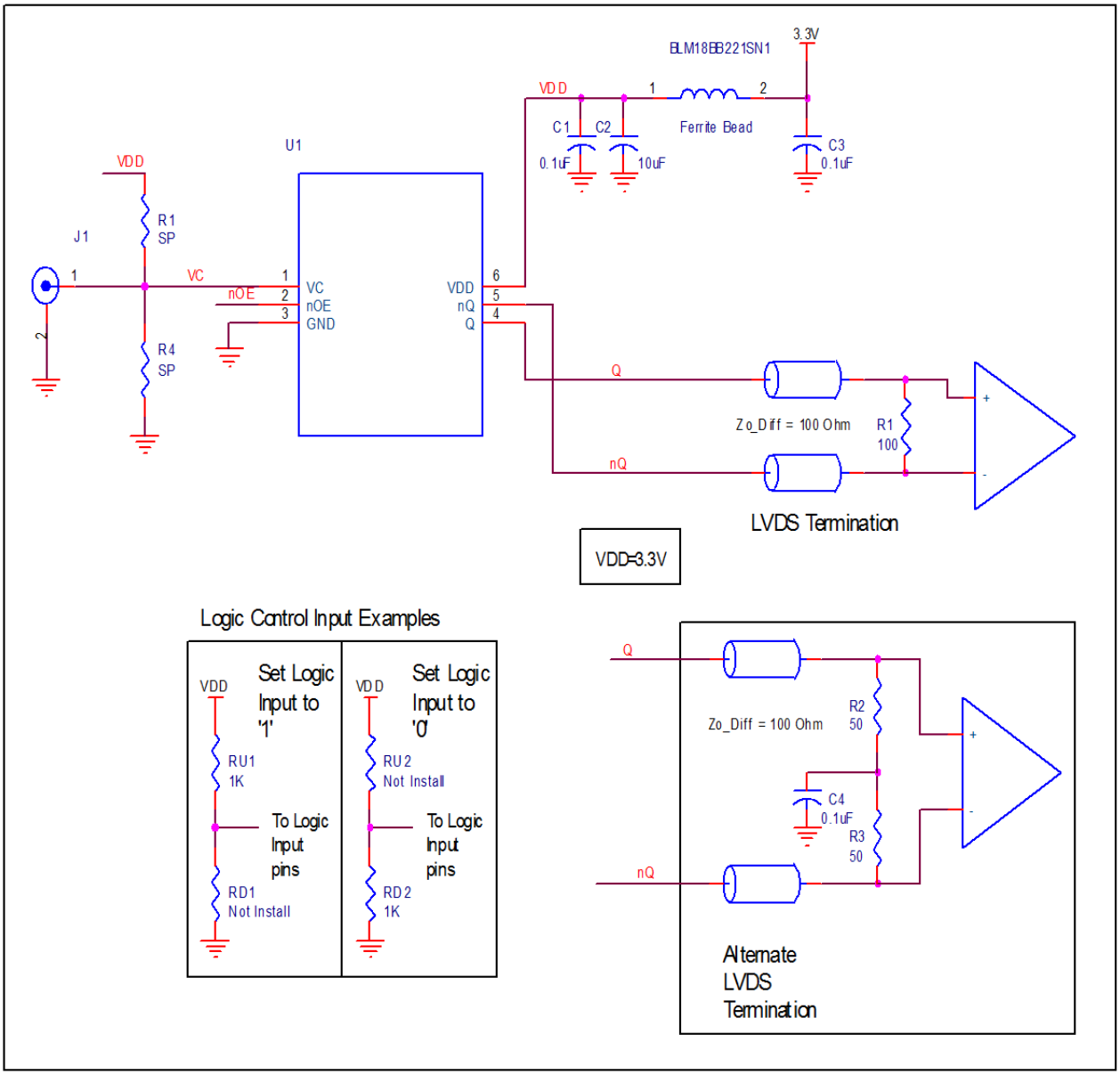


**Figure 2. IDT8N4SV76 Application Schematic**

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# Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N4SV76.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8N4SV76 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 175mA = **606mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

**Total Power**$_{_MAX}$ (3.3V, with all outputs switching) = 606mW + 30mW = **636.38mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.636W * 49.4°C/W = 116.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 6 Lead Ceramic VFQFN, Forced Convection**

| $\theta_{JA}$ **by Velocity** | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49.4°C/W | 44.2°C/W | 42.1°C/W |

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## Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49.4°C/W | 44.2°C/W | 42.1°C/W |

## Transistor Count

The transistor count for IDT8N4SV76 is: 47,414

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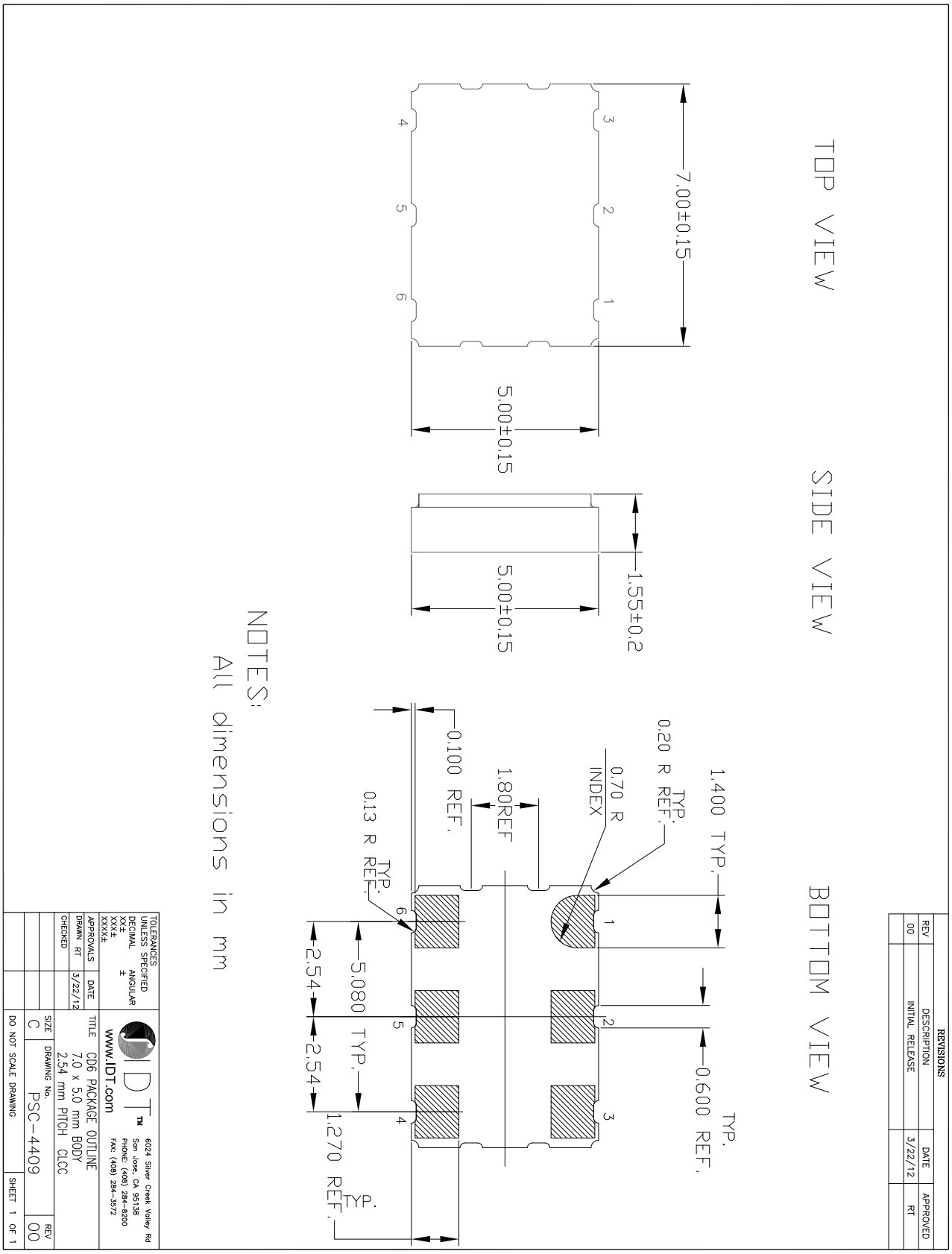
## Package Outline and Package Dimensions

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## Ordering Information for FemtoClock NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of devices options such as the output type, number of default frequencies, internal crystal frequency, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. Table 8 specifies the available order codes, including the device options, the default frequency codes can be obtained from the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document. Example part number: the order code 8N4SV76FC-0001CDI specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a LVPECL output, a ±50 ppm crystal frequency accuracy, contains a 114.285MHz internal crystal as frequency source, industrial temperature range, a lead-free (6/6 RoHS) 6-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100MHz, 122.88MHz, 125MHz and 156.25MHz and to the VCXO pull range of min. ±100 ppm.

Other default frequencies and order codes are available from IDT on request.

## Table 8. Order Codes

**Part/Order Number**

**8N X X XXX X X - dddd XX X X**

**FemtoClock NG**

**I/O Identifier**
**0**: LVCMOS
**3**: LVPECL
**4**: LVDS

**Number of Default Frequencies**
**S**: 1: Single
**D**: 2: Dual
**Q**: 4: Quad

**Part Number**

| | Function | #pins | OE fct. at pin |
|---|---|---|---|
| **001** | XO | 10 | OE@2 |
| **003** | XO | 10 | OE@1 |
| **V01** | VCXO | 10 | OE@2 |
| **V03** | VCXO | 10 | OE@1 |
| **V75** | VCXO | 6 | OE@2 |
| **V76** | VCXO | 6 | nOE@2 |
| **V85** | VCXO | 6 | — |
| **085** | XO | 6 | OE@1 |
| **270** | XO | 6 | OE@1 |
| **271** | XO | 6 | OE@2 |
| **272** | XO | 6 | nOE@2 |
| **273** | XO | 6 | nOE@1 |

**Shipping Package**
**8**: Tape & Reel
(no letter): Tray

**Ambient Temperature Range**
"**I**": Industrial: ($T_A$ = -40°C to 85°C)
(no letter) : ($T_A$ = 0°C to 70°C)

**Package Code**
**CD**: Lead-Free, 6/10-lead ceramic 5mm x 7mm x 1.55mm

**Default-Frequency and VCXO Pull Range**
*See* document *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information.*

| dddd | $f_{XTAL}$ (MHz) | PLL feedback | Use for |
|---|---|---|---|
| **0000** to **0999** | 114.285 | Fractional | VCXO, XO |
| **1000** to **1999** | 100.000 | Integer | XO |
| **2000** to **2999** | | Fractional | XO |

Last digit = **L**: configuration pre-programmed and not changeable

**Die Revision**
**C** (opt. 208)

**Option Code (Supply Voltage and Frequency-Stability)**
**A**: $V_{CC}$ = 3.3V±5%, ±100ppm
**B**: $V_{CC}$ = 2.5V±5%, ±100ppm
**E**: $V_{CC}$ = 3.3V±5%, ±50ppm
**F**: $V_{CC}$ = 2.5V±5%, ±50ppm
**K**: $V_{CC}$ = 3.3V±5%, ±20ppm
**L**: $V_{CC}$ = 2.5V±5%, ±20ppm

NOTE: For order information, also see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

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## Table 9. Device Marking

| | Industrial Temperature Range ($T_A$ = -40°C to 85°C) | Commercial Temperature Range ($T_A$ = 0°C to 70°C) |
|---|---|---|
| **Marking** | IDT8N4SV76**y**C-<br>**dddd**CDI | IDT8N4SV76**y**C-<br>**dddd**CD |
| | **y** = Option Code, **dddd**=Default-Frequency and VCXO Pull Range | |

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## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | | 5 | Absolute Maximum Ratings - Thermal Impedance changed from 41.4 to 41.9. | 4/25/12 |
| | | 14 | Power Considerations - corrected Thermal Resistance table and updated calculations. | |
| | T7 | 15 | Reliability Information - corrected thermal table. | |
| B | T4D | 6 | 3.3V LVDS DC Characteristics Table - updated specs. | 8/22/12 |
| | T4E | 6 | 2.5V LVDS DC Characteristics Table - updated specs. | |
| | | | Per PCN #N1206-02. | |
| B | 5A | 7 | RMS Phase Jitter, Test Conditions, corrected typos for 500MHz and 100MHz; “≤” to “<” | 11/20/2013 |

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