THE DATASHEET OF

PCF2129T/2,518

www.win-source.net 0086-755-83957316

PCF2129

Accurate RTC with integrated quartz crystal for industrial applications

Rev. 8.0 — 18 July 2022 Product data sheet

1 General description

The PCF2129 is a CMOS[1] Real Time Clock (RTC) and calendar with an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for very high accuracy and very low power consumption. The PCF2129 has a selectable I^2C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, a timestamp function, and many other features.

For a selection of NXP Real-Time Clocks, see Table 82

2 Features and benefits

- UL Recognized Component (PCF2129AT and PCF2129T)
- Operating temperature range from -40 °C to +85 °C
- Temperature Compensated Crystal Oscillator (TCXO) with integrated capacitors
- Typical accuracy:
  - PCF2129AT: ±3 ppm from -15 °C to +60 °C
  - PCF2129T: ±3 ppm from -30 °C to +80 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, seconds, and leap year correction
- Timestamp function
  - with interrupt capability
  - detection of two different events on one multilevel input pin (for example, for tamper detection)
- Two line bidirectional 400 kHz Fast-mode I^2C-bus interface
- Three line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage
- Battery low detection function
- Power-On Reset Override (PORO)
- Oscillator stop detection function
- Interrupt output (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable watchdog timer with interrupt
- Programmable alarm function with interrupt capability
- Programmable square output
- Clock operating voltage: 1.8 V to 4.2 V

1 The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Low supply current: typical 0.70 µA at V_{DD} = 3.3 V

3 Applications

- Electronic metering for electricity, water, and gas
- Precision timekeeping
- Access to accurate time of the day
- GPS equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCF2129AT	PCF2129AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCF2129T	PCF2129T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
PCF2129AT	PCF2129AT/2,518	SO20	reel 13" Q1 DP	2000	T_{amb} = -40 °C to +85 °C
PCF2129T	PCF2129T/2,518	SO16	reel 13" Q1 DP	1000	T_{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

5 Block diagram

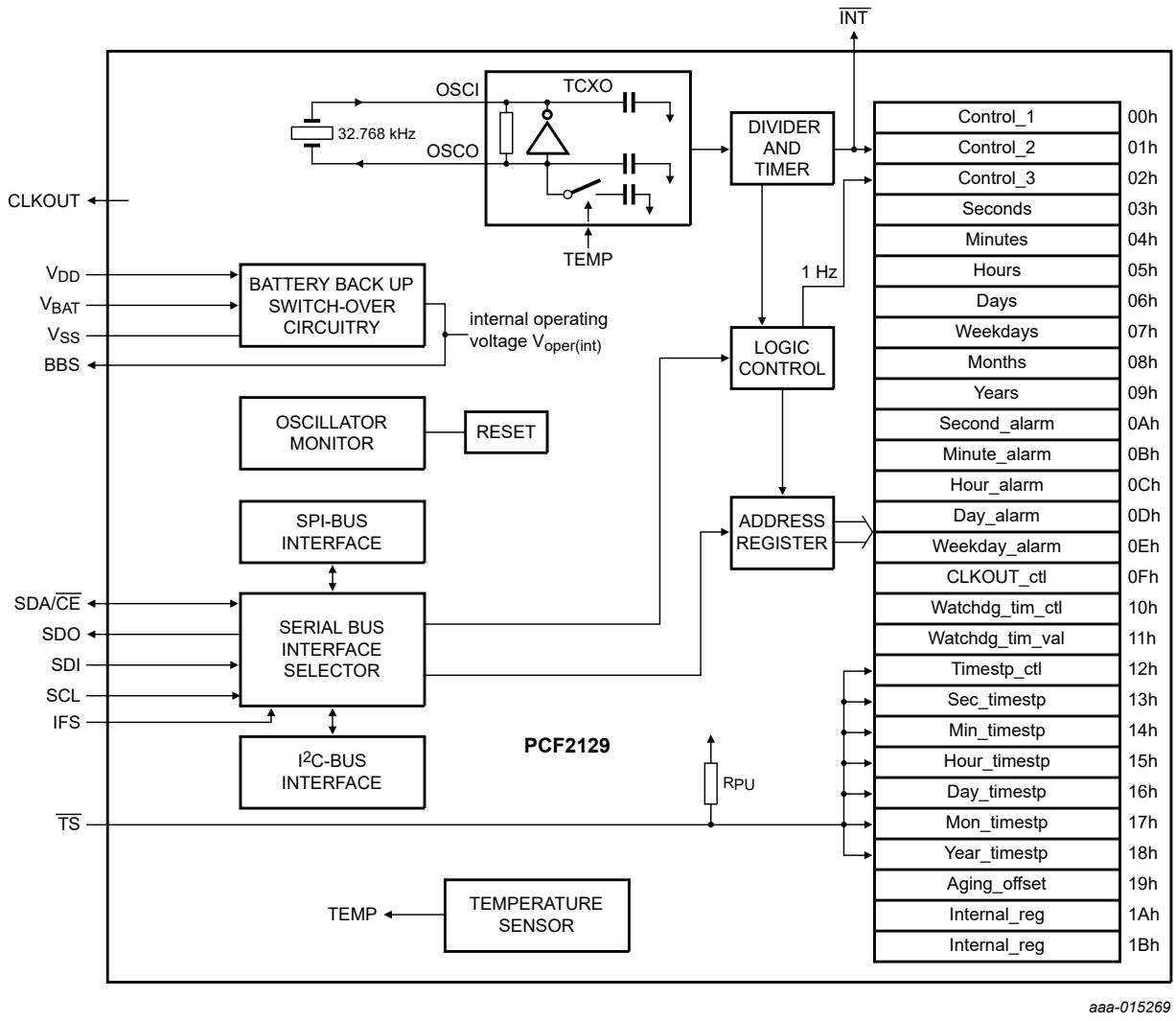


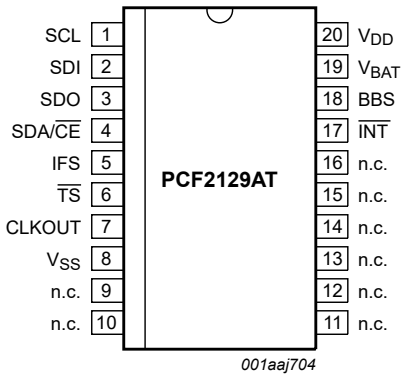
Figure 1. Block diagram of PCF2129

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

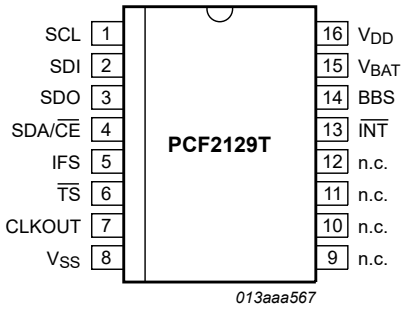
6 Pinning information

6.1 Pinning



Top view. For mechanical details, see Figure 50.

Figure 2. Pin configuration for PCF2129AT (SO20)



Top view. For mechanical details, see Figure 50.

Figure 3. Pin configuration for PCF2129T (SO16)

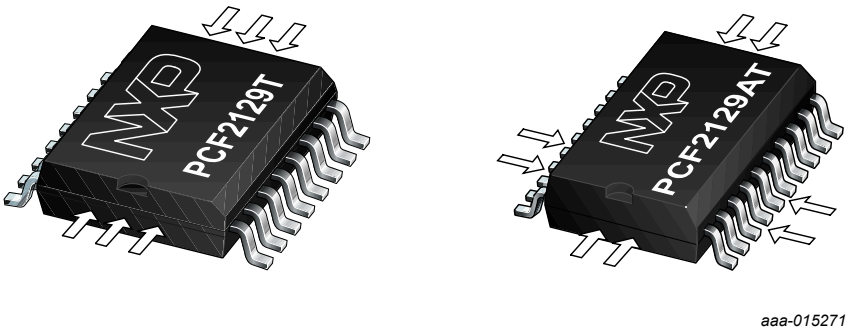


Figure 4. Position of the stubs from the package assembly process

After lead forming and cutting, there remain stubs from the package assembly process. These stubs are present at the edge of the package as illustrated in Figure 4. The stubs are at an electrical potential. To avoid malfunction of the PCF2129, it has to be ensured that they are not shorted with another electrical potential (e.g. by condensation).

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

6.2 Pin description

Table 3. Pin description of PCF2129

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin		Description
	PCF2129AT	PCF2129T	
SCL	1	1	combined serial clock input for both I^2C-bus and SPI-bus
SDI	2	2	serial data input for SPI-bus connect to pin V_{SS} if I^2C-bus is selected
SDO	3	3	serial data output for SPI-bus, push-pull
SDA/$\overline{CE}$	4	4	combined serial data input and output for the I^2C-bus and chip enable input (active LOW) for the SPI-bus
IFS	5	5	interface selector input connect to pin V_{SS} to select the SPI-bus connect to pin BBS to select the I^2C-bus
$\overline{TS}$	6	6	timestamp input (active LOW) with 200 kΩ internal pull-up resistor (R_{PU})
CLKOUT	7	7	clock output (open-drain)
V_{SS}	8	8	ground supply voltage
n.c.	9 to 16	9 to 12	not connected; do not connect; do not use as feed through
$\overline{INT}$	17	13	interrupt output (open-drain; active LOW)
BBS	18	14	output voltage (battery backed)
V_{BAT}	19	15	battery supply voltage (backup) connect to V_{SS} if battery switch over is not used
V_{DD}	20	16	supply voltage

7 Functional description

The PCF2129 is a Real Time Clock (RTC) and calendar with an on-chip Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package (see Section 7.3.3).

Address and data are transferred by a selectable 400 kHz Fast-mode I^2C-bus or a 3 line SPI-bus with separate data input and output (see Section 8). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCF2129 has a backup battery input pin and backup battery switch-over circuit which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see Section 7.5.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see Section 7.5.2). When the battery voltage drops below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.1 Register overview

The PCF2129 contains an auto-incrementing address register: the built-in address register will increment automatically after each read or write of a data byte up to the register 1Bh. After register 1Bh, the auto-incrementing will wrap around to address 00h (see Figure 5).

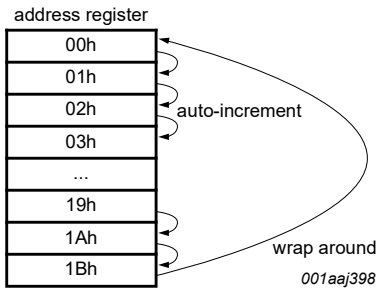


Figure 5. Handling address registers

- The first three registers (memory address 00h, 01h, and 02h) are used as control registers (see Section 7.2).
- The memory addresses 03h through to 09h are used as counters for the clock function (seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 7.8).
- The registers at addresses 0Ah through 0Eh define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 7.9).
- The register at address 0Fh defines the temperature measurement period and the clock out mode. The temperature measurement can be selected from every 4 minutes (default) down to every 30 seconds (see Table 13). CLKOUT frequencies of 32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see Table 14).
- The registers at addresses 10h and 11h are used for the watchdog timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 1 ms to greater than 4 hours (see Table 51). An interrupt is generated when the watchdog times out.
- The registers at addresses 12h to 18h are used for the timestamp function. When the trigger event happens, the actual time is saved in the timestamp registers (see Section 7.11).
- The register at address 19h is used for the correction of the crystal aging effect (see Section 7.4.1).
- The registers at addresses 1Ah and 1Bh are for internal use only.
- The registers Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen. This prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 7.8.8).

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 4. Register overview

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
Control registers											
00h	Control_1	EXT_TEST	T	STOP	TSF1	POR_OVRD	12_24	MI	SI	0000 1000	Table 6
01h	Control_2	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T	0000 0000	Table 8
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE	0000 0000	Table 10
Time and date registers											
03h	Seconds	OSF	SECONDS (0 to 59)							1XXX XXXX	Table 21
04h	Minutes	-	MINUTES (0 to 59)							- XXX XXXX	Table 24
05h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode					- - XX XXXX	Table 26
				HOURS (0 to 23) in 24-hour mode						- - XX XXXX	
06h	Days	-	-	DAYS (1 to 31)						- - XX XXXX	Table 28
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			- - - - - XXX	Table 30
08h	Months	-	-	-	MONTHS (1 to 12)					- - - X XXXX	Table 33
09h	Years	YEARS (0 to 99)								XXXX XXXX	Table 36
Alarm registers											
0Ah	Second_alarm	AE_S	SECOND_ALARM (0 to 59)							1XXX XXXX	Table 38
0Bh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)							1XXX XXXX	Table 40
0Ch	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode					1 - XX XXXX	Table 42
				HOUR_ALARM (0 to 23) in 24-hour mode						1 - XX XXXX	
0Dh	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)						1 - XX XXXX	Table 44
0Eh	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)			1 - - - - XXX	Table 46
CLKOUT control register											
0Fh	CLKOUT_ctl	TCR[1:0]		OTPR	-	-	COF[2:0]			00X - - 000	Table 12

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 4. Register overview...*continued*

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value	Reference
		7	6	5	4	3	2	1	0		
Watchdog registers											
10h	Watchdg_tim_ctl	WD_CD	T	TI_TP	-	-	-	TF[1:0]		000 - - - 11	Table 48
11h	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]								XXXX XXXX	Table 50
Timestamp registers											
12h	Timestp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]					00 - X XXXX	Table 57
13h	Sec_timestp	-	SECOND_TIMESTP (0 to 59)							- XXX XXXX	Table 59
14h	Min_timestp	-	MINUTE_TIMESTP (0 to 59)							- XXX XXXX	Table 61
15h	Hour_timestp	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode					- - XX XXXX	Table 63
				HOUR_TIMESTP (0 to 23) in 24-hour mode						- - XX XXXX	
16h	Day_timestp	-	-	DAY_TIMESTP (1 to 31)						- - XX XXXX	Table 65
17h	Mon_timestp	-	-	-	MONTH_TIMESTP (1 to 12)					- - - X XXXX	Table 67
18h	Year_timestp	YEAR_TIMESTP (0 to 99)								XXXX XXXX	Table 69
Aging offset register											
19h	Aging_offset	-	-	-	-	AO[3:0]				- - - - 1000	Table 16
Internal registers											
1Ah	Internal_reg	-	-	-	-	-	-	-	-	- - - - - - - -	-
1Bh	Internal_reg	-	-	-	-	-	-	-	-	- - - - - - - -	-

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.2 Control registers

The first 3 registers of the PCF2129, with the addresses 00h, 01h, and 02h, are used as control registers.

7.2.1 Register Control_1

Table 5. Control_1 - control and status register 1 (address 00h) bit allocation

Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	EXT_ TEST	T	STOP	TSF1	POR_ OVRD	12_24	MI	SI
Reset value	0	0	0	0	1	0	0	0

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	Section 7.13
		1	external clock test mode	
6	T	0	unused	-
5	STOP	0	RTC source clock runs	Section 7.14
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available	
4	TSF1	0	no timestamp interrupt generated	Section 7.11.1
		1	flag set when $\overline{TS}$ input is driven to an intermediate level between power supply and ground; flag must be cleared to clear interrupt	
3	POR_OVRD	0	Power-On Reset Override (PORO) facility disabled; **set logic 0 for normal operation**	Section 7.7.2
		1	Power-On Reset Override (PORO) sequence reception enabled	
2	12_24	0	24-hour mode selected	Table 26, Table 42, Table 43, Table 63
		1	12-hour mode selected	
1	MI	0	minute interrupt disabled	Section 7.12.1
		1	minute interrupt enabled	
0	SI	0	second interrupt disabled	
		1	second interrupt enabled	

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.2.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit allocation

Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T
Reset value	0	0	0	0	0	0	0	0

Table 8. Control_2 - control and status register 2 (address 01h) bit description

Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description	Reference
7	MSF	0	no minute or second interrupt generated	Section 7.12
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	WDTF	0	no watchdog timer interrupt or reset generated	Section 7.12.3
		1	flag set when watchdog timer interrupt or reset generated; flag cannot be cleared by command (read-only)	
5	TSF2	0	no timestamp interrupt generated	Section 7.11.1
		1	flag set when $\overline{TS}$ input is driven to ground; flag must be cleared to clear interrupt	
4	AF	0	no alarm interrupt generated	Section 7.9.6
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
3	T	0	unused	-
2	TSIE	0	no interrupt generated from timestamp flag	Section 7.12.5
		1	interrupt generated when timestamp flag set	
1	AIE	0	no interrupt generated from the alarm flag	Section 7.12.4
		1	interrupt generated when alarm flag set	
0	T	0	unused	-

7.2.3 Register Control_3

Table 9. Control_3 - control and status register 3 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
Reset value	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 10. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	see Table 18	control of the battery switch-over, battery low detection, and extra power fail detection functions	Section 7.5
4	BTSE	0	no timestamp when battery switch-over occurs	Section 7.11.4
		1	time-stamped when battery switch-over occurs	
3	BF	0	no battery switch-over interrupt generated	Section 7.5.1 and Section 7.11.4
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	BLF	0	battery status ok; no battery low interrupt generated	Section 7.5.2
		1	battery status low; flag cannot be cleared by command	
1	BIE	0	no interrupt generated from the battery flag (BF)	Section 7.12.6
		1	interrupt generated when BF is set	
0	BLIE	0	no interrupt generated from battery low flag (BLF)	Section 7.12.7
		1	interrupt generated when BLF is set	

7.3 Register CLKOUT_ctl

Table 11. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TCR[1:0]		OTPR	-	-	COF[2:0]		
Reset value	0	0	X	-	-	0	0	0

Table 12. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 6	TCR[1:0]	see Table 13	temperature measurement period
5	OTPR	0	no OTP refresh
		1	OTP refresh performed
4 to 3	-	-	unused
2 to 0	COF[2:0]	see Table 14	CLKOUT frequency selection

7.3.1 Temperature compensated crystal oscillator

The frequency of tuning fork quartz crystal oscillators is temperature-dependent. In the PCF2129, the frequency deviation caused by temperature variation is corrected by adjusting the load capacitance of the crystal oscillator.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

The load capacitance is changed by switching between two load capacitance values using a modulation signal with a programmable duty cycle. In order to compensate the spread of the quartz parameters every chip is factory calibrated.

The frequency accuracy can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of f_{CLKOUT} = 32.768 kHz (default value) leads to inaccurate measurements. Accurate frequency measurement occurs when f_{CLKOUT} = 16.384 kHz or lower is selected (see Table 14).

7.3.1.1 Temperature measurement

The PCF2129 has a temperature sensor circuit used to perform the temperature compensation of the frequency. The temperature is measured immediately after power-on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT_ctl.

Table 13. Temperature measurement period

TCR[1:0]		Temperature measurement period
00	[1]	4 min
01		2 min
10		1 min
11		30 seconds

[1] Default value.

7.3.2 OTP refresh

Each IC is calibrated during production and testing of the device. The calibration parameters are stored on EPROM cells called One Time Programmable (OTP) cells. It is recommended to process an OTP refresh once after the power is up and the oscillator is operating stable. The OTP refresh takes less than 100 ms to complete.

To perform an OTP refresh, bit OTPR has to be cleared (set to logic 0) and then set to logic 1 again.

7.3.3 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] control bits in register CLKOUT_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator.

CLKOUT is an open-drain output and enabled at power-on. When disabled, the output is high-impedance.

Table 14. CLKOUT frequency selection

COF[2:0]		CLKOUT frequency (Hz)	Typical duty cycle[1]
000	[2][3]	32 768	60 : 40 to 40 : 60
001		16 384	50 : 50
010		8 192	50 : 50
011		4 096	50 : 50
100		2 048	50 : 50

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 14. CLKOUT frequency selection*...continued*

COF[2:0]		CLKOUT frequency (Hz)	Typical duty cycle[1]
101		1 024	50 : 50
110		1	50 : 50
111		CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.
[2] Default value.
[3] The specified accuracy of the RTC can be only achieved with CLKOUT frequencies not equal to 32.768 kHz or if CLKOUT is disabled.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation all but the 32.768 kHz frequencies are 50 : 50.

7.4 Register Aging_offset

Table 15. Aging_offset - crystal aging offset register (address 19h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	AO[3:0]			
Reset value	-	-	-	-	1	0	0	0

Table 16. Aging_offset - crystal aging offset register (address 19h) bit description

Bit positions labeled as - are not implemented and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	-	-	unused
3 to 0	AO[3:0]	see Table 17	aging offset value

7.4.1 Crystal aging correction

The PCF2129 has an offset register Aging_offset to correct the crystal aging effects[2].

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative, in the temperature compensation circuit which allows correcting the aging effect.

At 25 °C, the aging offset bits allow a frequency correction of typically 1 ppm per AO[3:0] value, from -7 ppm to +8 ppm.

Table 17. Frequency correction at 25 °C, typical

AO[3:0]			ppm
Decimal	Binary		
0	0000		+8
1	0001		+7
2	0010		+6

2 For further information, refer to the application note [1].

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 17. Frequency correction at 25 °C, typical...*continued*

AO[3:0]			ppm
Decimal	Binary		
3	0011		+5
4	0100		+4
5	0101		+3
6	0110		+2
7	0111		+1
8	1000	[1]	0
9	1001		-1
10	1010		-2
11	1011		-3
12	1100		-4
13	1101		-5
14	1110		-6
15	1111		-7

[1] Default value.

7.5 Power management functions

The PCF2129 has two power supplies:

V_{DD}

the main power supply

V_{BAT}

the battery backup supply

Internally, the PCF2129 is operating with the internal operating voltage $V_{oper(int)}$ which is also available as V_{BBS} on the battery backed output voltage pin, BBS. Depending on the condition of the main power supply and the selected power management function, $V_{oper(int)}$ is either on the potential of V_{DD} or V_{BAT} (see Section 7.5.3).

Two power management functions are implemented:

Battery switch-over function

monitoring the main power supply V_{DD} and switching to V_{BAT} in case a power fail condition is detected (see Section 7.5.1).

Battery low detection function

monitoring the status of the battery, V_{BAT} (see Section 7.5.2).

The power management functions are controlled by the control bits PWRMNG[2:0] (see Table 18) in register Control_3 (see Table 10):

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 18. Power management control bit description

PWRMNG[2:0]		Function
000	[1]	battery switch-over function is enabled in standard mode; battery low detection function is enabled
001		battery switch-over function is enabled in standard mode; battery low detection function is disabled
010		battery switch-over function is enabled in standard mode; battery low detection function is disabled
011		battery switch-over function is enabled in direct switching mode; battery low detection function is enabled
100		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
101		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
111	[2]	battery switch-over function is disabled, only one power supply (V_{DD}); battery low detection function is disabled

[1] Default value.
[2] When the battery switch-over function is disabled, the PCF2129 works only with the power supply V_{DD}. V_{BAT} must be put to ground and the battery low detection function is disabled.

7.5.1 Battery switch-over function

The PCF2129 has a backup battery switch-over circuit which monitors the main power supply V_{DD}. When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

Standard mode

the power failure condition happens when:

$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. The battery switch-over in standard mode works only for $V_{DD} > 2.5$ V

Direct switching mode

the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 7.12.6).
3. If the control bit BTSE (register Control_3) is logic 1, the timestamp registers store the time and date when the battery switch occurred (see Section 7.11.4).
4. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

The interface is disabled in battery backup operation:

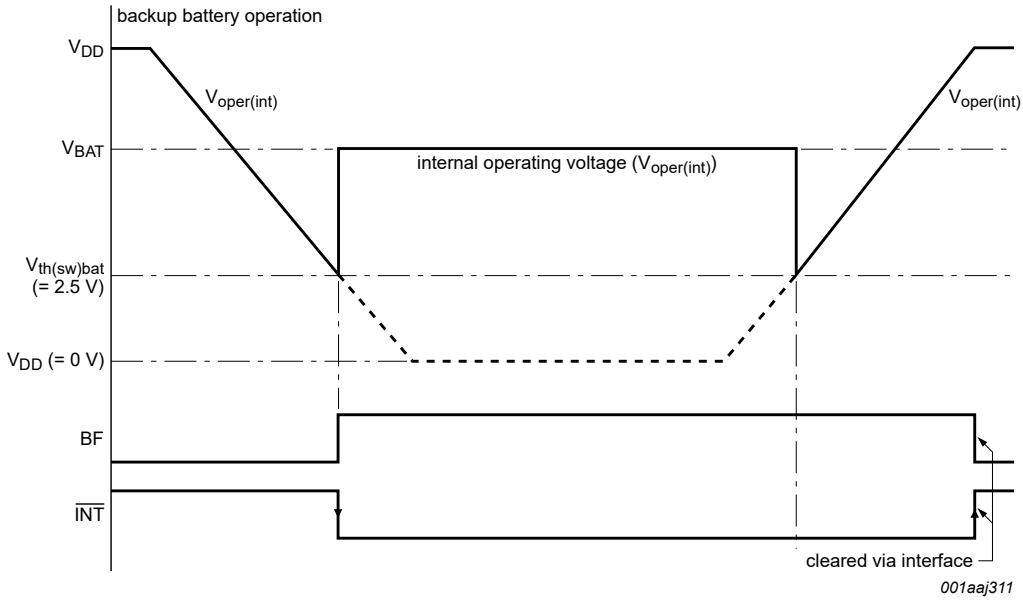
- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

For further information about I^2C-bus communication and battery backup operation, see Section 8.3.

7.5.1.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{BAT} potential.



$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. In standard mode, the battery switch-over works only for $V_{DD} > 2.5$ V.

V_{DD} may be lower than V_{BAT} (for example V_{DD} = 3 V, V_{BAT} = 4.1 V).

Figure 6. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled)

7.5.1.2 Direct switching mode

If $V_{DD} > V_{BAT}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$: $V_{oper(int)}$ is at V_{BAT} potential.

The direct switching mode is useful in systems where V_{DD} is always higher than V_{BAT}. This mode is not recommended if the V_{DD} and V_{BAT} values are similar (for example, V_{DD} = 3.3 V, $V_{BAT} \geq 3.0$ V). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

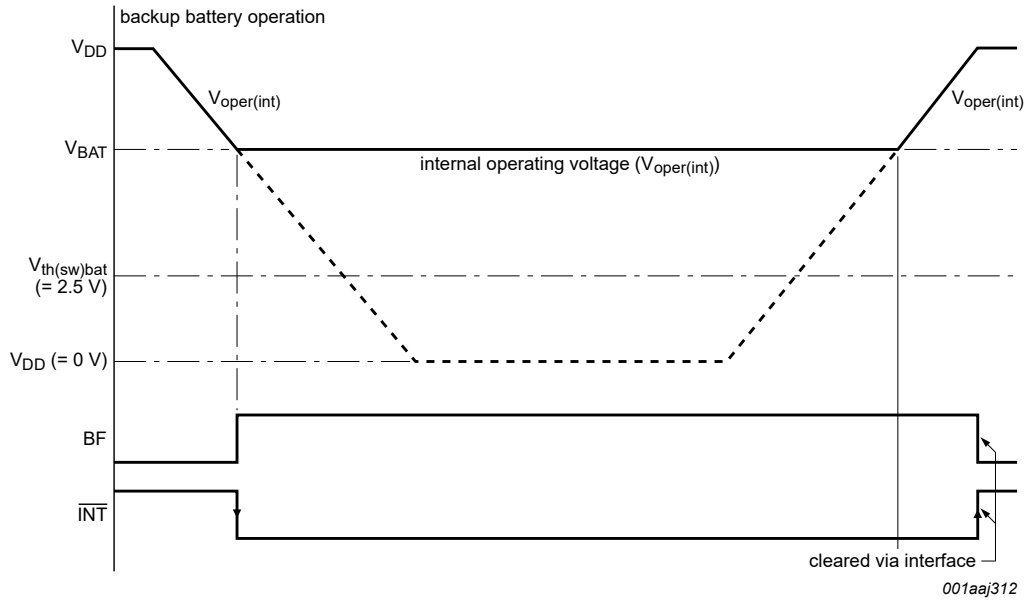


Figure 7. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled)

7.5.1.3 Battery switch-over disabled: only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- $V_{oper(int)}$ is at V_{DD} potential
- The battery flag (BF) is always logic 0

7.5.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in Figure 8.

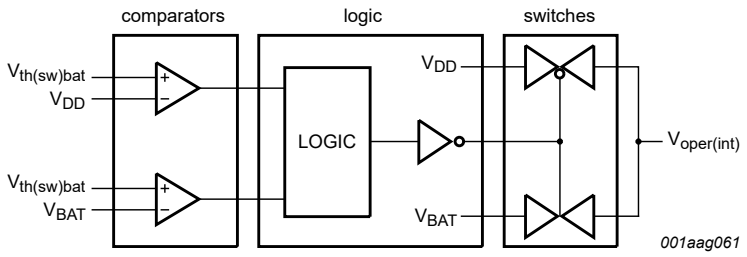


Figure 8. Battery switch-over circuit, simplified block diagram

$V_{oper(int)}$ is at V_{DD} or V_{BAT} potential.

Remark: It has to be assured that there are decoupling capacitors on the pins V_{DD}, V_{BAT}, and BBS.

7.5.2 Battery low detection function

The PCF2129 has a battery low detection circuit which monitors the status of the battery V_{BAT}.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V), the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery cannot prevent that the supply voltage drops below V_{low} (typical 1.2 V) and with that the data integrity gets lost. (For further information about V_{low} see Section 7.6.)

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 9):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled (see Section 7.12.7).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared by command. It is automatically cleared by the battery low detection circuit when the battery is replaced or when the voltage rises again above the threshold value. This could happen if a super capacitor is used as a backup source and the main power is applied again.

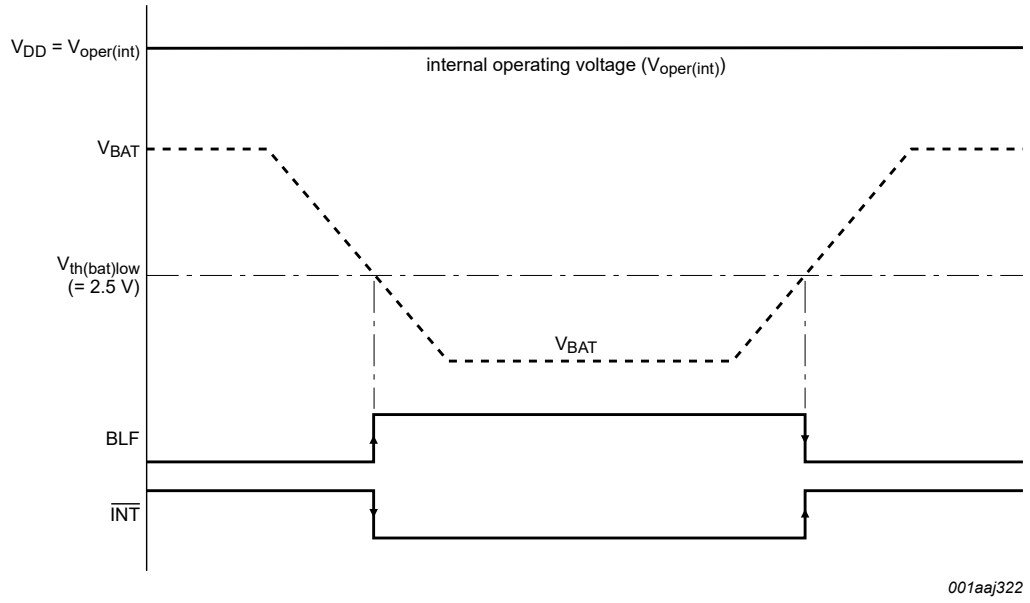


Figure 9. Battery low detection behavior with bit BLIE set logic 1 (enabled)

7.5.3 Battery backup supply

The V_{BBS} voltage on the output pin BBS is at the same potential as the internal operating voltage $V_{oper(int)}$, depending on the selected battery switch-over function mode:

Table 19. Output pin BBS

Battery switch-over function mode	Conditions	Potential of $V_{oper(int)}$ and V_{BBS}
standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	V_{DD}
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	V_{BAT}
direct switching	$V_{DD} > V_{BAT}$	V_{DD}

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 19. Output pin BBS*...continued*

Battery switch-over function mode	Conditions	Potential of $V_{oper(int)}$ and V_{BBS}
	$V_{DD} < V_{BAT}$	V_{BAT}
disabled	only V_{DD} available, V_{BAT} must be put to ground	V_{DD}

The output pin BBS can be used as a supply for external devices with battery backup needs, such as SRAM (see [1]). For this case, Figure 10 shows the typical driving capability when V_{BBS} is driven from V_{DD}.

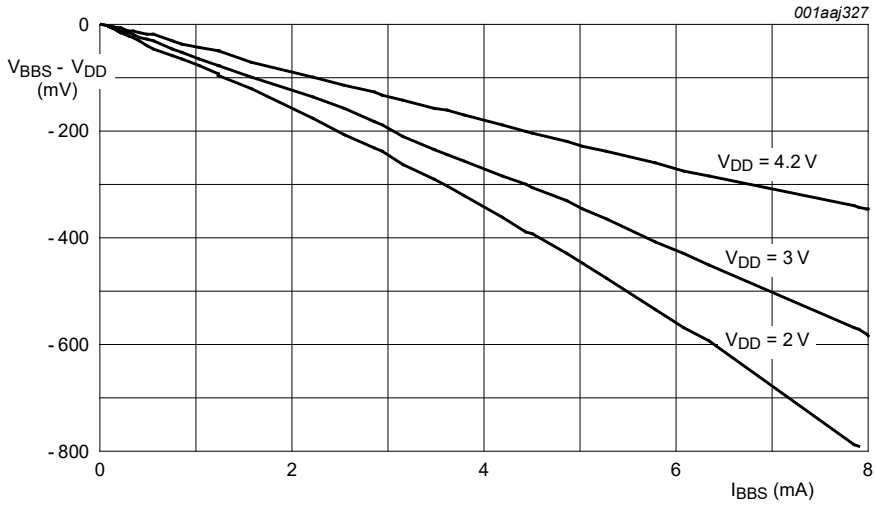


Figure 10. Typical driving capability of V_{BBS}: (V_{BBS} - V_{DD}) with respect to the output load current I_{BBS}

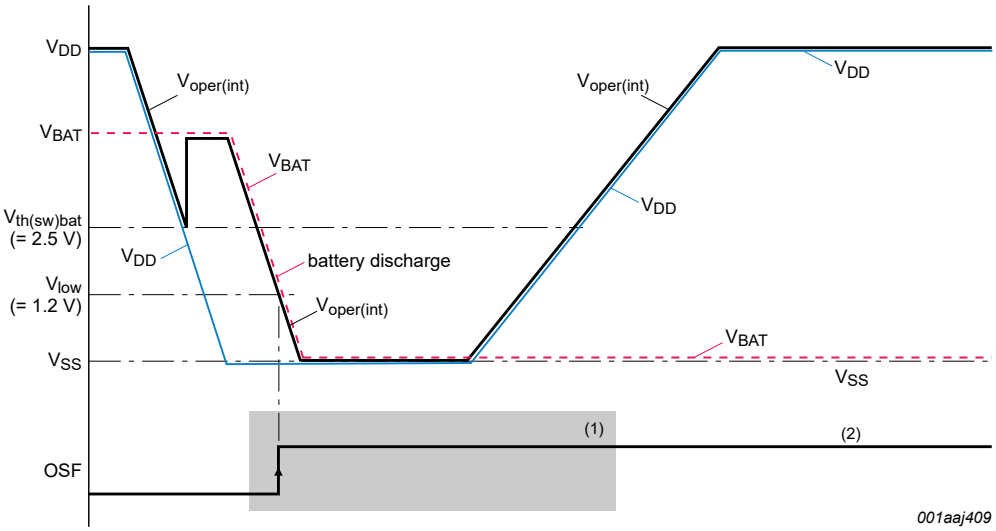
7.6 Oscillator stop detection function

The PCF2129 has an on-chip oscillator detection circuit which monitors the status of the oscillation: whenever the oscillation stops, a reset occurs and the oscillator stop flag OSF (in register Seconds) is set logic 1.

- **Power-on:**
  1. The oscillator is not running, the chip is in reset (OSF is logic 1).
  2. When the oscillator starts running and is stable after power-on, the chip exits from reset.
  3. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
- **Power supply failure:**
  1. When the power supply of the chip drops below a certain value (V_{low}), typically 1.2 V, the oscillator stops running and a reset occurs.
  2. When the power supply returns to normal operation, the oscillator starts running again, the chip exits from reset.
  3. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



1. Theoretical state of the signals since there is no power.
2. The oscillator stop flag (OSF), set logic 1, indicates that the oscillation has stopped and a reset has occurred since the flag was last cleared (OSF set logic 0). In this case, the integrity of the clock information is not guaranteed. The OSF flag is cleared by command.

Figure 11. Power failure event due to battery discharge: reset occurs

7.7 Reset function

The PCF2129 has a Power-On Reset (POR) and a Power-On Reset Override (PORO) function implemented.

7.7.1 Power-On Reset (POR)

The POR is active whenever the oscillator is stopped. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance (see Figure 12). This time may be in the range of 200 ms to 2 s depending on temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

The OTP refresh (see Section 7.3.2) should ideally be executed as the first instruction after start-up and also after a reset due to an oscillator stop.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

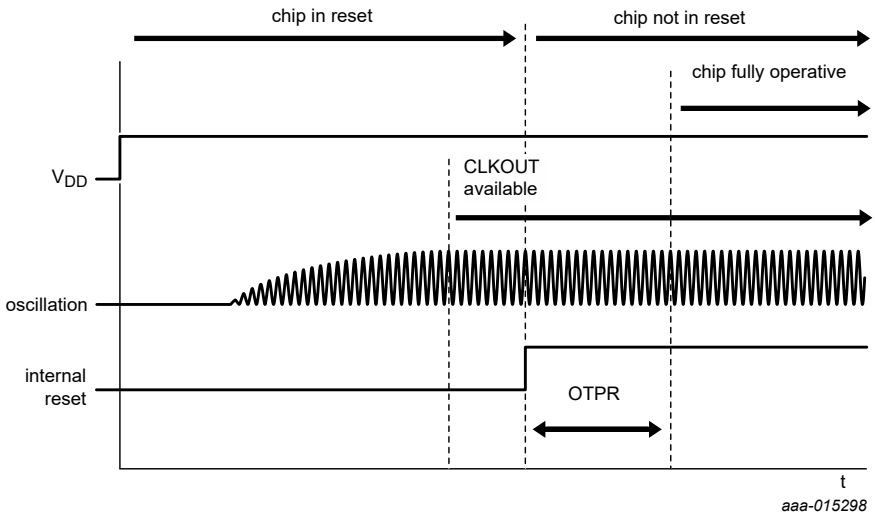


Figure 12. Dependency between POR and oscillator

After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- Power-On Reset Override (PORO) available to be set
- 24-hour mode is selected
- Battery switch-over is enabled
- Battery low detection is enabled

The register values after power-on are shown in Table 4.

7.7.2 Power-On Reset Override (PORO)

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and therefore speed up the on-board test of the device.

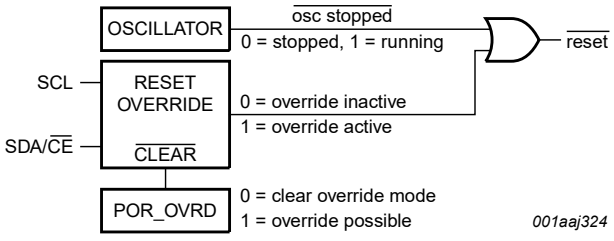


Figure 13. Power-On Reset (POR) system

The setting of the PORO mode requires that POR_OVRD in register Control_1 is set logic 1 and that the signals at the interface pins SDA/$\overline{CE}$ and SCL are toggled as illustrated in Figure 14. All timings shown are required minimum.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

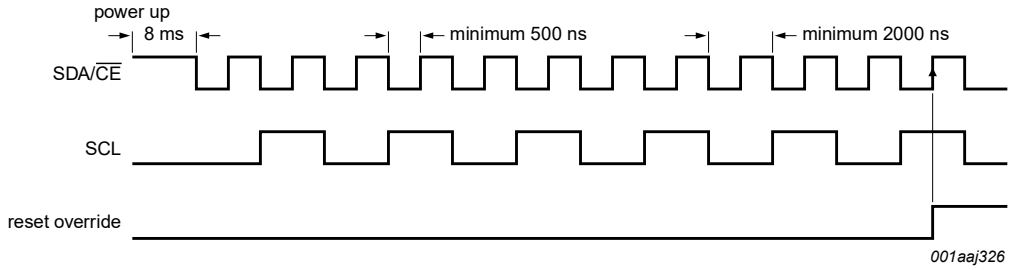


Figure 14. Power-On Reset Override (PORO) sequence, valid for both I²C-bus and SPI-bus

Once the override mode is entered, the device is immediately released from the reset state and the set-up operation can commence.

The PORO mode is cleared by writing logic 0 to POR_OVRD. POR_OVRD must be logic 1 before a re-entry into the override mode is possible. Setting POR_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the PORO mode.

7.8 Time and date function

Most of these registers are coded in the Binary Coded Decimal (BCD) format.

7.8.1 Register Seconds

Table 20. Seconds - seconds and clock integrity register (address 03h) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	OSF	SECONDS (0 to 59)						
Reset value	1	X	X	X	X	X	X	X

Table 21. Seconds - seconds and clock integrity register (address 03h) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	clock integrity is guaranteed
		1	-	clock integrity is not guaranteed: oscillator has stopped and chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

Table 22. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 22. Seconds coded in BCD format*...continued*

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

7.8.2 Register Minutes

Table 23. Minutes - minutes register (address 04h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	MINUTES (0 to 59)						
Reset value	-	X	X	X	X	X	X	X

Table 24. Minutes - minutes register (address 04h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

7.8.3 Register Hours

Table 25. Hours - hours register (address 05h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	AMPM	HOURS (1 to 12) in 12-hour mode				
			HOURS (0 to 23) in 24-hour mode					
Reset value	-	-	X	X	X	X	X	X

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 26. Hours - hours register (address 05h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12-hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours coded in BCD format when in 12-hour mode
3 to 0		0 to 9	unit place	
24-hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours coded in BCD format when in 24-hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1 (see Table 6).

7.8.4 Register Days

Table 27. Days - days register (address 06h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	DAYS (1 to 31)					
Reset value	-	-	X	X	X	X	X	X

Table 28. Days - days register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] If the year counter contains a value which is exactly divisible by 4, including the year 00, the RTC compensates for leap years by adding a 29th day to February.

7.8.5 Register Weekdays

Table 29. Weekdays - weekdays register (address 07h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	WEEKDAYS (0 to 6)		
Reset value	-	-	-	-	-	X	X	X

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 30. Weekdays - weekdays register (address 07h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday value, see Table 31

Although the association of the weekdays counter to the actual weekday is arbitrary, the PCF2129 assumes that Sunday is 000 and Monday is 001 for the purpose of determining the increment for calendar weeks.

Table 31. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be reassigned by the user.

7.8.6 Register Months

Table 32. Months - months register (address 08h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	MONTHS (1 to 12)				
Reset value	-	-	-	X	X	X	X	X

Table 33. Months - months register (address 08h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 34
3 to 0		0 to 9	unit place	

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 34. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

7.8.7 Register Years

Table 35. Years - years register (address 09h) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	YEARS (0 to 99)							
Reset value	X	X	X	X	X	X	X	X

Table 36. Years - years register (address 09h) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

7.8.8 Setting and reading the time

Figure 15 shows the data flow and data dependencies starting from the 1 Hz clock tick.

During read/write operations, the time counting circuits (memory locations 03h through 09h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

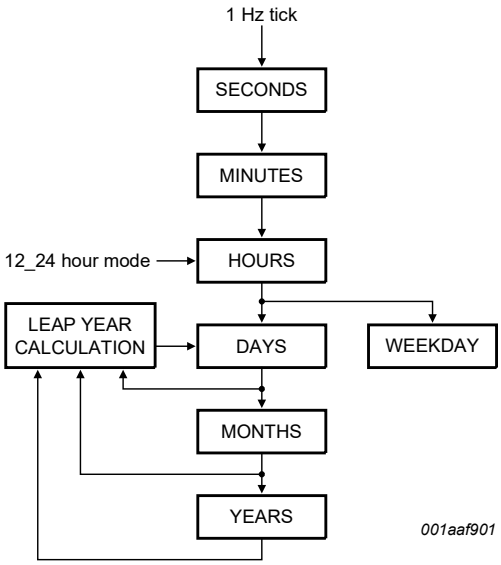


Figure 15. Data flow of the time function

After this read/write access is completed, the time circuit is released again. Any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 16).

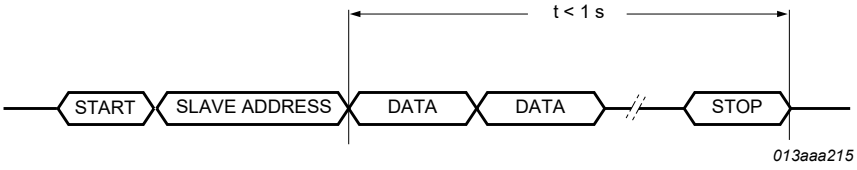


Figure 16. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go. That is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

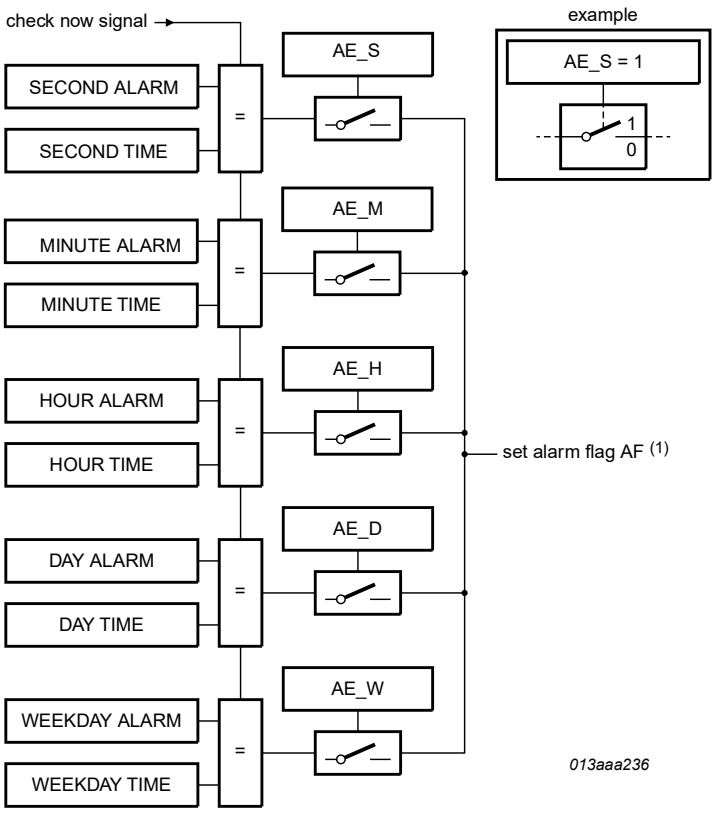
As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

7.9 Alarm function

When one or more of the alarm bit fields are loaded with a valid second, minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the actual second, minute, hour, day, and weekday (see Figure 17).

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



1. Only when all enabled alarm settings are matching.

Figure 17. Alarm function block diagram

The generation of interrupts from the alarm function is described in Section 7.12.4.

7.9.1 Register Second_alarm

Table 37. Second_alarm - second alarm register (address 0Ah) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_S	SECOND_ALARM (0 to 59)						
Reset value	1	X	X	X	X	X	X	X

Table 38. Second_alarm - second alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AE_S	0	-	second alarm is enabled
		1	-	second alarm is disabled
6 to 4	SECOND_ALARM	0 to 5	ten's place	second alarm information coded in BCD format
3 to 0		0 to 9	unit place	

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.9.2 Register Minute_alarm

Table 39. Minute_alarm - minute alarm register (address 0Bh) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_M	MINUTE_ALARM (0 to 59)						
Reset value	1	X	X	X	X	X	X	X

Table 40. Minute_alarm - minute alarm register (address 0Bh) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	minute alarm is enabled
		1	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

7.9.3 Register Hour_alarm

Table 41. Hour_alarm - hour alarm register (address 0Ch) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
			HOUR_ALARM (0 to 23) in 24-hour mode					
Reset value	1	-	X	X	X	X	X	X

Table 42. Hour_alarm - hour alarm register (address 0Ch) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	hour alarm is enabled
		1	-	hour alarm is disabled
6	-	-	-	unused
12-hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	unit place	
24-hour mode[1]				

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 42. Hour_alarm - hour alarm register (address 0Ch) bit description*...continued*

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

7.9.4 Register Day_alarm

Table 43. Day_alarm - day alarm register (address 0Dh) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_D	-	DAY_ALARM (1 to 31)					
Reset value	1	-	X	X	X	X	X	X

Table 44. Day_alarm - day alarm register (address 0Dh) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	day alarm is enabled
		1	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

7.9.5 Register Weekday_alarm

Table 45. Weekday_alarm - weekday alarm register (address 0Eh) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
Reset value	1	-	-	-	-	X	X	X

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 46. Weekday_alarm - weekday alarm register (address 0Eh) bit description

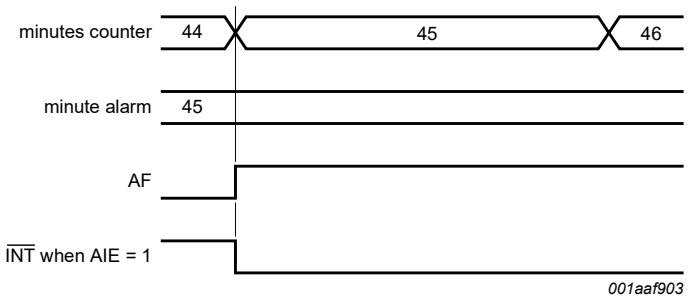
Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information

7.9.6 Alarm flag

When all enabled comparisons first match, the alarm flag AF (register Control_2) is set. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. For clearing the flags, see Section 7.10.5

Alarm registers which have their alarm enable bit AE_x at logic 1 are ignored.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 18. Alarm flag timing diagram

7.10 Timer functions

The PCF2129 has a watchdog timer function. The timer can be switched on and off by using the control bit WD_CD in the register Watchdg_tim_ctl.

The watchdog timer has four selectable source clocks. It can, for example, be used to detect a microcontroller with interrupt and reset capability which is out of control (see Section 7.10.3)

To control the timer function and timer output, the registers Control_2, Watchdg_tim_ctl, and Watchdg_tim_val are used.

7.10.1 Register Watchdg_tim_ctl

Table 47. Watchdg_tim_ctl - watchdog timer control register (address 10h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0.

Bit	7	6	5	4	3	2	1	0
Symbol	WD_CD	T	TI_TP	-	-	-	TF[1:0]	
Reset value	0	0	0	-	-	-	1	1

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 48. Watchdg_tim_ctl - watchdog timer control register (address 10h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as T must always be written with logic 0.

Bit	Symbol	Value	Description
7	WD_CD	0	watchdog timer disabled
		1	watchdog timer enabled; the interrupt pin $\overline{INT}$ is activated when timed out
6	T	0	unused
5	TI_TP	0	the interrupt pin $\overline{INT}$ is configured to generate a permanent active signal when MSF is set
		1	the interrupt pin $\overline{INT}$ is configured to generate a pulsed signal when MSF flag is set (see Figure 21)
4 to 2	-	-	unused
1 to 0	TF[1:0]		timer source clock for watchdog timer
		00	4.096 kHz
		01	64 Hz
		10	1 Hz
		11	$^{1}/_{60}$ Hz

7.10.2 Register Watchdg_tim_val

Table 49. Watchdg_tim_val - watchdog timer value register (address 11h) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	WATCHDG_TIM_VAL[7:0]							
Reset value	X	X	X	X	X	X	X	X

Table 50. Watchdg_tim_val - watchdog timer value register (address 11h) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 0	WATCHDG_TIM_ VAL[7:0]	00 to FF	timer period in seconds: $TimerPeriod = \frac{n}{SourceClockFrequency}$ where n is the timer value

Table 51. Programmable watchdog timer

TF[1:0]	Timer source clock frequency	Units	Minimum timer period (n = 1)	Units	Maximum timer period (n = 255)	Units
00	4.096	kHz	244	µs	62.256	ms
01	64	Hz	15.625	ms	3.984	s
10	1	Hz	1	s	255	s

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 51. Programmable watchdog timer...*continued*

TF[1:0]	Timer source clock frequency	Units	Minimum timer period (n = 1)	Units	Maximum timer period (n = 255)	Units
11	$^{1}/_{60}$	Hz	60	s	15 300	s

7.10.3 Watchdog timer function

The watchdog timer function is enabled or disabled by the WD_CD bit of the register Watchdg_tim_ctl (see Table 48).

The 2 bits TF[1:0] in register Watchdg_tim_ctl determine one of the four source clock frequencies for the watchdog timer: 4.096 kHz, 64 Hz, 1 Hz, or $^{1}/_{60}$ Hz (see Table 51).

When the watchdog timer function is enabled, the 8-bit timer in register Watchdg_tim_val determines the watchdog timer period (see Table 51).

The watchdog timer counts down from the software programmed 8-bit binary value n in register Watchdg_tim_val. When the counter reaches 1, the watchdog timer flag WDTF (register Control_2) is set logic 1 and an interrupt is generated.

The counter does not automatically reload.

When WD_CD is logic 0 (watchdog timer disabled) and the Microcontroller Unit (MCU) loads a watchdog timer value n:

- the flag WDTF is reset
- $\overline{INT}$ is cleared
- the watchdog timer starts again

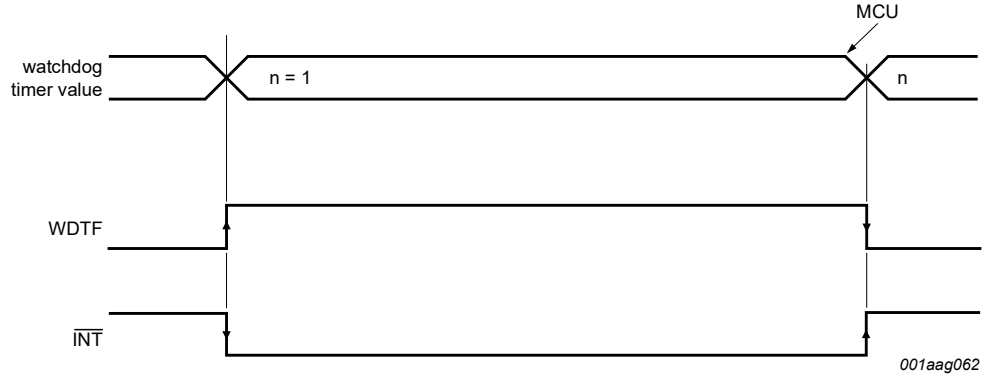
Loading the counter with 0 will:

- reset the flag WDTF
- clear $\overline{INT}$
- stop the watchdog timer

Remark: WDTF is read only and cannot be cleared by command. WDTF can be cleared by:

- loading a value in register Watchdg_tim_val
- reading of the register Control_2

Writing a logic 0 or logic 1 to WDTF has no effect.



Counter reached 1, WDTF is logic 1, and an interrupt is generated.

Figure 19. WD_CD set logic 1: watchdog activates an interrupt when timed out

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

- When the watchdog timer counter reaches 1, the watchdog timer flag WDTF is set logic 1
- When a minute or second interrupt occurs, the minute/second flag MSF is set logic 1 (see Section 7.12.1).

7.10.4 Pre-defined timers: second and minute interrupt

PCF2129 has two pre-defined timers which are used to generate an interrupt either once per second or once per minute (see Section 7.12.1). The pulse generator for the minute or second interrupt operates from an internal 64 Hz clock. It is independent of the watchdog timer. Each of these timers can be enabled by the bits SI (second interrupt) and MI (minute interrupt) in register Control_1.

7.10.5 Clearing flags

The flags MSF, AF, and TSFx can be cleared by command. To prevent one flag being overwritten while clearing another, a logic AND is performed during the write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Two examples are given for clearing the flags. Clearing a flag is made by a write command:

- Bits labeled with - must be written with their previous values
- Bits labeled with T have to be written with logic 0
- WDTF is read only and has to be written with logic 0

Repeatedly rewriting these bits has no influence on the functional behavior.

Table 52. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	MSF	WDTF	TSF2	AF	T	-	-	T

Table 53. Example values in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	1	0	0	0	0

The following tables show what instruction must be sent to clear the appropriate flag.

Table 54. Example to clear only AF (bit 4)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	0	0	0[1]	0[1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 55. Example to clear only MSF (bit 7)

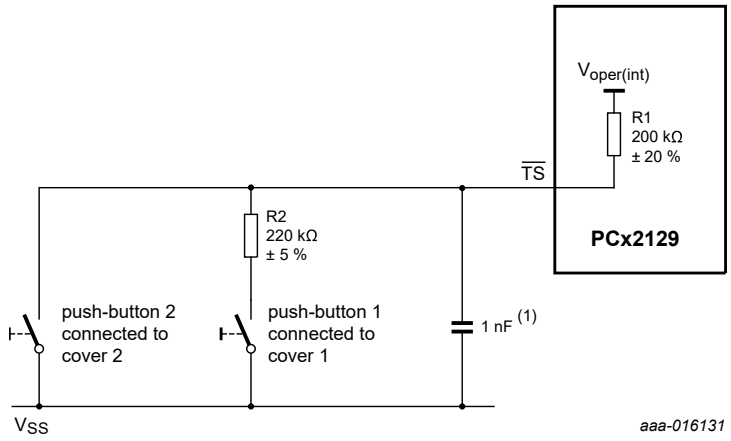
Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	0	1	1	0	0[1]	0[1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

7.11 Timestamp function

The PCF2129 has an active LOW timestamp input pin $\overline{TS}$, internally pulled with an on-chip pull-up resistor to $V_{oper(int)}$. It also has a timestamp detection circuit which can detect two different events:

1. Input on pin $\overline{TS}$ is driven to an intermediate level between power supply and ground.
2. Input on pin $\overline{TS}$ is driven to ground.



1. When using switches or push-buttons, it is recommended to connect a 1 nF capacitance to the $\overline{TS}$ pin to ensure proper switching.

Figure 20. Timestamp detection with two push-buttons on the TS pin (for example, for tamper detection)

The timestamp function is enabled by default after power-on and it can be switched off by setting the control bit TSOFF (register Timestp_ctl).

A most common application of the timestamp function is described in [1].

See Section 7.12.5 for a description of interrupt generation from the timestamp function.

7.11.1 Timestamp flag

1. When the $\overline{TS}$ input pin is driven to an intermediate level between the power supply and ground, either on the falling edge from V_{DD} or on the rising edge from ground, then the following sequence occurs:
2. The actual date and time are stored in the timestamp registers.
3. The timestamp flag TSF1 (register Control_1) is set.
4. If the TSIE bit (register Control_2) is active, an interrupt on the $\overline{INT}$ pin is generated.

The TSF1 flag can be cleared by command. Clearing the flag clears the interrupt. Once TSF1 is cleared, it will only be set again when a new negative or positive edge on pin $\overline{TS}$ is detected.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

1. When the $\overline{TS}$ input pin is driven to ground, the following sequence occurs:
2. The actual date and time are stored in the timestamp registers.
3. In addition to the TSF1 flag, the TSF2 flag (register Control_2) is set.
4. If the TSIE bit is active, an interrupt on the $\overline{INT}$ pin is generated.

The TSF1 and TSF2 flags can be cleared by command; clearing both flags clears the interrupt. Once TSF2 is cleared, it will only be set again when $\overline{TS}$ pin is driven to ground once again.

7.11.2 Timestamp mode

The timestamp function has two different modes selected by the control bit TSM (timestamp mode) in register Timestp_ctl:

- If TSM is logic 0 (default): in subsequent trigger events without clearing the timestamp flags, the last timestamp event is stored
- If TSM is logic 1: in subsequent trigger events without clearing the timestamp flags, the first timestamp event is stored

The timestamp function also depends on the control bit BTSE in register Control_3, see Section 7.11.4.

7.11.3 Timestamp registers

7.11.3.1 Register Timestp_ctl

Table 56. Timestp_ctl - timestamp control register (address 12h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]				
Reset value	0	0	-	X	X	X	X	X

Table 57. Timestp_ctl - timestamp control register (address 12h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7	TSM	0	in subsequent events without clearing the timestamp flags, the last event is stored
		1	in subsequent events without clearing the timestamp flags, the first event is stored
6	TSOFF	0	timestamp function active
		1	timestamp function disabled
5	-	-	unused
4 to 0	1_O_16_TIMESTP[4:0]		$^{1}/_{16}$ second timestamp information coded in BCD format

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.11.3.2 Register Sec_timestp

Table 58. Sec_timestp - second timestamp register (address 13h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	SECOND_TIMESTP (0 to 59)						
Reset value	-	X	X	X	X	X	X	X

Table 59. Sec_timestp - second timestamp register (address 13h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	SECOND_TIMESTP	0 to 5	ten's place	second timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.11.3.3 Register Min_timestp

Table 60. Min_timestp - minute timestamp register (address 14h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	MINUTE_TIMESTP (0 to 59)						
Reset value	-	X	X	X	X	X	X	X

Table 61. Min_timestp - minute timestamp register (address 14h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTE_TIMESTP	0 to 5	ten's place	minute timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.11.3.4 Register Hour_timestp

Table 62. Hour_timestp - hour timestamp register (address 15h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
			HOUR_TIMESTP (0 to 23) in 24-hour mode					

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 62. Hour_timestp - hour timestamp register (address 15h) bit allocation*...continued*

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Reset value	-	-	X	X	X	X	X	X

Table 63. Hour_timestp - hour timestamp register (address 15h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12-hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_TIMESTP	0 to 1	ten's place	hour timestamp information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	unit place	
24-hour mode[1]				
5 to 4	HOUR_TIMESTP	0 to 2	ten's place	hour timestamp information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

7.11.3.5 Register Day_timestp

Table 64. Day_timestp - day timestamp register (address 16h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	DAY_TIMESTP (1 to 31)					
Reset value	-	-	X	X	X	X	X	X

Table 65. Day_timestp - day timestamp register (address 16h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAY_TIMESTP	0 to 3	ten's place	day timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.11.3.6 Register Mon_timestp

Table 66. Mon_timestp - month timestamp register (address 17h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	MONTH_TIMESTP (1 to 12)				
Reset value	-	-	-	X	X	X	X	X

Table 67. Mon_timestp - month timestamp register (address 17h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTH_TIMESTP	0 to 1	ten's place	month timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.11.3.7 Register Year_timestp

Table 68. Year_timestp - year timestamp register (address 18h) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	YEAR_TIMESTP (0 to 99)							
Reset value	X	X	X	X	X	X	X	X

Table 69. Year_timestp - year timestamp register (address 18h) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7 to 4	YEAR_TIMESTP	0 to 9	ten's place	year timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.11.4 Dependency between Battery switch-over and timestamp

The timestamp function depends on the control bit BTSE in register Control-_3:

Table 70. Battery switch-over and timestamp

BTSE	BF		Description
0	-	[1]	the battery switch-over does not affect the timestamp registers
1			If a battery switch-over event occurs:

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 70. Battery switch-over and timestamp*...continued*

BTSE	BF		Description
	0	[1]	the timestamp registers store the time and date when the switch-over occurs; after this event occurred BF is set logic 1
	1		the timestamp registers are not modified; in this condition subsequent battery switch-over events or falling edges on pin $\overline{TS}$ are not registered

[1] Default value.

7.12 Interrupt output, INT

PCF2129 has an interrupt output pin $\overline{INT}$ which is open-drain, active LOW (requiring a pull-up resistor if used). Interrupts may be sourced from different places:

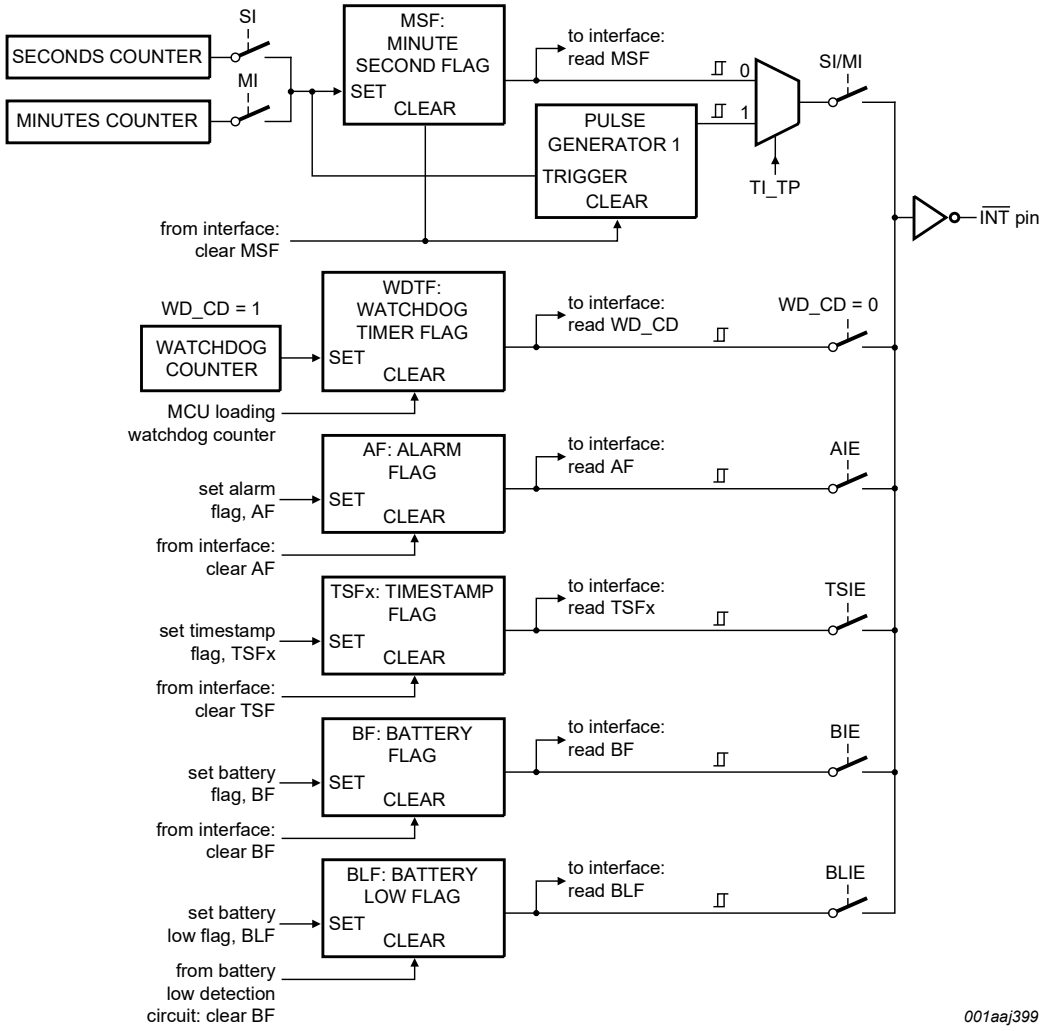
- second or minute timer
- watchdog timer
- alarm
- timestamp
- battery switch-over
- battery low detection

The control bit TI_TP (register Watchdg_tim_ctl) is used to configure whether the interrupts generated from the second/minute timer (flag MSF in register Control_2) are pulsed signals or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal which follows the status of the corresponding flags. When the interrupt sources are all disabled, $\overline{INT}$ remains high-impedance.

- The flags MSF, AF, TSFx, and BF can be cleared by command.
- The flag WDTF is read only. How it can be cleared is explained in Section 7.10.5.
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



When SI, MI, WD_CD, AIE, TSIE, BIE, BLIE are all disabled, $\overline{INT}$ remains high-impedance.

Figure 21. Interrupt block diagram

7.12.1 Minute and second interrupts

Minute and second interrupts are generated by predefined timers. The timers can be enabled independently from one another by the bits MI and SI in register Control_1. However, a minute interrupt enabled on top of a second interrupt cannot be distinguishable since it occurs at the same time.

The minute/second flag MSF (register Control_2) is set logic 1 when either the seconds or the minutes counter increments according to the enabled interrupt (see Table 71). The MSF flag can be cleared by command.

Table 71. Effect of bits MI and SI on pin $\overline{INT}$ and bit MSF

MI	SI	Result on $\overline{INT}$	Result on MSF
0	0	no interrupt generated	MSF never set
1	0	an interrupt once per minute	MSF set when **minutes** counter increments

All information provided in this document is subject to legal disclaimers.

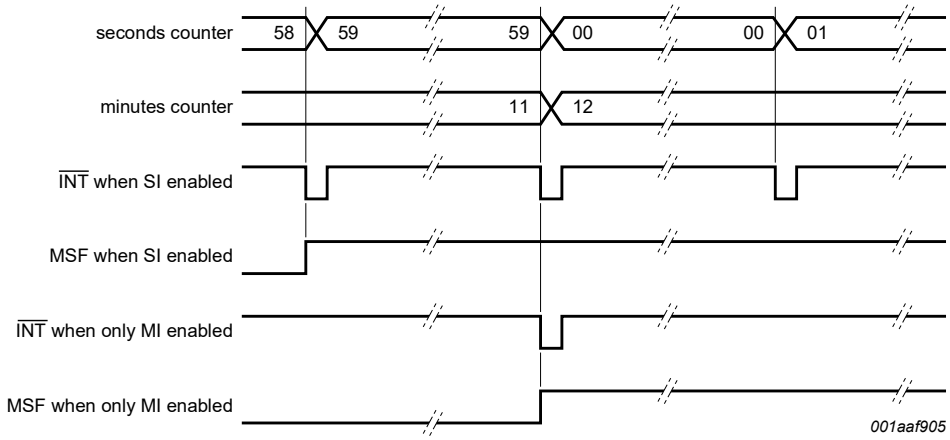
© 2022 NXP B.V. All rights reserved.

Table 71. Effect of bits MI and SI on pin $\overline{INT}$ and bit MSF*...continued*

MI	SI	Result on $\overline{INT}$	Result on MSF
0	1	an interrupt once per second	MSF set when **seconds** counter increments
1	1	an interrupt once per second	MSF set when **seconds** counter increments

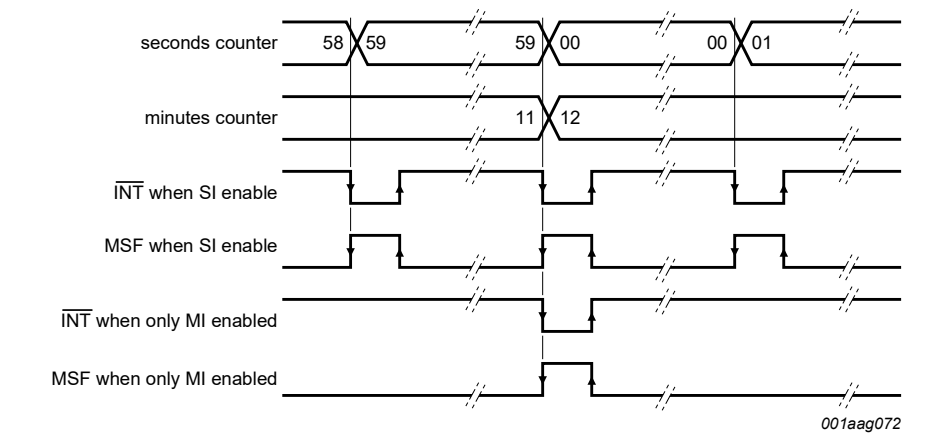
When MSF is set logic 1:

- If TI_TP is logic 1, the interrupt is generated as a pulsed signal.
- If TI_TP is logic 0, the interrupt is permanently active signal that remains until MSF is cleared.



In this example, bit TI_TP is logic 1 and the MSF flag is not cleared after an interrupt.

Figure 22. INT example for SI and MI when TI_TP is logic 1



In this example, bit TI_TP is logic 0 and the MSF flag is cleared after an interrupt.

Figure 23. INT example for SI and MI when TI_TP is logic 0

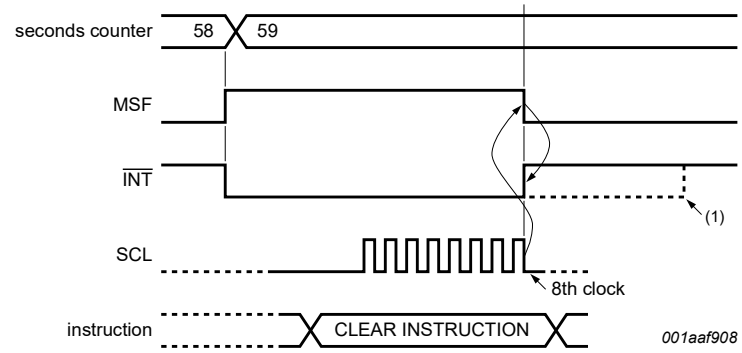
The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and generates a pulse of $^{1}/_{64}$ seconds in duration.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

7.12.2 INT pulse shortening

If the MSF flag (register Control_2) is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately when it is serviced, that is, the system does not have to wait for the completion of the pulse before continuing; see Figure 24. Instructions for clearing the bit MSF can be found in Section 7.10.5.



1. Indicates normal duration of $\overline{INT}$ pulse.

The timing shown for clearing bit MSF is also valid for the non-pulsed interrupt mode, that is, when TI_TP is logic 0, where the $\overline{INT}$ pulse may be shortened by setting both bits MI and SI logic 0.

Figure 24. Example of shortening the INT pulse by clearing the MSF flag

7.12.3 Watchdog timer interrupts

The generation of interrupts from the watchdog timer is controlled using the WD_CD bit (register Watchdg_tim_ctl). The interrupt is generated as an active signal which follows the status of the watchdog timer flag WDTF (register Control_2). No pulse generation is possible for watchdog timer interrupts.

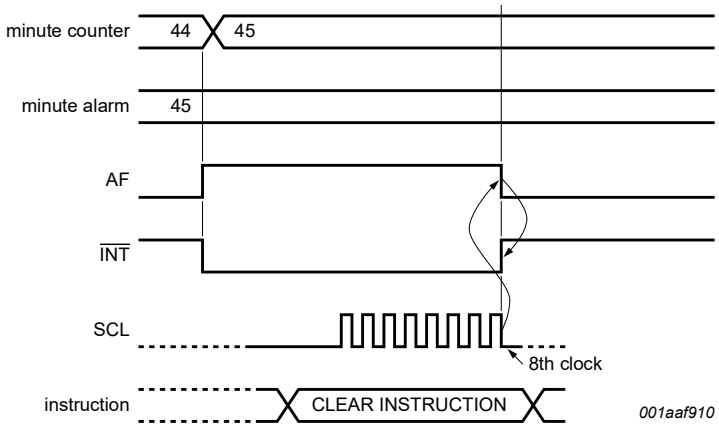
The interrupt is cleared when the flag WDTF is reset. WDTF is a read-only bit and cannot be cleared by command. Instructions for clearing it can be found in Section 7.10.5.

7.12.4 Alarm interrupts

Generation of interrupts from the alarm function is controlled by the bit AIE (register Control_2). If AIE is enabled, the $\overline{INT}$ pin follows the status of bit AF (register Control_2). Clearing AF immediately clears $\overline{INT}$. No pulse generation is possible for alarm interrupts.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 25. AF timing diagram

7.12.5 Timestamp interrupts

Interrupt generation from the timestamp function is controlled using the TSIE bit (register Control_2). If TSIE is enabled, the $\overline{INT}$ pin follows the status of the flags TSFx. Clearing the flags TSFx immediately clears $\overline{INT}$. No pulse generation is possible for timestamp interrupts.

7.12.6 Battery switch-over interrupts

Generation of interrupts from the battery switch-over is controlled by the BIE bit (register Control_3). If BIE is enabled, the $\overline{INT}$ pin follows the status of bit BF in register Control_3 (see Table 70). Clearing BF immediately clears $\overline{INT}$. No pulse generation is possible for battery switch-over interrupts.

7.12.7 Battery low detection interrupts

Generation of interrupts from the battery low detection is controlled by the BLIE bit (register Control_3). If BLIE is enabled, the $\overline{INT}$ pin follows the status of bit BLF (register Control_3). The interrupt is cleared when the battery is replaced (BLF is logic 0) or when bit BLIE is disabled (BLIE is logic 0). BLF is read only and therefore cannot be cleared by command.

7.13 External clock test mode

A test mode is available which allows on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST logic 1 (register Control_1). Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal (64 Hz) with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1 000 ns. The internal clock, now sourced from CLKOUT, is divided down by a 2^6 divider chain called prescaler (see Table 72). The prescaler can be set into a known state by using bit STOP. When bit STOP is logic 1, the prescaler is reset to 0. STOP must be cleared before the prescaler can operate again.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operating example:

1. Set EXT_TEST test mode (register Control_1, EXT_TEST is logic 1).
2. Set bit STOP (register Control_1, STOP is logic 1).
3. Set time registers to desired value.
4. Clear STOP (register Control_1, STOP is logic 0).
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

7.14 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. STOP causes the upper part of the prescaler (F_9 to F_{14}) to be held in reset and thus no 1 Hz ticks are generated. The time circuits can then be set and will not increment until the STOP bit is released. STOP doesn't affect the CLKOUT signal but the output of the prescaler in the range of 32 Hz to 1 Hz (see Figure 26).

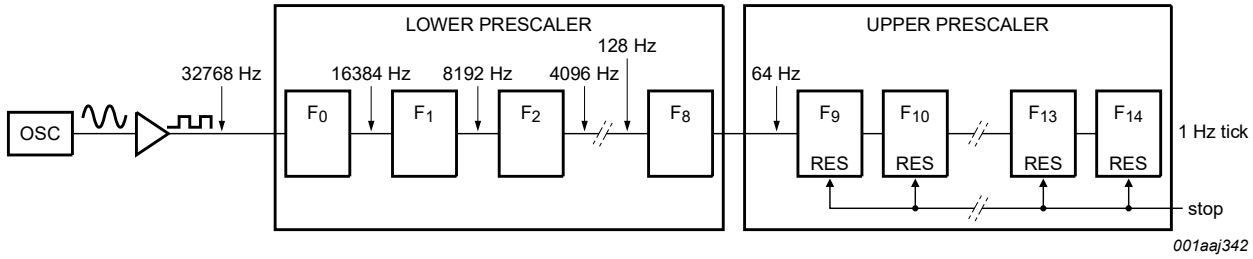


Figure 26. STOP bit functional diagram

The lower stages of the prescaler, F_0 to F_8, are not reset and because the I^2C-bus and the SPI-bus are asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between 0 and one 64 Hz cycle (0.484 375 s and 0.500 000 s), see Table 72 and Figure 27.

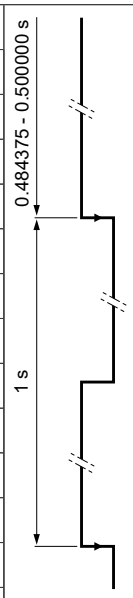
Table 72. First increment of time circuits after stop release

Bit STOP	Prescaler bits[1] F_0 to F_8 - F_9 to F_{14}	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	010000111-010100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0 to F_8 are not reset and values cannot be predicted externally				
1	xxxxxxxxx-000000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	xxxxxxxxx-000000		08:00:00	prescaler is reset; time circuits are frozen

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 72. First increment of time circuits after stop release*...continued*

Bit STOP	Prescaler bits[1] F_0 to F_8 - F_9 to F_{14}	1 Hz tick	Time hh:mm:ss	Comment
STOP bit is released by user				
0	xxxxxxxxx-000000		08:00:00	prescaler is now running
0	xxxxxxxxx-100000		08:00:00	
0	xxxxxxxxx-100000		08:00:00	
0	xxxxxxxxx-110000		08:00:00	
:	:		:	
0	111111111-111110		08:00:00	
0	000000000-000001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
0	100000000-000001		08:00:01	
:	:		:	
0	111111111-111111		08:00:01	
0	000000000-000000		08:00:01	
0	100000000-000000			
:	:		:	
0	111111111-111110		08:00:01	
0	000000000-000001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

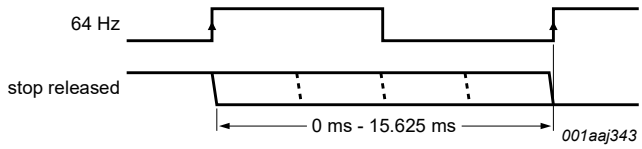


Figure 27. STOP bit release timing

8 Interfaces

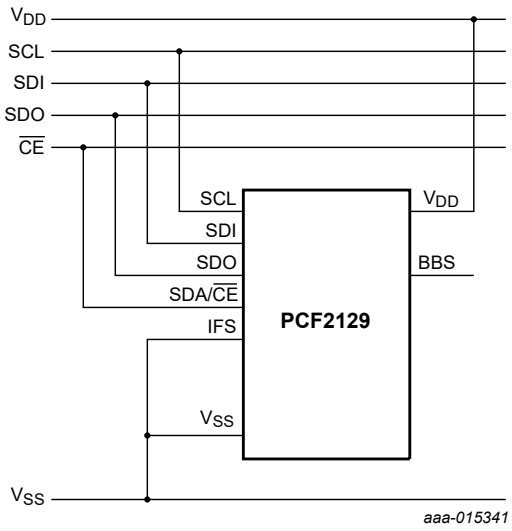
The PCF2129 has an I^2C-bus or SPI-bus interface using the same pins. The selection is done using the interface selection pin IFS (see Table 73).

Table 73. Interface selection input pin IFS

Pin	Connection	Bus interface	Reference
IFS	V_{SS}	SPI-bus	Section 8.1
	BBS	I^2C-bus	Section 8.2

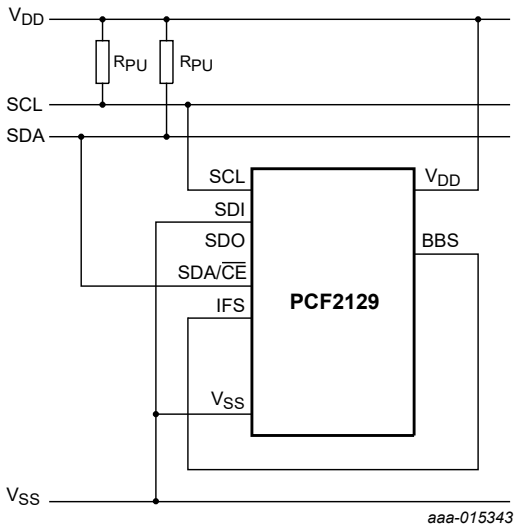
All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



To select the SPI-bus interface, pin IFS has to be connected to pin V_{SS}.

a. SPI-bus interface selection



To select the I^2C-bus interface, pin IFS has to be connected to pin BBS.

b. I^2C-bus interface selection

Figure 28. Interface selection

8.1 SPI-bus interface

Data transfer to and from the device is made by a 3 line SPI-bus (see Table 74). The data lines for input and output are split. The data input and output line can be connected together to facilitate a bidirectional data bus (see Figure 29). The SPI-bus is initialized whenever the chip enable line pin SDA/$\overline{CE}$ is inactive.

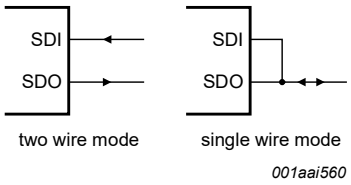


Figure 29. SDI, SDO configurations

Table 74. Serial interface

Symbol	Function		Description
SDA/$\overline{CE}$	chip enable input; active LOW	[1]	when HIGH, the interface is reset; input may be higher than V_{DD}
SCL	serial clock input		when SDA/$\overline{CE}$ is HIGH, input may float; input may be higher than V_{DD}
SDI	serial data input		when SDA/$\overline{CE}$ is HIGH, input may float; input may be higher than V_{DD}; input data is sampled on the rising edge of SCL

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 74. Serial interface...*continued*

Symbol	Function		Description
SDO	serial data output		push-pull output; drives from V_{SS} to $V_{oper(int)}$ (V_{BBS}); output data is changed on the falling edge of SCL

[1] The chip enable must not be wired permanently LOW.

8.1.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a whole byte, with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal SDA/$\overline{CE}$. The first byte transmitted is the command byte. Subsequent bytes are either data to be written or data to be read (see Figure 30).

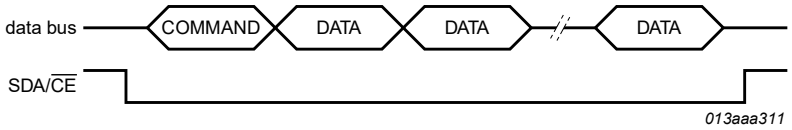


Figure 30. Data transfer overview

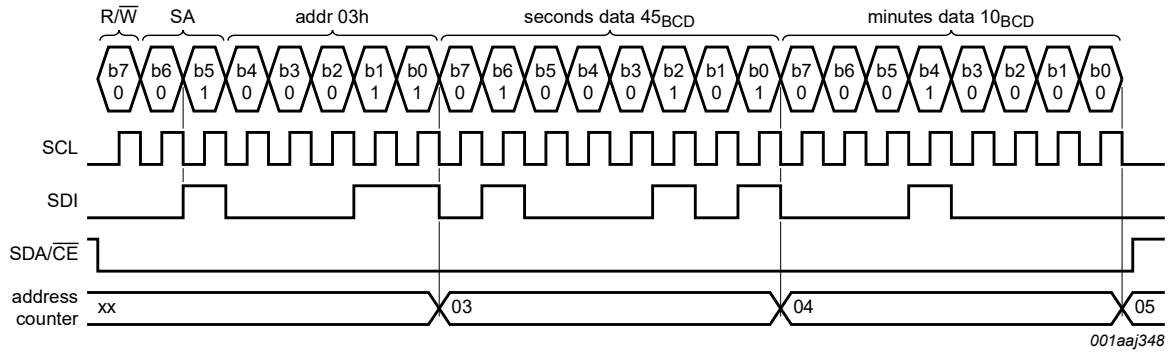
The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The R/$\overline{W}$ bit defines if the following bytes are read or write information.

Table 75. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or write selection
		0	write data
		1	read data
6 to 5	SA	01	subaddress; other codes will cause the device to ignore data transfer
4 to 0	RA	00h to 1Bh	register address

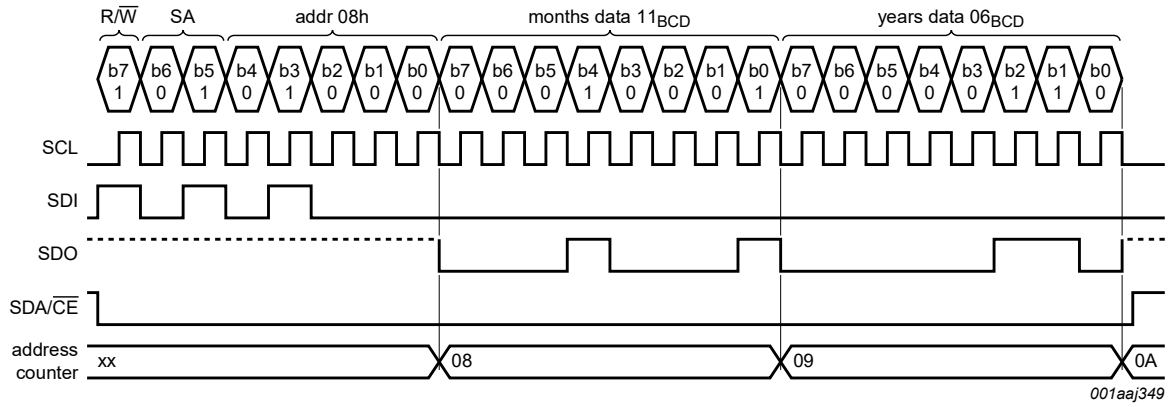
All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



In this example, the Seconds register is set to 45 seconds and the Minutes register to 10 minutes.

Figure 31. SPI-bus write example



In this example, the registers Months and Years are read. The pins SDI and SDO are not connected together. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents may result.

Figure 32. SPI-bus read example

8.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines are connected to a positive supply by a pull-up resistor. Data transfer is initiated only when the bus is not busy.

8.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 33).

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

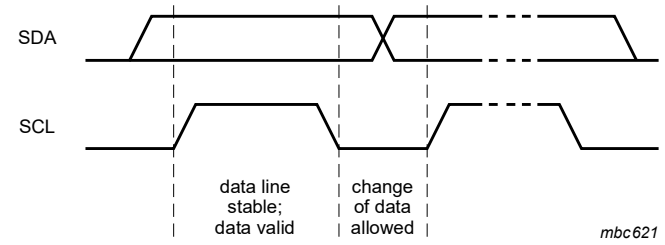


Figure 33. Bit transfer

8.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition S. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P (see Figure 34).

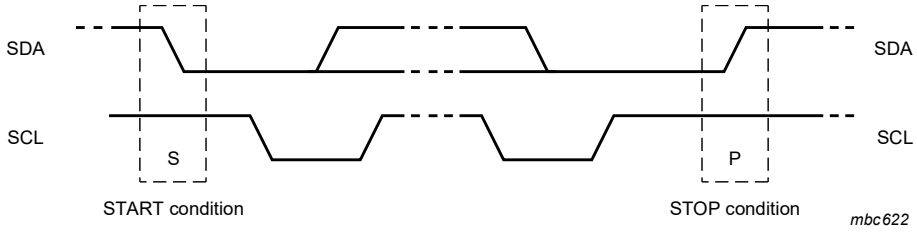


Figure 34. Definition of START and STOP conditions

Remark: For the PCF2129, a repeated START is not allowed. Therefore a STOP has to be released before the next START.

8.2.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves.

The PCF2129 can act as a slave transmitter and a slave receiver.

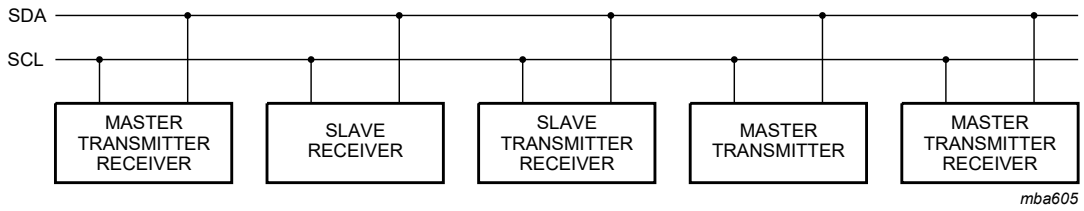


Figure 35. System configuration

8.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is illustrated in Figure 36.

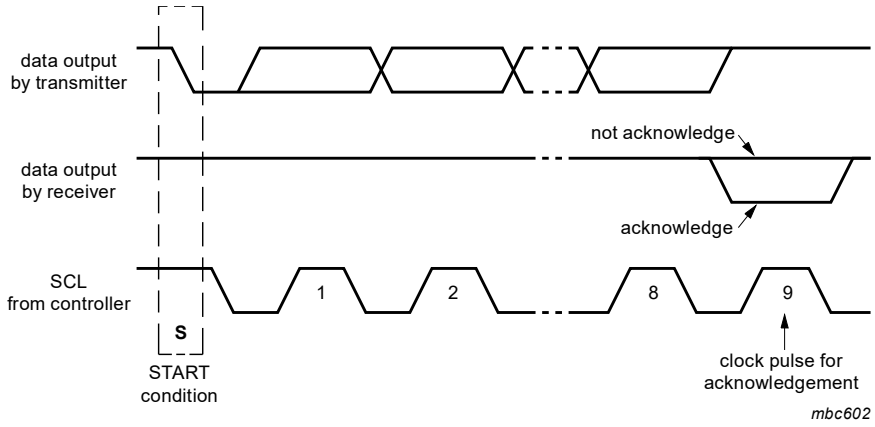


Figure 36. Acknowledgement on the I^2C-bus

8.2.5 I^2C-bus protocol

After a start condition, a valid hardware address has to be sent to a PCF2129 device. The appropriate I^2C-bus slave address is 1010 001. The entire I^2C-bus slave address byte is shown in Table 76.

Table 76. I^2C slave address byte

	Slave address							
Bit	7	6	5	4	3	2	1	0
	MSB							LSB
	1	0	1	0	0	0	1	R/$\overline{W}$

The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer (read is logic 1, write is logic 0).

For the format and the timing of the START condition (S), the STOP condition (P), and the acknowledge (A) refer to the I^2C-bus specification [7] and the characteristics table (Table 81). In the write mode, a data transfer is terminated by sending a STOP condition. A repeated START (Sr) condition is not applicable.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

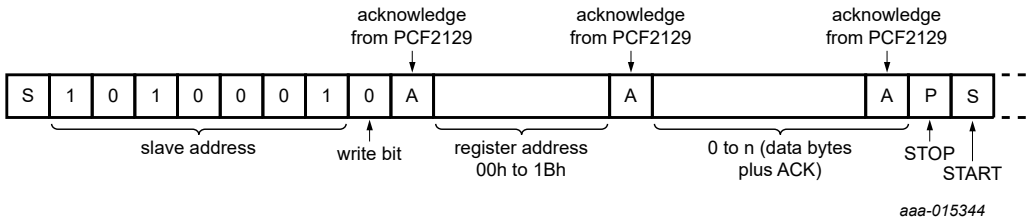


Figure 37. Bus protocol, writing to registers

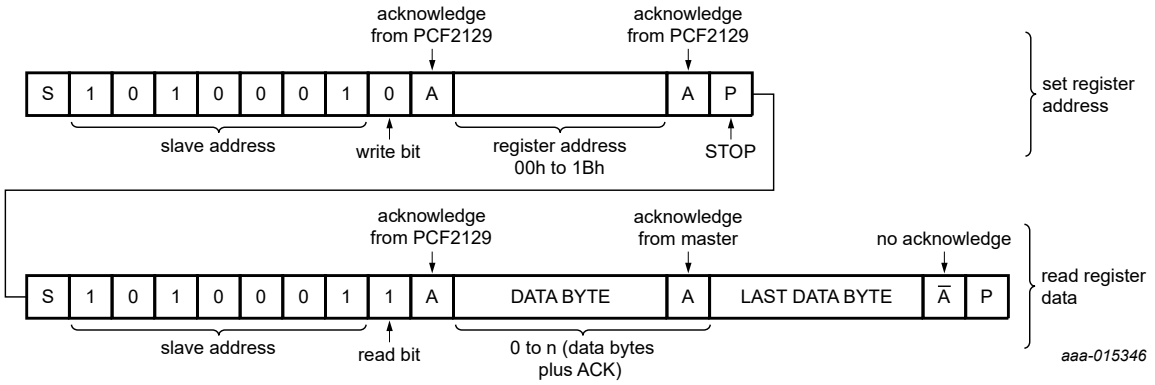


Figure 38. Bus protocol, reading from registers

8.3 Bus communication and battery backup operation

To save power during battery backup operation (see Section 7.5.1), the bus interfaces are inactive. Therefore the communication via I^2C- or SPI-bus should be terminated before the supply of the PCF2129 is switched from V_{DD} to V_{BAT}.

Remark: If the I^2C-bus communication was terminated uncontrolled, the I^2C-bus has to be reinitialized by sending a STOP followed by a START after the device switched back from battery backup operation to V_{DD} supply operation.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

9 Internal circuitry

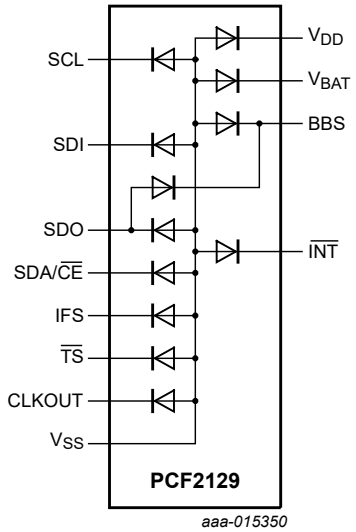


Figure 39. Device diode protection diagram of PCF2129

10 Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

11 Limiting values

Table 77. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.5	V
I_{DD}	supply current			-50	+50	mA
V_i	input voltage			-0.5	+6.5	V
I_I	input current			-10	+10	mA
V_O	output voltage			-0.5	+6.5	V
I_O	output current			-10	+10	mA
		at pin SDA/$\overline{CE}$		-10	+20	mA
V_{BAT}	battery supply voltage			-0.5	+6.5	V
P_{tot}	total power dissipation			-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±4 000	V
		CDM	[2]	-	±1 250	V

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 77. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{lu}	latch-up current		[3]	-	200	mA
T_{stg}	storage temperature		[4]	-55	+85	°C
T_{amb}	ambient temperature	operating device		-40	+85	°C

[1] Pass level; Human Body Model (HBM) according to [2].
[2] Pass level; Charged-Device Model (CDM), according to [3].
[3] Pass level; latch-up testing according to [4] at maximum ambient temperature ($T_{amb(max)}$).
[4] According to the store and transport requirements (see [8]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

12 Static characteristics

Table 78. Static characteristics

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage		[1]	1.8	-	4.2	V
V_{BAT}	battery supply voltage			1.8	-	4.2	V
$V_{DD(cal)}$	calibration supply voltage			-	3.3	-	V
V_{low}	low voltage			-	1.2	-	V
I_{DD}	supply current	interface active; supplied by V_{DD}					
		SPI-bus (f_{SCL} = 6.5 MHz)		-	-	800	µA
		I^2C-bus (f_{SCL} = 400 kHz)		-	-	200	µA
		interface inactive (f_{SCL} = 0 Hz)[2]; TCR[1:0] = 00 (see Table 12)					
		PWRMNG[2:0] = 111 (see Table 18); TSOFF = 1 (see Table 57); COF[2:0] = 111 (see Table 14)					
		V_{DD} = 1.8 V		-	470	-	nA
		V_{DD} = 3.3 V		-	700	1 500	nA
		V_{DD} = 4.2 V		-	800	-	nA
		PWRMNG[2:0] = 111 (see Table 18); TSOFF = 1 (see Table 57); COF[2:0] = 000 (see Table 14)					
		V_{DD} = 1.8 V		-	560	-	nA
		V_{DD} = 3.3 V		-	850	-	nA
		V_{DD} = 4.2 V		-	1 050	-	nA
		PWRMNG[2:0] = 000 (see Table 18); TSOFF = 0 (see Table 57); COF[2:0] = 111 (see Table 14)					

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 78. Static characteristics...*continued*

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{DD} or V_{BAT} = 1.8 V	[3]	-	1 750	-	nA
		V_{DD} or V_{BAT} = 3.3 V	[3]	-	2 150	-	nA
		V_{DD} or V_{BAT} = 4.2 V	[3]	-	2 350	3 500	nA
		PWRMNG[2:0] = 000 (see Table 18); TSOFF = 0 (see Table 57); COF[2:0] = 000 (see Table 14)					
		V_{DD} or V_{BAT} = 1.8 V	[3]	-	1 840	-	nA
		V_{DD} or V_{BAT} = 3.3 V	[3]	-	2 300	-	nA
		V_{DD} or V_{BAT} = 4.2 V	[3]	-	2 600	-	nA
$I_{L(bat)}$	battery leakage current	V_{DD} is active supply; V_{BAT} = 3.0 V		-	50	100	nA
Power management							
$V_{th(sw)bat}$	battery switch threshold voltage			-	2.5	-	V
$V_{th(bat)low}$	low battery threshold voltage			-	2.5	-	V
		T_{amb} = 25 °C		2.25	-	2.85	V
Inputs[4]							
V_I	input voltage			-0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage			-	-	$0.25V_{DD}$	V
		T_{amb} = -20 °C to +85 °C; V_{DD} > 2.0 V		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}		-	0	-	µA
		post ESD event		-1	-	+1	µA
C_i	input capacitance		[5]	-	-	7	pF
Outputs							
V_O	output voltage	on pins CLKOUT, $\overline{INT}$, referring to external pull-up		-0.5	-	+5.5	V
		on pin BBS		1.8	-	4.2	V
		on pin SDO		-0.5	-	V_{DD} + 0.5	V
V_{OH}	HIGH output voltage	on pin SDO		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW output voltage	on pins CLKOUT, $\overline{INT}$, and SDO		V_{SS}	-	$0.2V_{DD}$	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V					
		on pin SDA/$\overline{CE}$	[6]	3	17	-	mA
		on all other outputs		1.0	-	-	mA

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

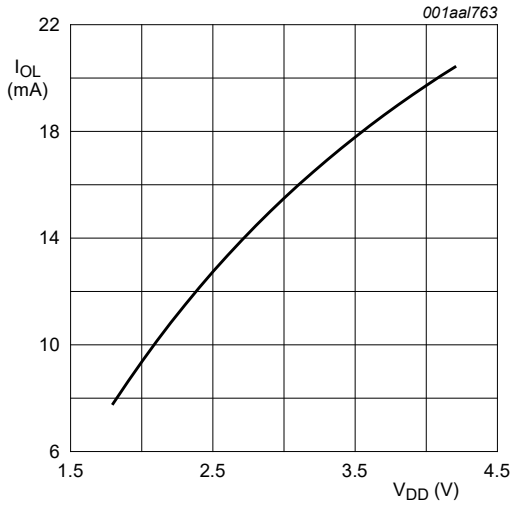
Table 78. Static characteristics...*continued*

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OH}	HIGH-level output current	output source current; on pin SDO; V_{OH} = 3.8 V; V_{DD} = 4.2 V		1.0	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}		-	0	-	µA
		post ESD event		-1	-	+1	µA

[1] For reliable oscillator start-up at power-on: $V_{DD(po)min} = V_{DD(min)} + 0.3$ V.
[2] Timer source clock = $^1/_{60}$ Hz, level of pins SDA/CE, SDI, and SCL is V_{DD} or V_{SS}.
[3] When the device is supplied by the V_{BAT} pin instead of the V_{DD} pin, the current values for I_{BAT} are as specified for I_{DD} under the same conditions.
[4] The I^2C-bus and SPI-bus interfaces of PCF2129 are 5 V tolerant.
[5] Tested on sample basis.
[6] For further information, see Figure 40.

12.1 Current consumption characteristics, typical

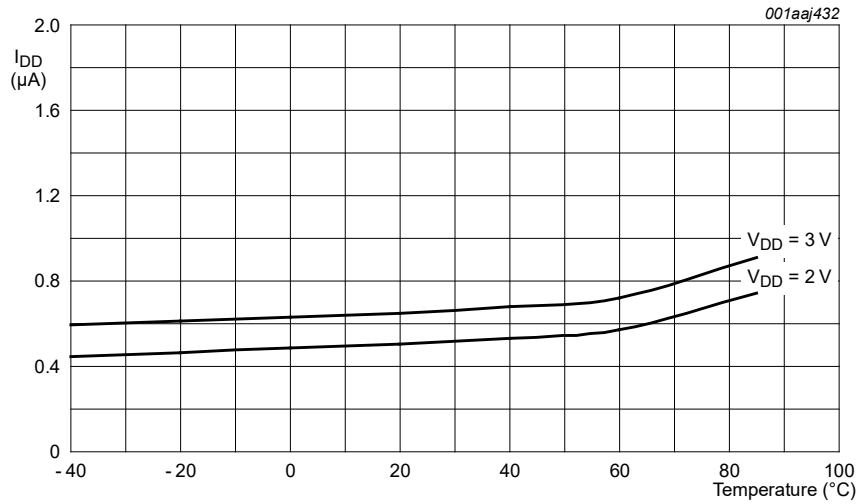


Typical value; V_{OL} = 0.4 V.

Figure 40. I_{OL} on pin SDA/CE

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

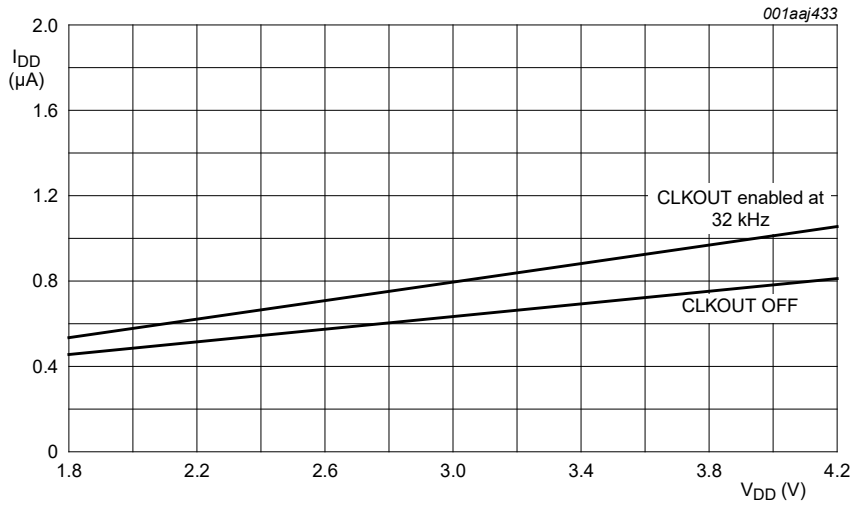


CLKOUT disabled; PWRMNG[2:0] = 111; TSOFF = 1; $\overline{TS}$ input floating.

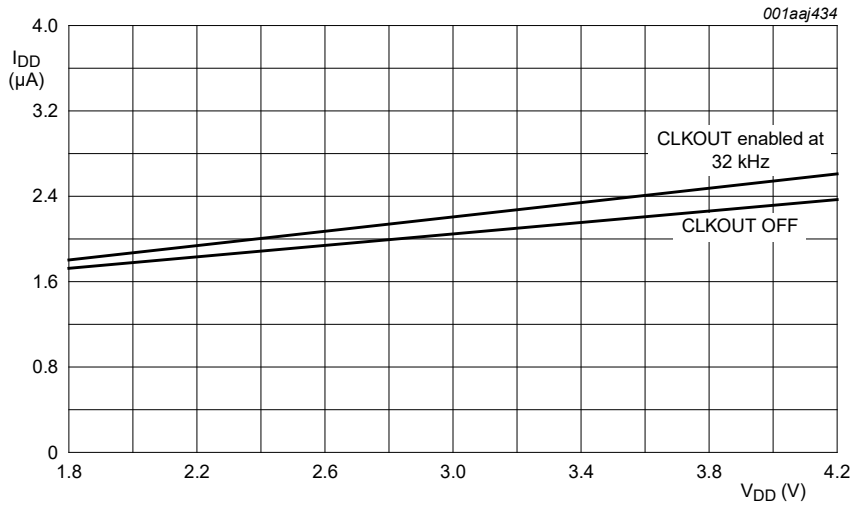
Figure 41. I_{DD} as a function of temperature

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



a. PWRMNG[2:0] = 111; TSOFF = 1; T_{amb} = 25 °C; $\overline{TS}$ input floating

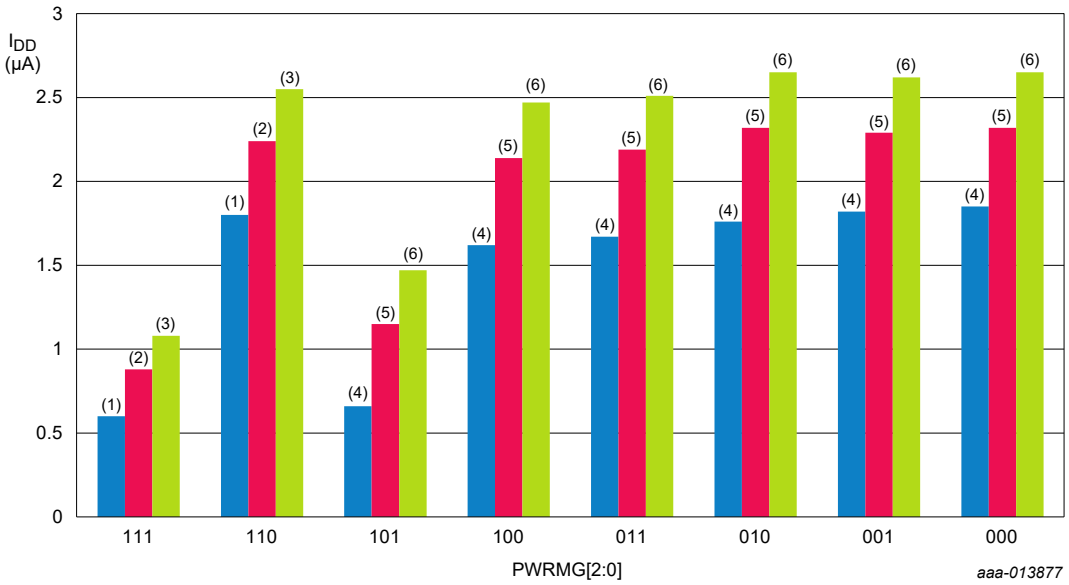


b. PWRMNG[2:0] = 000; TSOFF = 0; T_{amb} = 25 °C; $\overline{TS}$ input floating

Figure 42. I_{DD} as a function of V_{DD}

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



Interface inactive; T_{amb} = 25 °C; V_{BAT} = 0 V; default configuration.
Description of the PWRMNG[2:0] settings, see Table 18.

1. V_{DD} = 1.8 V.
2. V_{DD} = 3.3 V.
3. V_{DD} = 4.2 V.
4. V_{DD} or V_{BAT} = 1.8 V.
5. V_{DD} or V_{BAT} = 3.3 V.
6. V_{DD} or V_{BAT} = 4.2 V.

Figure 43. Typical I_{DD} as a function of the power management settings

12.2 Frequency characteristics

Table 79. Frequency characteristics

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_o	output frequency	on pin CLKOUT; V_{DD} or V_{BAT} = 3.3 V; COF[2:0] = 000; AO[3:0] = 1000		-	32.768	-	kHz
Δf/f	frequency stability	V_{DD} or V_{BAT} = 3.3 V					
		PCF2129AT					
		T_{amb} = -15 °C to +60 °C	[1][2]	-	±3	±5	ppm
		T_{amb} = -25 °C to -15 °C and T_{amb} = +60 °C to +65 °C	[1][2]	-	±5	±10	ppm
		PCF2129T					
		T_{amb} = -30 °C to +80 °C	[1][2]	-	±3	±8	ppm
		T_{amb} = -40 °C to -30 °C and T_{amb} = +80 °C to +85 °C	[1][2]	-	±5	±15	ppm

All information provided in this document is subject to legal disclaimers.

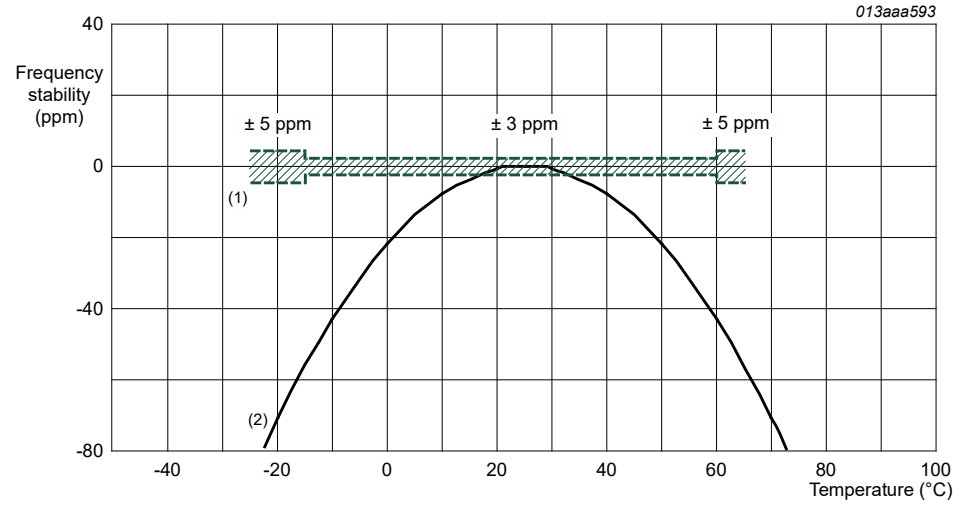
© 2022 NXP B.V. All rights reserved.

Table 79. Frequency characteristics...*continued*

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	crystal aging					
		PCF2129AT					
		first year; V_{DD} or V_{BAT} = 3.3 V	[3]	-	-	±3	ppm
		PCF2129T					
		first year	[3]	-	-	±3	ppm
		ten years		-	-	±8	ppm
Δf/ΔV	frequency variation with voltage	on pin CLKOUT		-	±1	-	ppm/V

[1] ±1 ppm corresponds to a time deviation of ±0.0864 seconds per day.
[2] Only valid if CLKOUT frequencies are not equal to 32.768 kHz or if CLKOUT is disabled.
[3] Not production tested. Effects of reflow soldering are included (see [1]).

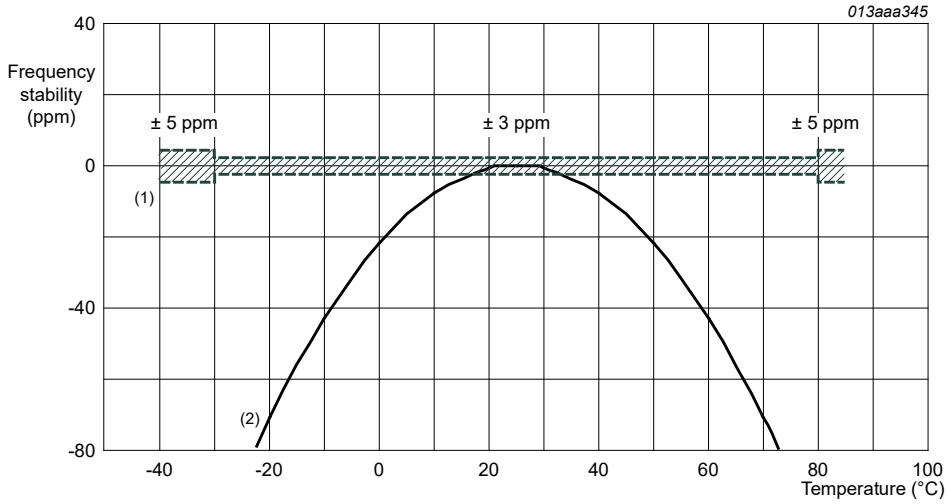


1. Typical temperature compensated frequency response.
2. Uncompensated typical tuning-fork crystal frequency.

Figure 44. Typical characteristic of frequency with respect to temperature of PCF2129AT

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.



1. Typical temperature compensated frequency response.
2. Uncompensated typical tuning-fork crystal frequency.

Figure 45. Typical characteristic of frequency with respect to temperature of PCF2129T

13 Dynamic characteristics

13.1 SPI-bus timing characteristics

Table 80. SPI-bus characteristics

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} (see Figure 46).

Symbol	Parameter	Conditions		V_{DD} = 1.8 V		V_{DD} = 4.2 V		Unit
				Min	Max	Min	Max	
Pin SCL								
$f_{clk(SCL)}$	SCL clock frequency			-	2.0	-	6.5	MHz
t_{SCL}	SCL time			800	-	140	-	ns
$t_{clk(H)}$	clock HIGH time			100	-	70	-	ns
$t_{clk(L)}$	clock LOW time			400	-	70	-	ns
t_r	rise time	for SCL signal		-	100	-	100	ns
t_f	fall time	for SCL signal		-	100	-	100	ns
Pin SDA/$\overline{CE}$								
$t_{su(CE_N)}$	CE_N set-up time			60	-	30	-	ns
$t_{h(CE_N)}$	CE_N hold time			40	-	25	-	ns
$t_{rec(CE_N)}$	CE_N recovery time			100	-	30	-	ns
$t_{w(CE_N)}$	CE_N pulse width			-	0.99	-	0.99	s
Pin SDI								
t_{su}	set-up time	set-up time for SDI data		70	-	20	-	ns

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 80. SPI-bus characteristics...*continued*

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} (see Figure 46).

Symbol	Parameter	Conditions		V_{DD} = 1.8 V		V_{DD} = 4.2 V		Unit
				Min	Max	Min	Max	
t_h	hold time	hold time for SDI data		70	-	20	-	ns
Pin SDO								
$t_{d(R)SDO}$	SDO read delay time	C_L = 50 pF		-	225	-	55	ns
$t_{dis(SDO)}$	SDO disable time		[1]	-	90	-	25	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict		0	-	0	-	ns

[1] No load value; bus is held up by bus capacitance; use RC time constant with application values.

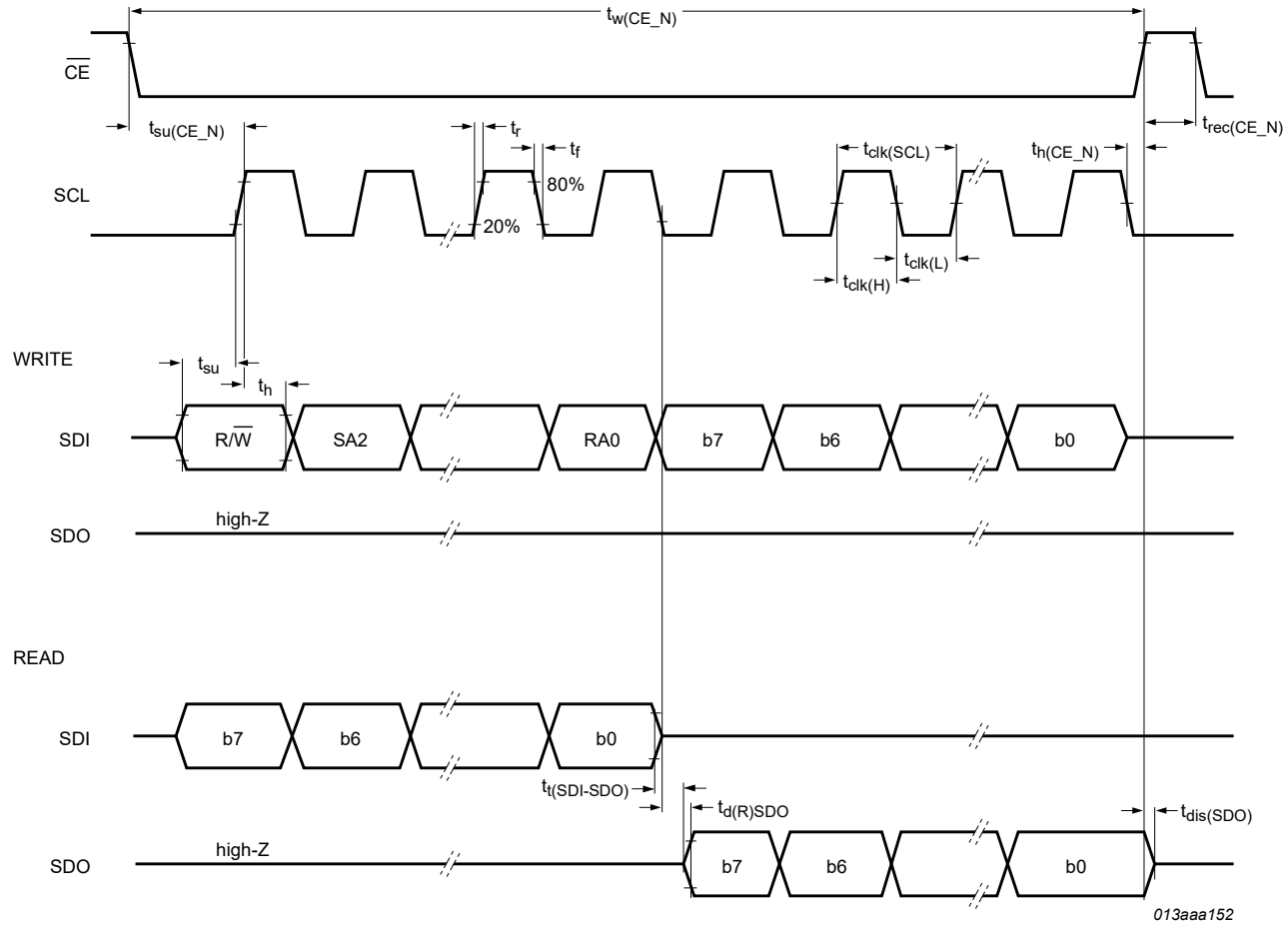


Figure 46. SPI-bus timing

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

13.2 I²C-bus timing characteristics

Table 81. I²C-bus characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 47).

Symbol	Parameter		Standard mode		Fast-mode (Fm)		Unit
			Min	Max	Min	Max	
Pin SCL							
f_{SCL}	SCL clock frequency	[1]	0	100	0	400	kHz
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
Pin SDA/$\overline{CE}$							
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
Pins SCL and SDA/$\overline{CE}$							
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals	[2][3][4]	-	1 000	$20 + 0.1C_b$	300	ns
t_f	fall time of both SDA and SCL signals	[2][3][4]	-	300	$20 + 0.1C_b$	300	ns
$t_{VD;ACK}$	data valid acknowledge time	[5]	0.1	3.45	0.1	0.9	µs
$t_{VD;DAT}$	data valid time	[6]	300	-	75	-	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.

[2] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[3] C_b is the total capacitance of one bus line in pF.

[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA/$\overline{CE}$ pin, the SCL pin, and the SDA/SCL bus lines without exceeding the maximum t_f.

[5] $t_{VD;ACK}$ is the time of the acknowledgement signal from SCL LOW to SDA (out) LOW.

[6] $t_{VD;DAT}$ is the minimum time for valid SDA (out) data following SCL LOW.

[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

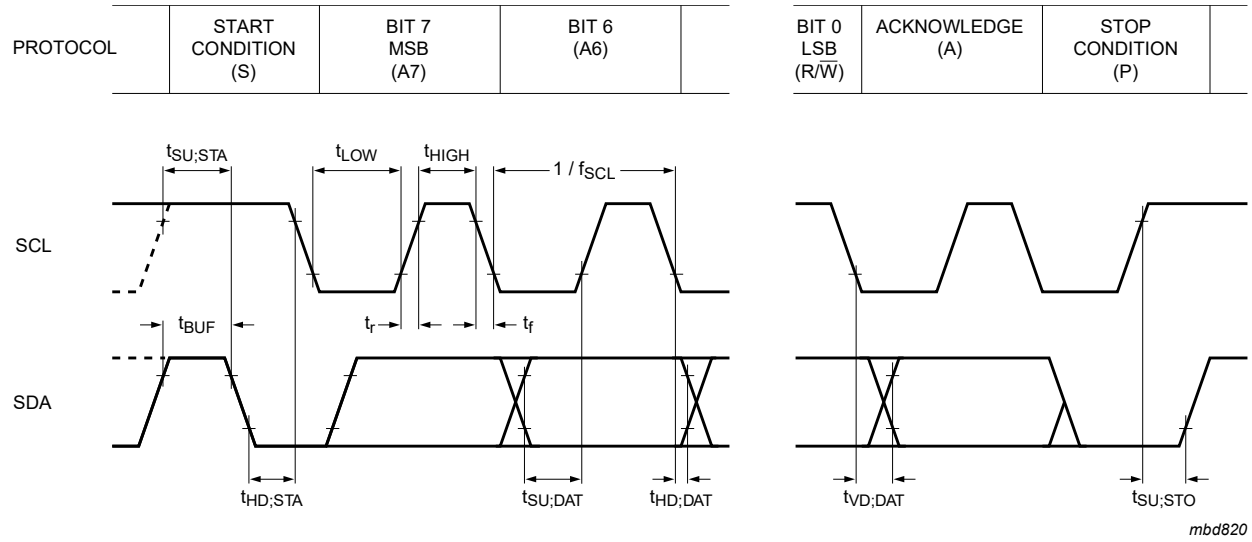
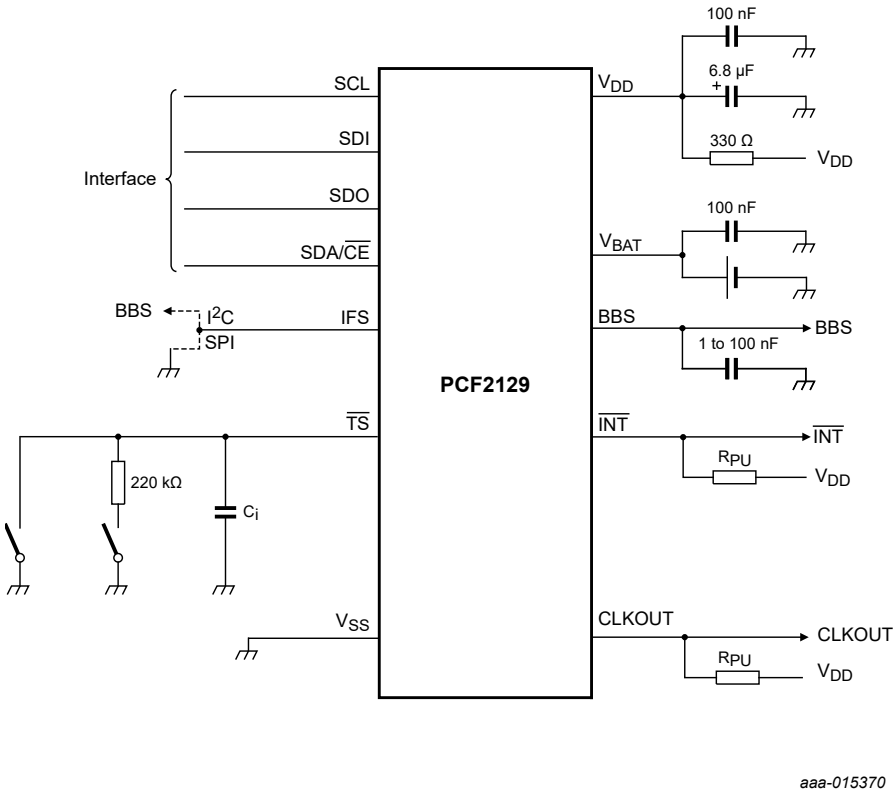


Figure 47. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

14 Application information



C_i: In case mechanical switches are used, a capacitor of 1 nF is recommended.
R_{PU}: For example, 10 kΩ.

Figure 48. General application diagram

For information about application configuration, see [1].

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

15 Test information

15.1 Quality information

UL Component Recognition

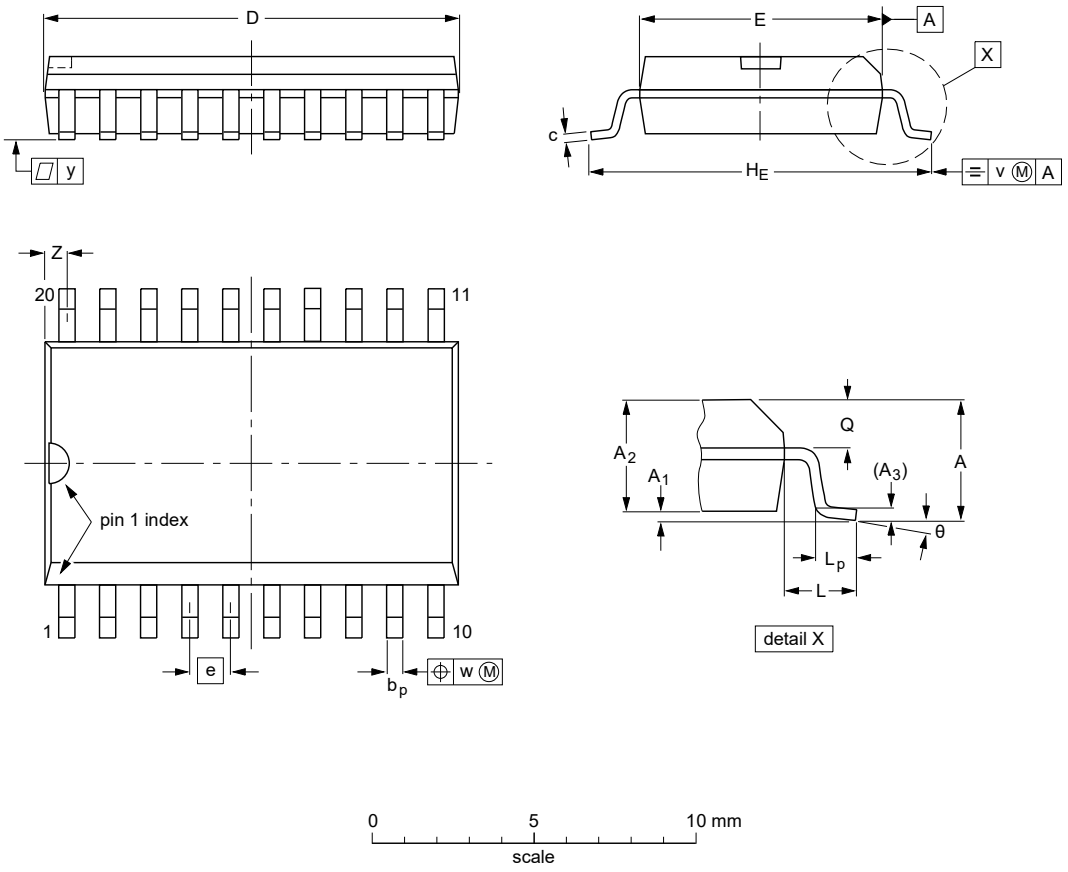
This (component or material) is Recognized by UL. Representative samples of this component have been evaluated by UL and meet applicable UL requirements.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

16 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

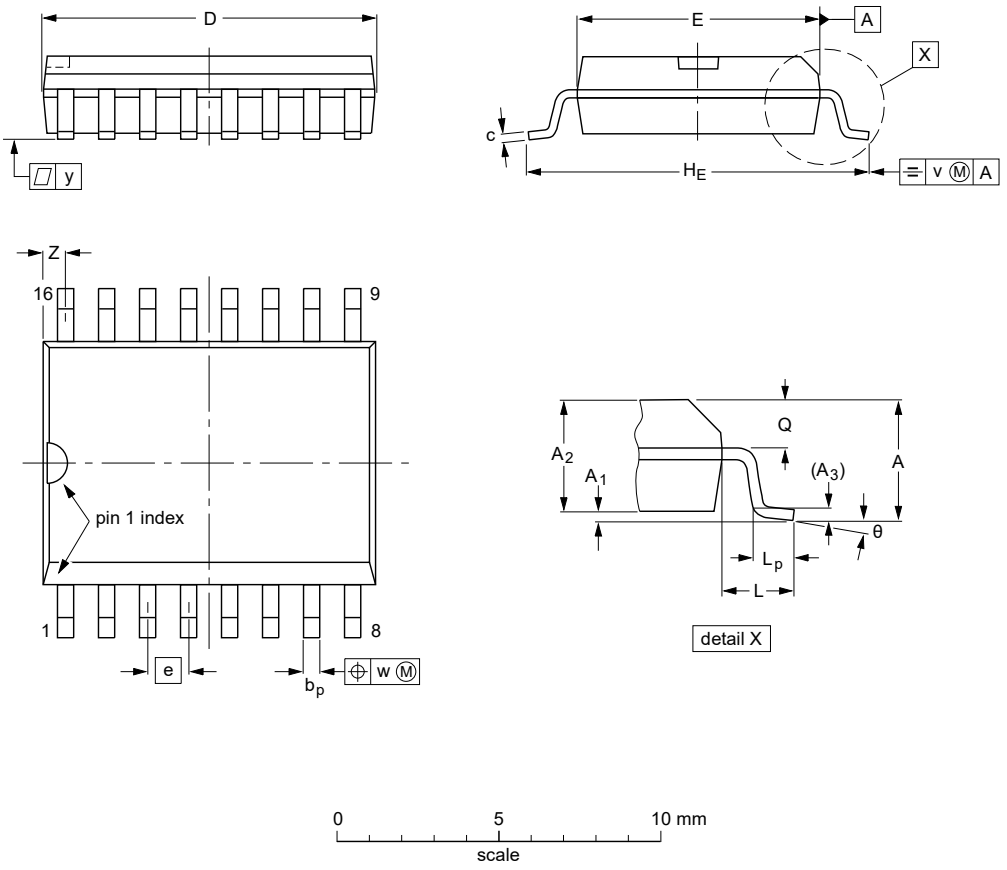
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Figure 49. Package outline SOT163-1 (SO20) of PCF2129AT

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Figure 50. Package outline SOT162-1 (SO16) of PCF2129T

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

17 Packing information

17.1 Tape and reel information

For tape and reel packing information, see

- [5] for the PCF2129T.
- [6] for the PCF2129AT.

18 Soldering

For information about soldering, see [1].

18.1 Footprint information

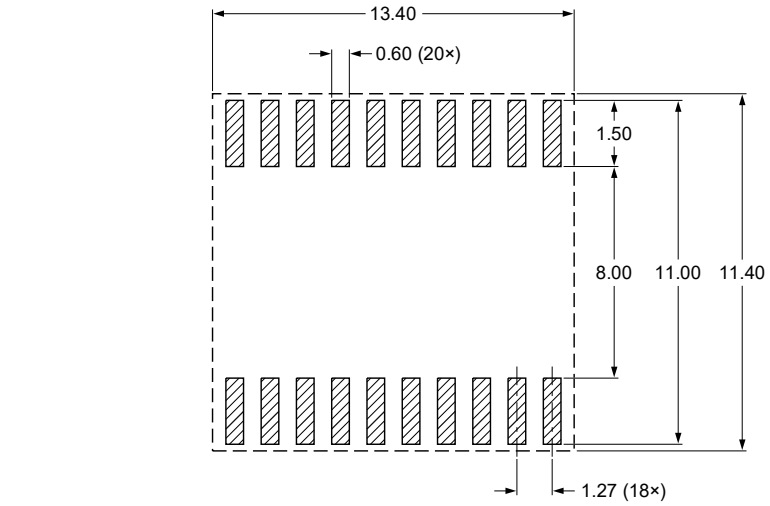
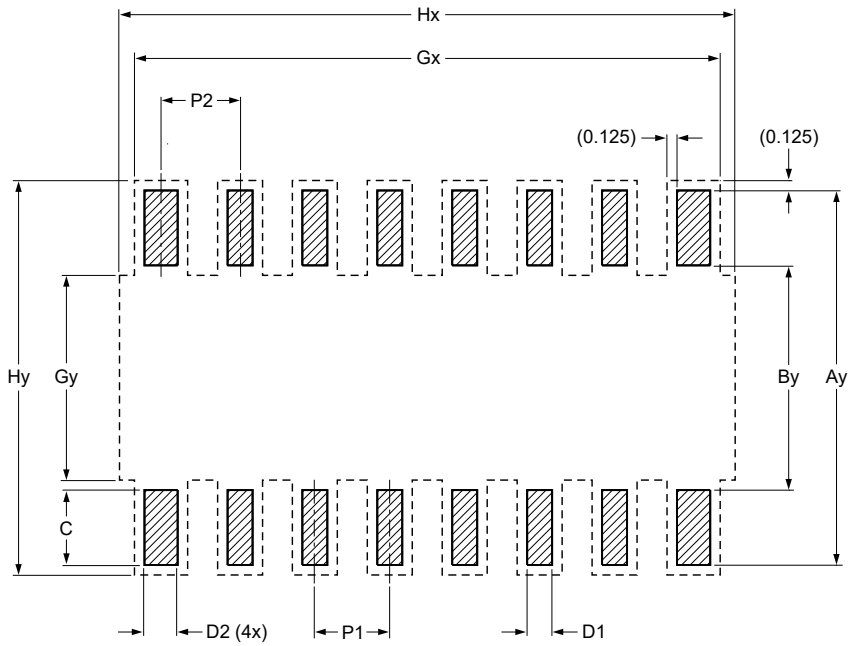


Figure 51. Footprint information for reflow soldering of SOT163-1 (SO20) of PCF2129AT

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Footprint information for reflow soldering of SO16 package **SOT162-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	11.200	6.400	2.400	0.700	0.800	10.040	8.600	11.900	11.450

sot162-1_fr

Figure 52. Footprint information for reflow soldering of SOT162-1 (SO16) of PCF2129T

19 Appendix

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

19.1 Real-Time Clock selection

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 82. Selection of Real-Time Clocks

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF8563	X	1	I^2C	250	-	-	-	-	SO8, TSSOP8, HVSON10
PCF8564A	X	1	I^2C	250	-	-	-	integrated oscillator caps	WLCSP
PCA8565	X	1	I^2C	600	-	-	grade 1	high robustness, T_{amb}= -40 °C to 125 °C	TSSOP8, HVSON10
PCA8565A	X	1	I^2C	600	-	-	-	integrated oscillator caps, T_{amb}= -40 °C to 125 °C	WLCSP
PCF85063	-	1	I^2C	220	-	-	-	basic functions only, no alarm	HXSON8
PCF85063A	X	1	I^2C	220	-	-	-	tiny package	SO8, DFN2626-10
PCF85063B	X	1	SPI	220	-	-	-	tiny package	DFN2626-10
PCF85263A	X	2	I^2C	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$ s	SO8, TSSOP10, TSSOP8, DFN2626-10
PCF85263B	X	2	SPI	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s	TSSOP10, DFN2626-10
PCF85363A	X	2	I^2C	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10
PCF85363B	X	2	SPI	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10
PCF8523	X	2	I^2C	150	X	-	-	lowest power 150 nA in operation, FM+ 1 MHz	SO8, HVSON8, TSSOP14, WLCSP
PCF2123	X	1	SPI	100	-	-	-	lowest power 100 nA in operation	TSSOP14, HVQFN16
PCF2127	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated, 512 Byte RAM	SO16
PCF2127A	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated, 512 Byte RAM	SO20

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Table 82. Selection of Real-Time Clocks*...continued*

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF2129	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated	SO16
PCF2129A	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated	SO20
PCA2129	X	1	I^2C and SPI	500	X	X	grade 3	temperature compensated, quartz built in, calibrated	SO16
PCA21125	X	1	SPI	820	-	-	grade 1	high robustness, T_{amb}= -40 °C to 125 °C	TSSOP14

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

20 Abbreviations

Table 83. Abbreviations

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
GPS	Global Positioning System
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MCU	Microcontroller Unit
MM	Machine Model
MSB	Most Significant Bit
PM	Post Meridiem
POR	Power-On Reset
PORO	Power-On Reset Override
PPM	Parts Per Million
RC	Resistance-Capacitance
RTC	Real-Time Clock
SCL	Serial CLock line
SDA	Serial DAta line
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Xtal Oscillator
Xtal	crystal

21 References

[1] AN11186 Application and soldering information for the PCA2129 and PCF2129 TCXO RTC

[2] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[3] JESD22-C101 Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[4] JESD78 IC Latch-Up Test

[5] SOT162-1_518 SO16; Reel pack; SMD, 13", packing information

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

[6] SOT163-1_518 SO20; Reel pack; SMD, 13", packing information
[7] UM10204 I^2C-bus specification and user manual
[8] UM10569 Store and transport requirements

22 Revision history

Table 84. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2129 v.8	20220718	Product data sheet	-	PCF2129 v.7
Modifications:	• Added UL certification information • Updated layout of Section 4			
PCF2129 v.7	20141219	Product data sheet	-	PCF2129AT v.6 PCF2129T v.4
PCF2129AT				
PCF2127AT v.6	20130711	Product data sheet	-	PCF2127AT v.5
PCF2129AT v.5	20130212	Product data sheet	-	PCF2129AT v.4
PCF2129AT v.4	20121107	Product data sheet	-	PCF2129AT v.3
PCF2129AT v.3	20121004	Product data sheet	-	PCF2129AT v.2
PCF2129AT v.2	20100507	Product data sheet	-	PCF2129AT v.1
PCF2129AT v.1	20100113	Product data sheet	-	-
PCF2129T				
PCF2129T v.4	20130711	Product data sheet	-	PCF2129T v.3
PCF2129T v.3	20130212	Product data sheet	-	PCF2129T v.2
PCF2129T v.2	20121025	Product data sheet	-	PCF2129T v.1
PCF2129T v.1	20120618	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

23 Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

23.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

23.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

23.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Tables

Tab. 1. Ordering information 2
Tab. 2. Ordering options 2
Tab. 3. Pin description of PCF2129 5
Tab. 4. Register overview 7
Tab. 5. Control_1 - control and status register 1 (address 00h) bit allocation 9
Tab. 6. Control_1 - control and status register 1 (address 00h) bit description 9
Tab. 7. Control_2 - control and status register 2 (address 01h) bit allocation 10
Tab. 8. Control_2 - control and status register 2 (address 01h) bit description 10
Tab. 9. Control_3 - control and status register 3 (address 02h) bit allocation 10
Tab. 10. Control_3 - control and status register 3 (address 02h) bit description 11
Tab. 11. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit allocation 11
Tab. 12. CLKOUT_ctl - CLKOUT control register (address 0Fh) bit description 11
Tab. 13. Temperature measurement period 12
Tab. 14. CLKOUT frequency selection 12
Tab. 15. Aging_offset - crystal aging offset register (address 19h) bit allocation 13
Tab. 16. Aging_offset - crystal aging offset register (address 19h) bit description 13
Tab. 17. Frequency correction at 25 °C, typical 13
Tab. 18. Power management control bit description 15
Tab. 19. Output pin BBS 18
Tab. 20. Seconds - seconds and clock integrity register (address 03h) bit allocation 22
Tab. 21. Seconds - seconds and clock integrity register (address 03h) bit description 22
Tab. 22. Seconds coded in BCD format 22
Tab. 23. Minutes - minutes register (address 04h) bit allocation 23
Tab. 24. Minutes - minutes register (address 04h) bit description 23
Tab. 25. Hours - hours register (address 05h) bit allocation 23
Tab. 26. Hours - hours register (address 05h) bit description 24
Tab. 27. Days - days register (address 06h) bit allocation 24
Tab. 28. Days - days register (address 06h) bit description 24
Tab. 29. Weekdays - weekdays register (address 07h) bit allocation 24
Tab. 30. Weekdays - weekdays register (address 07h) bit description 25
Tab. 31. Weekday assignments 25
Tab. 32. Months - months register (address 08h) bit allocation 25
Tab. 33. Months - months register (address 08h) bit description 25
Tab. 34. Month assignments in BCD format 26
Tab. 35. Years - years register (address 09h) bit allocation 26
Tab. 36. Years - years register (address 09h) bit description 26
Tab. 37. Second_alarm - second alarm register (address 0Ah) bit allocation 28
Tab. 38. Second_alarm - second alarm register (address 0Ah) bit description 28
Tab. 39. Minute_alarm - minute alarm register (address 0Bh) bit allocation 29
Tab. 40. Minute_alarm - minute alarm register (address 0Bh) bit description 29
Tab. 41. Hour_alarm - hour alarm register (address 0Ch) bit allocation 29
Tab. 42. Hour_alarm - hour alarm register (address 0Ch) bit description 29
Tab. 43. Day_alarm - day alarm register (address 0Dh) bit allocation 30
Tab. 44. Day_alarm - day alarm register (address 0Dh) bit description 30
Tab. 45. Weekday_alarm - weekday alarm register (address 0Eh) bit allocation 30
Tab. 46. Weekday_alarm - weekday alarm register (address 0Eh) bit description 31
Tab. 47. Watchdg_tim_ctl - watchdog timer control register (address 10h) bit allocation 31
Tab. 48. Watchdg_tim_ctl - watchdog timer control register (address 10h) bit description 32
Tab. 49. Watchdg_tim_val - watchdog timer value register (address 11h) bit allocation 32
Tab. 50. Watchdg_tim_val - watchdog timer value register (address 11h) bit description 32
Tab. 51. Programmable watchdog timer 32
Tab. 52. Flag location in register Control_2 34
Tab. 53. Example values in register Control_2 34
Tab. 54. Example to clear only AF (bit 4) 34
Tab. 55. Example to clear only MSF (bit 7) 35
Tab. 56. Timestp_ctl - timestamp control register (address 12h) bit allocation 36
Tab. 57. Timestp_ctl - timestamp control register (address 12h) bit description 36
Tab. 58. Sec_timestp - second timestamp register (address 13h) bit allocation 37
Tab. 59. Sec_timestp - second timestamp register (address 13h) bit description 37
Tab. 60. Min_timestp - minute timestamp register (address 14h) bit allocation 37
Tab. 61. Min_timestp - minute timestamp register (address 14h) bit description 37
Tab. 62. Hour_timestp - hour timestamp register (address 15h) bit allocation 37
Tab. 63. Hour_timestp - hour timestamp register (address 15h) bit description 38
Tab. 64. Day_timestp - day timestamp register (address 16h) bit allocation 38

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Tab. 65. Day_timestp - day timestamp register (address 16h) bit description 38
Tab. 66. Mon_timestp - month timestamp register (address 17h) bit allocation 39
Tab. 67. Mon_timestp - month timestamp register (address 17h) bit description 39
Tab. 68. Year_timestp - year timestamp register (address 18h) bit allocation 39
Tab. 69. Year_timestp - year timestamp register (address 18h) bit description 39
Tab. 70. Battery switch-over and timestamp 39
Tab. 71. Effect of bits MI and SI on pin INT and bit MSF 41
Tab. 72. First increment of time circuits after stop release 45
Tab. 73. Interface selection input pin IFS 46
Tab. 74. Serial interface 47
Tab. 75. Command byte definition 48
Tab. 76. I2C slave address byte 51
Tab. 77. Limiting values 53
Tab. 78. Static characteristics 54
Tab. 79. Frequency characteristics 59
Tab. 80. SPI-bus characteristics 61
Tab. 81. I2C-bus characteristics 63
Tab. 82. Selection of Real-Time Clocks 71
Tab. 83. Abbreviations 73
Tab. 84. Revision history 74

Figures

Fig. 1. Block diagram of PCF2129 3
Fig. 2. Pin configuration for PCF2129AT (SO20) 4
Fig. 3. Pin configuration for PCF2129T (SO16) 4
Fig. 4. Position of the stubs from the package assembly process 4
Fig. 5. Handling address registers 6
Fig. 6. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled) 16
Fig. 7. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled) 17
Fig. 8. Battery switch-over circuit, simplified block diagram 17
Fig. 9. Battery low detection behavior with bit BLIE set logic 1 (enabled) 18
Fig. 10. Typical driving capability of VBBS: (VBBS - VDD) with respect to the output load current IBBS 19
Fig. 11. Power failure event due to battery discharge: reset occurs 20
Fig. 12. Dependency between POR and oscillator 21
Fig. 13. Power-On Reset (POR) system 21
Fig. 14. Power-On Reset Override (PORO) sequence, valid for both I2C-bus and SPI-bus 22
Fig. 15. Data flow of the time function 27
Fig. 16. Access time for read/write operations 27
Fig. 17. Alarm function block diagram 28
Fig. 18. Alarm flag timing diagram 31
Fig. 19. WD_CD set logic 1: watchdog activates an interrupt when timed out 33
Fig. 20. Timestamp detection with two push-buttons on the TS pin (for example, for tamper detection) 35
Fig. 21. Interrupt block diagram 41
Fig. 22. INT example for SI and MI when TI_TP is logic 1 42
Fig. 23. INT example for SI and MI when TI_TP is logic 0 42
Fig. 24. Example of shortening the INT pulse by clearing the MSF flag 43
Fig. 25. AF timing diagram 44
Fig. 26. STOP bit functional diagram 45
Fig. 27. STOP bit release timing 46
Fig. 28. Interface selection 47
Fig. 29. SDI, SDO configurations 47
Fig. 30. Data transfer overview 48
Fig. 31. SPI-bus write example 49
Fig. 32. SPI-bus read example 49
Fig. 33. Bit transfer 50
Fig. 34. Definition of START and STOP conditions 50
Fig. 35. System configuration 50
Fig. 36. Acknowledgement on the I2C-bus 51
Fig. 37. Bus protocol, writing to registers 52
Fig. 38. Bus protocol, reading from registers 52
Fig. 39. Device diode protection diagram of PCF2129 53
Fig. 40. IOL on pin SDA/CE 56
Fig. 41. IDD as a function of temperature 57
Fig. 42. IDD as a function of VDD 58
Fig. 43. Typical IDD as a function of the power management settings 59
Fig. 44. Typical characteristic of frequency with respect to temperature of PCF2129AT 60
Fig. 45. Typical characteristic of frequency with respect to temperature of PCF2129T 61
Fig. 46. SPI-bus timing 62
Fig. 47. I2C-bus timing diagram; rise and fall times refer to 30 % and 70 % 64
Fig. 48. General application diagram 64
Fig. 49. Package outline SOT163-1 (SO20) of PCF2129AT 66
Fig. 50. Package outline SOT162-1 (SO16) of PCF2129T 67
Fig. 51. Footprint information for reflow soldering of SOT163-1 (SO20) of PCF2129AT 68
Fig. 52. Footprint information for reflow soldering of SOT162-1 (SO16) of PCF2129T 69

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
4.1 Ordering options 2
5 Block diagram 3
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 5
7 Functional description 5
7.1 Register overview 6
7.2 Control registers 9
7.2.1 Register Control_1 9
7.2.2 Register Control_2 10
7.2.3 Register Control_3 10
7.3 Register CLKOUT_ctl 11
7.3.1 Temperature compensated crystal oscillator 11
7.3.1.1 Temperature measurement 12
7.3.2 OTP refresh 12
7.3.3 Clock output 12
7.4 Register Aging_offset 13
7.4.1 Crystal aging correction 13
7.5 Power management functions 14
7.5.1 Battery switch-over function 15
7.5.1.1 Standard mode 16
7.5.1.2 Direct switching mode 16
7.5.1.3 Battery switch-over disabled: only one power supply (VDD) 17
7.5.1.4 Battery switch-over architecture 17
7.5.2 Battery low detection function 17
7.5.3 Battery backup supply 18
7.6 Oscillator stop detection function 19
7.7 Reset function 20
7.7.1 Power-On Reset (POR) 20
7.7.2 Power-On Reset Override (PORO) 21
7.8 Time and date function 22
7.8.1 Register Seconds 22
7.8.2 Register Minutes 23
7.8.3 Register Hours 23
7.8.4 Register Days 24
7.8.5 Register Weekdays 24
7.8.6 Register Months 25
7.8.7 Register Years 26
7.8.8 Setting and reading the time 26
7.9 Alarm function 27
7.9.1 Register Second_alarm 28
7.9.2 Register Minute_alarm 29
7.9.3 Register Hour_alarm 29
7.9.4 Register Day_alarm 30
7.9.5 Register Weekday_alarm 30
7.9.6 Alarm flag 31
7.10 Timer functions 31
7.10.1 Register Watchdg_tim_ctl 31
7.10.2 Register Watchdg_tim_val 32
7.10.3 Watchdog timer function 33
7.10.4 Pre-defined timers: second and minute interrupt 34
7.10.5 Clearing flags 34
7.11 Timestamp function 35
7.11.1 Timestamp flag 35
7.11.2 Timestamp mode 36
7.11.3 Timestamp registers 36
7.11.3.1 Register Timestp_ctl 36
7.11.3.2 Register Sec_timestp 37
7.11.3.3 Register Min_timestp 37
7.11.3.4 Register Hour_timestp 37
7.11.3.5 Register Day_timestp 38
7.11.3.6 Register Mon_timestp 39
7.11.3.7 Register Year_timestp 39
7.11.4 Dependency between Battery switch-over and timestamp 39
7.12 Interrupt output, INT 40
7.12.1 Minute and second interrupts 41
7.12.2 INT pulse shortening 43
7.12.3 Watchdog timer interrupts 43
7.12.4 Alarm interrupts 43
7.12.5 Timestamp interrupts 44
7.12.6 Battery switch-over interrupts 44
7.12.7 Battery low detection interrupts 44
7.13 External clock test mode 44
7.14 STOP bit function 45
8 Interfaces 46
8.1 SPI-bus interface 47
8.1.1 Data transmission 48
8.2 I2C-bus interface 49
8.2.1 Bit transfer 49
8.2.2 START and STOP conditions 50
8.2.3 System configuration 50
8.2.4 Acknowledge 50
8.2.5 I2C-bus protocol 51
8.3 Bus communication and battery backup operation 52
9 Internal circuitry 53
10 Safety notes 53
11 Limiting values 53
12 Static characteristics 54
12.1 Current consumption characteristics, typical 56
12.2 Frequency characteristics 59
13 Dynamic characteristics 61
13.1 SPI-bus timing characteristics 61
13.2 I2C-bus timing characteristics 63
14 Application information 64
15 Test information 65
15.1 Quality information 65
16 Package outline 66
17 Packing information 68
17.1 Tape and reel information 68
18 Soldering 68
18.1 Footprint information 68
19 Appendix 69
19.1 Real-Time Clock selection 70

All information provided in this document is subject to legal disclaimers.

© 2022 NXP B.V. All rights reserved.

20 Abbreviations 73
21 References 73
22 Revision history 74
23 Legal information 75

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2022 NXP B.V. All rights reserved.

For more information, please visit: http://www.nxp.com

Date of release: 18 July 2022
Document identifier: PCF2129

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View PCF2129T/2,518 on WIN SOURCE
- NXP / Nexperia Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management