



# XMC4100 / XMC4200

Microcontroller Series  
for Industrial Applications

XMC4000 Family

ARM<sup>®</sup> Cortex<sup>®</sup>-M4  
32-bit processor core

Data Sheet

V1.5 2023-04

Microcontrollers

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**XMC4[12]00 Data Sheet**

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<b>86</b>	Deleted package details: PG-LQFP-64-19 and PG-VQFN-48-53. Added package details: PG-TQFP-64-21.
<b>88</b>	Deleted Table 56 and 57.
<b>89</b>	Added package diagram: PG-TQFP-64-21. Deleted package diagram: PG-LQFP-64-19.

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## **About this Document**

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[12]00 series devices.

The document describes the characteristics of a superset of the XMC4[12]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[12]00 throughout this manual.

### **XMC4000 Family User Documentation**

The set of user documentation includes:

- **Reference Manual**
  - describes the functionality of the superset of devices.
- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

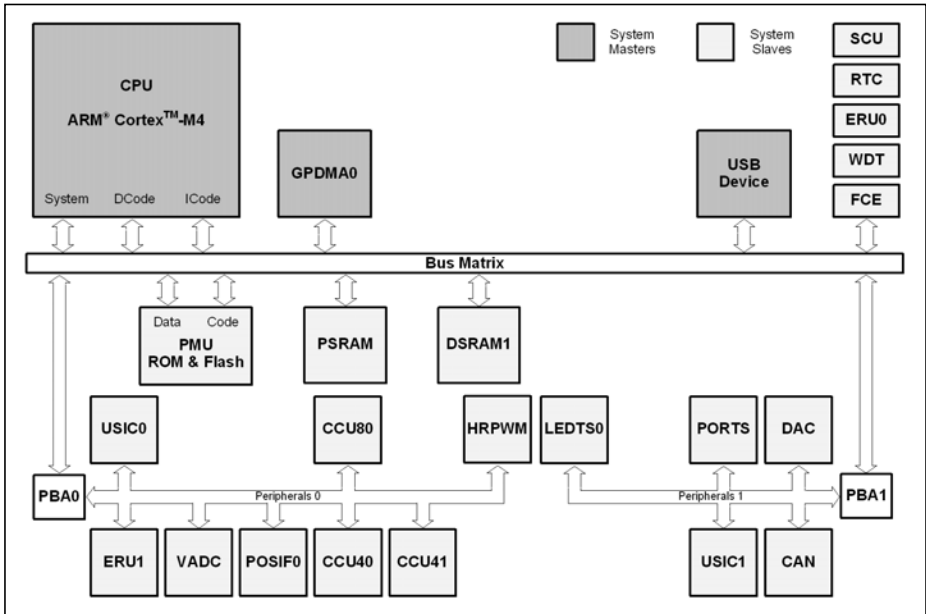
***Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.***

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc4000> to get access to the latest versions of those documents.

## 1 Summary of Features

The XMC4[12]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.



**Figure 1 System Block Diagram**

### CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

**On-Chip Memories**

- 16 KB on-chip boot ROM
- up to 16 KB on-chip high-speed program memory
- up to 24 KB on-chip high speed data memory
- up to 256 KB on-chip Flash Memory with 1 KB instruction cache

**Communication Peripherals**

- Universal Serial Bus, USB 2.0 device, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects (MO), data rate up to 1 MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

**Analog Frontend Peripherals**

- Two Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

**Industrial Control Peripherals**

- Two Capture/Compare Units 4 (CCU4) for use as general purpose timers
- One Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four High Resolution PWM (HRPWM) channels
- One Position Interface (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

**Input/Output Lines**

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

**On-Chip Debug Support**

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

## 1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP, TQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4[12]00 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4100 and XMC4200 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC4[12]00** is used for all derivatives throughout this document.

## 1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

**Table 1 Synopsis of XMC4[12]00 Device Types**

Derivative <sup>1)</sup>	Package	Flash Kbytes	SRAM Kbytes
XMC4200-F64x256	PG-yQFP-64 <sup>2)</sup>	256	40
XMC4200-Q48x256	PG-VQFN-48	256	40
XMC4100-F64x128	PG-yQFP-64 <sup>2)</sup>	128	20
XMC4100-Q48x128	PG-VQFN-48	128	20
XMC4104-F64x64	PG-yQFP-64 <sup>2)</sup>	64	20
XMC4104-Q48x64	PG-VQFN-48	64	20
XMC4104-F64x128	PG-yQFP-64 <sup>2)</sup>	128	20
XMC4104-Q48x128	PG-VQFN-48	128	20
XMC4108-F64x64	PG-yQFP-64 <sup>2)</sup>	64	20
XMC4108-Q48x64	PG-VQFN-48	64	20

1) x is a placeholder for the supported temperature range.

2) y is a placeholder for the QFP package variant, LQFP or TQFP depending on the stepping, see [Section 1.3](#).

### 1.3 Package Variants

Different markings of the XMC4[12]00 use different package variants. Details of those packages are given in the **“Package Parameters”** section of the Data Sheet.

**Table 2 XMC4[12]00 Package Variants**

Package Variant	Marking	Package
XMC4[12]00-F64	EES-AA, ES-AA, ES-AB, AB	PG-LQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-53
XMC4[12]00-F64	BA	PG-TQFP-64-19
XMC4[12]00-Q48		PG-VQFN-48-71

### 1.4 Device Type Features

The following table lists the available features per device type.

**Table 3 Features of XMC4[12]00 Device Types**

Derivative <sup>1)</sup>	LEDTS Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4200-F64x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4200-Q48x256	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-F64x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4100-Q48x128	1	1	2 x 2	N0, N1 MO[0..63]
XMC4104-F64x64	1	–	2 x 2	–
XMC4104-Q48x64	1	–	2 x 2	–
XMC4104-F64x128	1	–	2 x 2	–
XMC4104-Q48x128	1	–	2 x 2	–
XMC4108-F64x64	–	–	2 x 2	N0, MO[0..31]
XMC4108-Q48x64	–	–	2 x 2	N0, MO[0..31]

1) x is a placeholder for the supported temperature range.

**Table 4 Features of XMC4[12]00 Device Types**

Derivative <sup>1)</sup>	ADC Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4200-F64x256	10	2	2 x 4	1 x 4	1	1
XMC4200-Q48x256	9	2	2 x 4	1 x 4	1	1
XMC4100-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4100-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x64	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x64	9	2	2 x 4	1 x 4	1	1
XMC4104-F64x128	10	2	2 x 4	1 x 4	1	1
XMC4104-Q48x128	9	2	2 x 4	1 x 4	1	1
XMC4108-F64x64	10	2	2 x 4	1 x 4	1	–
XMC4108-Q48x64	9	2	2 x 4	1 x 4	1	–

1) x is a placeholder for the supported temperature range.

## 1.5 Definition of Feature Variants

The XMC4[12]00 types are offered with several memory sizes and number of available VADC channels. [Table 5](#) describes the location of the available Flash memory, [Table 6](#) describes the location of the available SRAMs, [Table 7](#) the available VADC channels.

**Table 5 Flash Memory Ranges**

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	0800 0000 <sub>H</sub> – 0803 FFFF <sub>H</sub>	0C00 0000 <sub>H</sub> – 0C03 FFFF <sub>H</sub>
128 Kbytes	0800 0000 <sub>H</sub> – 0801 FFFF <sub>H</sub>	0C00 0000 <sub>H</sub> – 0C01 FFFF <sub>H</sub>
64 Kbytes	0800 0000 <sub>H</sub> – 0800 FFFF <sub>H</sub>	0C00 0000 <sub>H</sub> – 0C00 FFFF <sub>H</sub>

**Table 6 SRAM Memory Ranges**

Total SRAM Size	Program SRAM	System Data SRAM
40 Kbytes	1FFF C000 <sub>H</sub> – 1FFF FFFF <sub>H</sub>	2000 0000 <sub>H</sub> – 2000 5FFF <sub>H</sub>
20 Kbytes	1FFF E000 <sub>H</sub> – 1FFF FFFF <sub>H</sub>	2000 0000 <sub>H</sub> – 2000 2FFF <sub>H</sub>

**Table 7 ADC Channels<sup>1)</sup>**

Package	VADC G0	VADC G1
LQFP-64, TQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6
PG-VQFN-48	CH0, CH3..CH7	CH0, CH1, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

## 1.6 Identification Registers

The identification registers allow software to identify the marking.

**Table 8 XMC4200 Identification Registers**

Register Name	Value	Marking
SCU_IDCHIP	0004 2001 <sub>H</sub>	EES-AA, ES-AA
SCU_IDCHIP	0004 2002 <sub>H</sub>	ES-AB, AB
SCU_IDCHIP	0004 2003 <sub>H</sub>	BA
JTAG IDCODE	101D D083 <sub>H</sub>	EES-AA, ES-AA
JTAG IDCODE	201D D083 <sub>H</sub>	ES-AB, AB
JTAG IDCODE	301D D083 <sub>H</sub>	BA

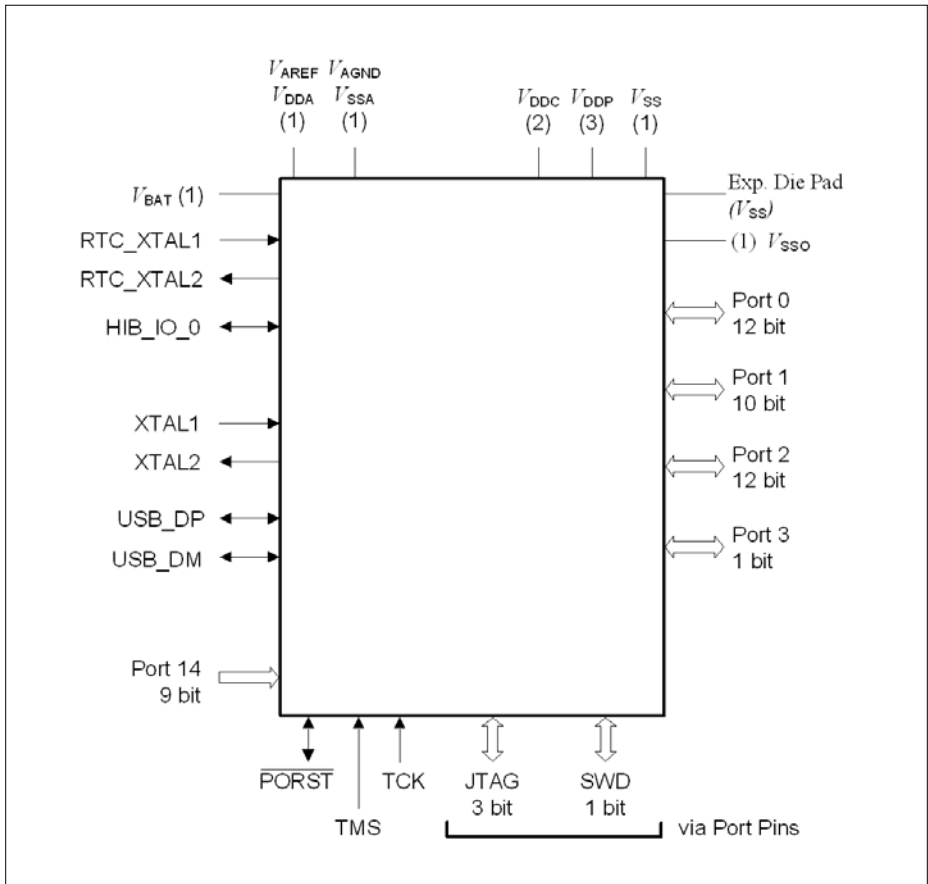
**Table 9 XMC4100 Identification Registers**

<b>Register Name</b>	<b>Value</b>	<b>Marking</b>
SCU_IDCHIP	0004 2001 <sub>H</sub>	EES-AA, ES-AA
SCU_IDCHIP	0004 2002 <sub>H</sub>	ES-AB, AB
SCU_IDCHIP	0004 1003 <sub>H</sub>	BA
JTAG IDCODE	101D D083 <sub>H</sub>	EES-AA, ES-AA
JTAG IDCODE	201D D083 <sub>H</sub>	ES-AB, AB
JTAG IDCODE	301D D083 <sub>H</sub>	BA

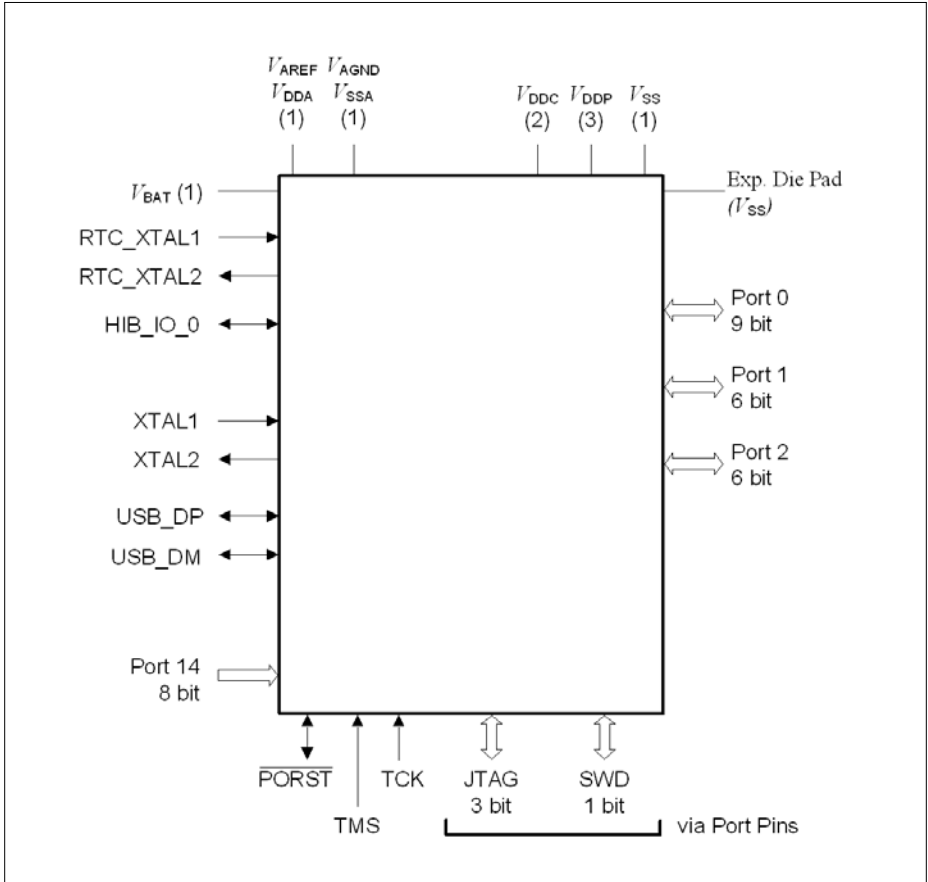
## 2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

### 2.1 Logic Symbols



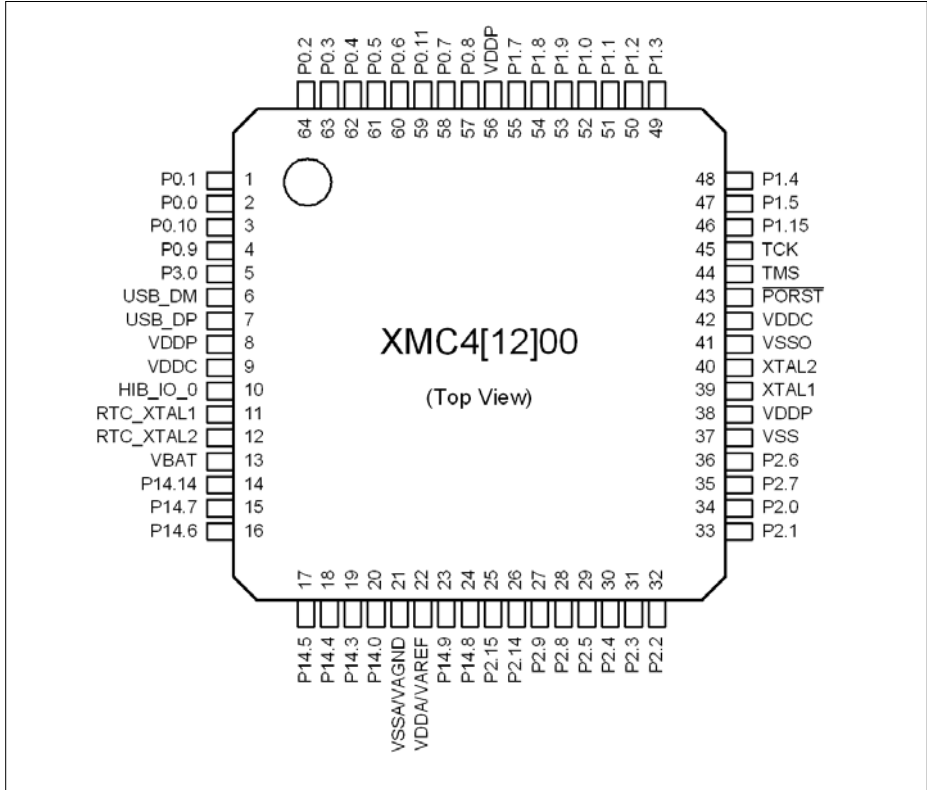
**Figure 2 XMC4[12]00 Logic Symbol PG-LQFP-64 and PG-TQFP-64**



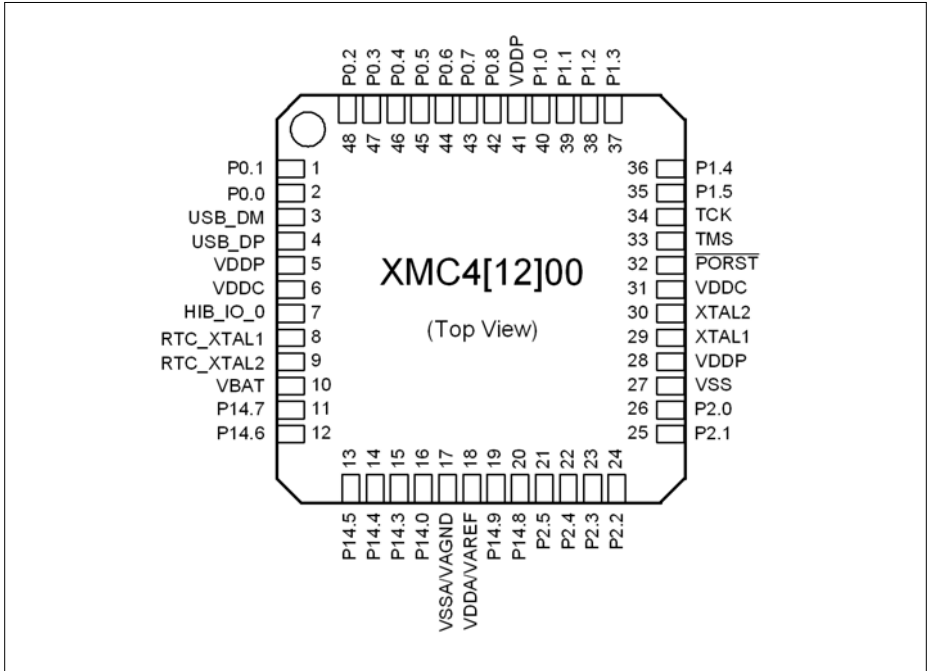
**Figure 3 XMC4[12]00 Logic Symbol PG-VQFN-48**

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.



**Figure 4 XMC4[12]00 PG-LQFP-64 and PG-TQFP-64 Pin Configuration (top view)**



**Figure 5 XMC4[12]00 PG-VQFN-48 Pin Configuration (top view)**

## 2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

**Table 10 Package Pin Mapping Description**

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A1+	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e.  $\overline{\text{PORST}}$ ) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, special=special pad, In=input pad, AN/DIG\_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

**Table 11 Package Pin Mapping**

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	64	48	A1+	
P0.3	63	47	A1+	
P0.4	62	46	A1+	
P0.5	61	45	A1+	
P0.6	60	44	A1+	
P0.7	58	43	A1+	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	57	42	A1+	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	4	-	A1+	
P0.10	3	-	A1+	

**General Device Information**

**Table 11 Package Pin Mapping (cont'd)**

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P0.11	59	-	A1+	
P1.0	52	40	A1+	
P1.1	51	39	A1+	
P1.2	50	38	A1+	
P1.3	49	37	A1+	
P1.4	48	36	A1+	
P1.5	47	35	A1+	
P1.7	55	-	A1+	
P1.8	54	-	A1+	
P1.9	53	-	A1+	
P1.15	46	-	A1+	
P2.0	34	26	A1+	
P2.1	33	25	A1+	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	32	24	A1+	
P2.3	31	23	A1+	
P2.4	30	22	A1+	
P2.5	29	21	A1+	
P2.6	36	-	A1+	
P2.7	35	-	A1+	
P2.8	28	-	A1+	
P2.9	27	-	A1+	
P2.14	26	-	A1+	
P2.15	25	-	A1+	
P3.0	5	-	A1+	
P14.0	20	16	AN/DIG_IN	
P14.3	19	15	AN/DIG_IN	
P14.4	18	14	AN/DIG_IN	
P14.5	17	13	AN/DIG_IN	
P14.6	16	12	AN/DIG_IN	
P14.7	15	11	AN/DIG_IN	
P14.8	24	20	AN/DAC/DIG_IN	

**General Device Information**
**Table 11 Package Pin Mapping (cont'd)**

Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
P14.9	23	19	AN/DAC/DIG_IN	
P14.14	14	-	AN/DIG_IN	
USB_DP	7	4	special	
USB_DM	6	3	special	
HIB_IO_0	10	7	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
TCK	45	34	A1	Weak pull-down active.
TMS	44	33	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
PORST	43	32	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	39	29	clock_IN	
XTAL2	40	30	clock_O	
RTC_XTAL1	11	8	clock_IN	
RTC_XTAL2	12	9	clock_O	
VBAT	13	10	Power	When VDDP is supplied VBAT has to be supplied as well.
VDDA/VAREF	22	18	AN_Power/AN_Ref	Shared analog supply and reference voltage pin.
VSSA/VAGND	21	17	AN_Power/AN_Ref	Shared analog supply and reference ground pin.
VDDC	9	6	Power	
VDDC	42	31	Power	
VDDP	8	5	Power	
VDDP	38	28	Power	
VDDP	56	41	Power	
VSS	37	27	Power	

**General Device Information**

**Table 11 Package Pin Mapping (cont'd)**

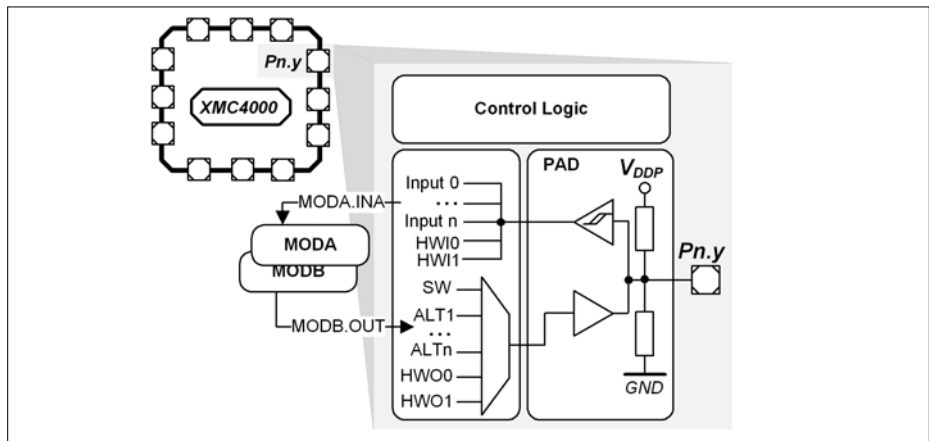
Function	LQFP-64 TQFP-64	VQFN-48	Pad Type	Notes
VSSO	41	-	Power	
VSS	Exp. Pad	Exp. Pad	Power	<p><b>Exposed Die Pad</b>            The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board.            For thermal aspects, please refer to the Data Sheet.            Board layout examples are given in an application note.</p>

## 2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

**Table 12 Port I/O Function Description**

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB



**Figure 6 Simplified Port Structure**

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn\_IN.y, Pn\_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn\_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn\_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

### 2.2.2.1 Port I/O Function Table

**Table 13 Port I/O Functions**

Function	Output				Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN. NO_TXD	CCU0. OUT2	LEDTS0. COL2			U1C1. DX00	ERJ0. 0B0	USB. VBUS/DETCT			HRP/WM0. C1NB	
P0.1		U1C1. DOU0	CCU0. OUT1	LEDTS0. COL3				ERJ0. 0A0				HRP/WM0. C2NB	
P0.2		U1C1. SELO	CCU0. OUT0	HRP/WM0. HROUT0	U1C0. DOU3	U1C0. HWI3		ERJ0. 3B3					
P0.3		U1C1. SEL0	CCU0. OUT0	HRP/WM0. HROUT20	U1C0. DOU2	U1C0. HWI2		ERJ1. 3B0					
P0.4		U1C0. DOU0	CCU0. OUT0	HRP/WM0. HROUT1	U1C0. DOU1	U1C0. HWI1		ERJ0. 2B3					
P0.5		U1C0. DOU0	CCU0. OUT0	HRP/WM0. HROUT0	U1C0. DOU0	U1C0. HWI0		ERJ1. 3A0					
P0.6		U1C0. SELO	CCU0. OUT30	HRP/WM0. HROUT30			U1C0. DX2A	ERJ0. 3B2		COJ0. IN2B			
P0.7	WM0T. SERVICE_OUT	U1C0. SELO	CCU0. OUT30	HRP/WM0. HROUT1		DB. TDI	U1C0. DX2B	ERJ0. 2B1		COJ0. IN2A	CCU0. IN2A	CCU0. IN2A	
P0.8	SQJ. ENCLK	U1C0. SCLKOUT	CCU0. OUT30	HRP/WM0. HROUT0		DB. TRST	U1C0. DX1B	ERJ0. 2A1		COJ0. IN1B			
P0.9	HRP/WM0. HROUT31	U1C1. SELO	CCU0. OUT2	LEDTS0. COL0			U1C1. DX2A	ERJ0. 1B0					
P0.10		U1C1. SCLKOUT	CCU0. OUT2	LEDTS0. COL1			U1C1. DX1A	ERJ0. 1A0					
P0.11		U1C0. SCLKOUT	CCU0. OUT31				U1C0. DX1A	ERJ0. 3A2					
P1.0		U1C0. SELO	CCU0. OUT3	ERJ1. P0OUT3			U1C0. DX2A	ERJ0. 3B0		COJ0. IN2A	HRP/WM0. C1NA		
P1.1		U1C0. SCLKOUT	CCU0. OUT2	ERJ1. P0OUT2			U1C0. DX1A	ERJ0. 3A0	POSIF0. IN2A	COJ0. IN2A	HRP/WM0. C1NA		
P1.2		U1C0. MCLKOUT	CCU0. OUT1	ERJ1. P0OUT1	U1C0. DOU3	U1C0. HWI3	U1C0. IN1A	ERJ1. 2B0	POSIF0. IN1A	COJ0. IN1A	HRP/WM0. C2NA		
P1.3		U1C0. MCLKOUT	CCU0. OUT0	ERJ1. P0OUT0	U1C0. DOU2	U1C0. HWI2	U1C0. IN0A	ERJ1. 2A0	POSIF0. IN0A	COJ0. IN0A	HRP/WM0. C0NB		
P1.4	WM0T. SERVICE_OUT	CAN. NO_TXD	CCU0. OUT33		U1C0. DOU1	U1C0. HWI1	U1C0. CAN. NO_RXD0	ERJ0. 2B0		COJ0. IN1C	HRP/WM0. B0A		
P1.5	CAN. NO_TXD	U1C0. DOU0	CCU0. OUT23		U1C0. DOU0	U1C0. HWI0	CAN. NO_RXD0A	ERJ1. 2A0		COJ0. IN1C	HRP/WM0. B0A		
P1.7		U1C0. DOU0		U1C1. SELO2				USB. VBUS/DETCT					

**Table 13 Port I/O Functions (cont'd)**

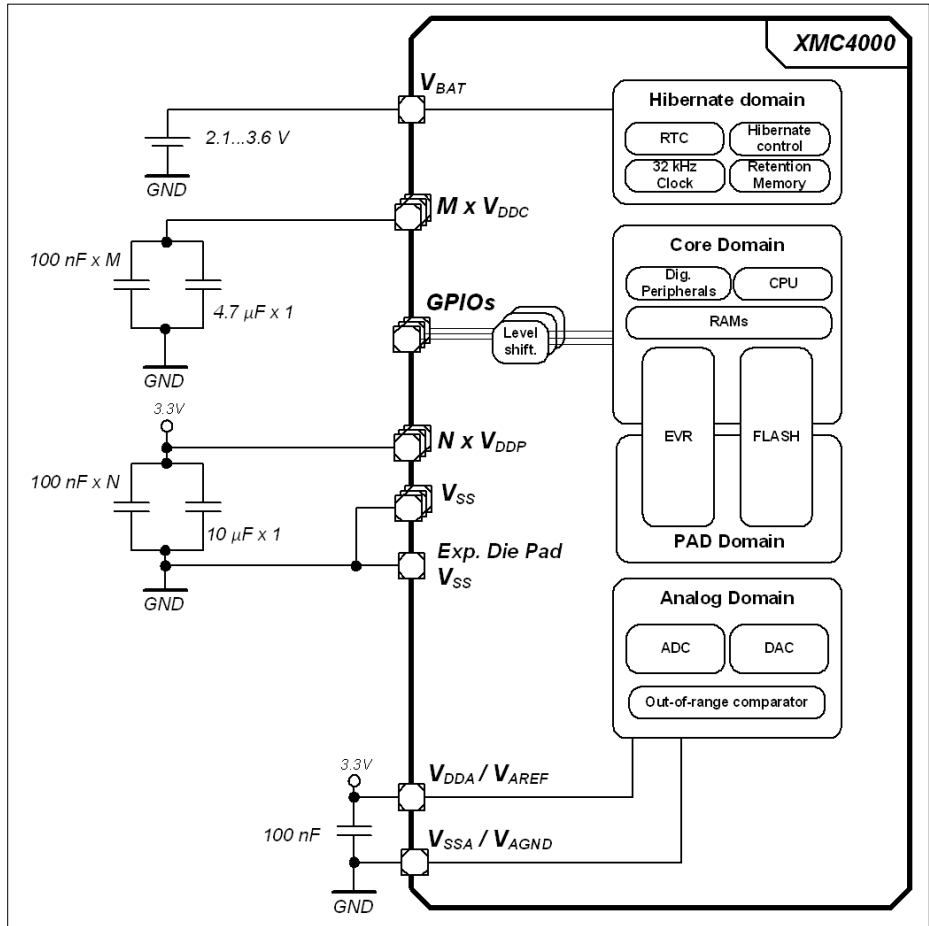
Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	Input	Input	Input	Input	Input			
P18		UIC0_SELO1		UIC1_SCLKOUT										
P19	UIC0_SCLKOUT			UIC1_SCLKOUT										
P115	SQU_EXCLK			UIC0_DOUT0						ERU1_1A0				
P20	CAN_NO_TXD			LEDTS0_COL1					ERJ0_0B3		COJ40_IN1C			
P21				LEDTS0_COLO	DR_TDO TRACE/SWO					ERU1_0B0	COJ40_IN1C			
P22	VADC_EMUX00		COJ41_OUT3	LEDTS0_LINE0	LEDTS0_EXTENDE00	LEDTS0_TSIN0A	UIC1_DANA	ERJ0_1B2			COJ41_IN1A			
P23	VADC_EMUX01	UIC1_SELO1	COJ41_OUT2	LEDTS0_LINE1	LEDTS0_EXTENDE01	LEDTS0_TSIN1A	UIC1_DX2A	ERJ0_1A2			COJ41_IN1A			
P24	VADC_EMUX02		COJ41_OUT1	LEDTS0_LINE2	LEDTS0_EXTENDE02	LEDTS0_TSIN2A	UIC1_DX1A	ERJ0_0B2			COJ41_IN1A	HRP/WM0_B11A		
P25		UIC1_DOUT0	COJ41_OUT0	LEDTS0_LINE3	LEDTS0_EXTENDE03	LEDTS0_TSIN3A	UIC1_DX0B	ERJ0_0A2			COJ41_IN1A	HRP/WM0_B12A		
P26			COJ90_OUT3	LEDTS0_COJ3			CAN_N1_TXDA	ERJ0_1B3			COJ40_IN1C			
P27		CAN_N1_TXD	COJ90_OUT03	LEDTS0_COJ2				ERU1_1B0			COJ40_IN1C			
P28			COJ90_OUT32	LEDTS0_LINE4	LEDTS0_EXTENDE04	LEDTS0_TSIN4A	DAC_TRIGGERS				COJ40_IN1B	COJ40_IN1B	COJ40_IN1B	COJ40_IN1B
P29			COJ90_OUT22	LEDTS0_LINE5	LEDTS0_EXTENDE05	LEDTS0_TSIN5A	DAC_TRIGGERM				COJ41_IN1B	COJ41_IN1B	COJ41_IN1B	COJ41_IN1B
P214	VADC_EMUX11	UIC0_DOUT0	COJ90_OUT21				UIC0_DAN0							
P215	VADC_EMUX12		COJ90_OUT11	LEDTS0_LINE6	LEDTS0_EXTENDE06	LEDTS0_TSIN6A	UIC0_DX0C							
P30		UIC1_SCLKOUT					UIC1_DX1B				COJ80_IN1C			
P14.0							VADC_G0CH0							
P14.3							VADC_G0CH3							
P14.4							VADC_G0CH4							
P14.5							VADC_G0CH5							
P14.6							VADC_G0CH6						GOOR05	
P14.7							VADC_G0CH7							
P14.8					DAC_OUT_0		VADC_G1CH0							

**Table 13 Port I/O Functions (cont'd)**

Function	Output					Input									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input	
P14.9					DAC OUT_1			VADC G1CCH							
P14.14								VADC G1CP9						G1ORC6	
USB_DP															
USB_DM															
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT					WAKEUPA					USB. VBUSDETCT C			
TCK						DB.TCK/ SWCLK									
TMS					DB.TMS/ SWDIO										
FORST															
XTAL1							U0C0. DX0F	U0C1. DX0F				U1C1. DX0F			
XTAL2															
RTC_XTAL1											ERN0. FBI				
RTC_XTAL2															

### 2.3 Power Connection Scheme

Figure 7 shows a reference power connection scheme for the XMC4[12]00.



**Figure 7 Power Connection Scheme**

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all  $V_{DDP}$  pins must be connected externally to one  $V_{DDP}$  net. In this reference scheme one 100 nF capacitor is connected at each supply pin against  $V_{SS}$ . An additional 10  $\mu$ F capacitor is connected to the  $V_{DDP}$  nets and an additional 4.7 $\mu$ F capacitor to the  $V_{DDC}$  nets.

The XMC4[12]00 has a common ground concept, all  $V_{SS}$ ,  $V_{SSA}$  and  $V_{SSO}$  pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

There are no dedicated connections for the analog reference  $V_{AREF}$  and  $V_{AGND}$ . Instead, they share the same pins as the analog supply pins  $V_{DDA}$  and  $V_{SSA}$ . Some analog channels can optionally serve as "Alternate Reference"; further details on this operating mode are described in the Reference Manual.

When  $V_{DDP}$  is supplied,  $V_{BAT}$  must be supplied as well. If no other supply source (e.g. battery) is connected to  $V_{BAT}$ , the  $V_{BAT}$  pin can also be connected directly to  $V_{DDP}$ .

## **3 Electrical Parameters**

### **3.1 General Parameters**

#### **3.1.1 Parameter Interpretation**

The parameters listed in this section partly represent the characteristics of the XMC4[12]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column "Symbol":

- **CC**  
Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[12]00 and must be regarded for system design.
- **SR**  
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[12]00 is designed in.

### 3.1.2 Absolute Maximum Ratings

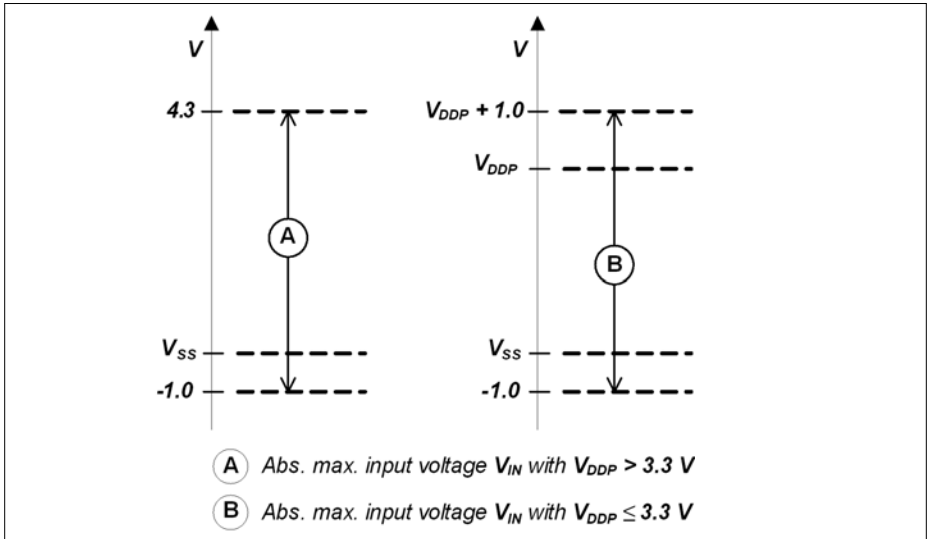
Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 14 Absolute Maximum Rating Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	$T_{ST}$	SR	-65	–	150	°C	–
Junction temperature	$T_J$	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to $V_{SS}$	$V_{DDP}$	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to $V_{SS}$	$V_{IN}$	SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to $V_{AGND}$	$V_{AIN}$ $V_{AREF}$	SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	$I_{IN}$	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition <sup>1)</sup>	$\Sigma I_{IN}$	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	$\Sigma I_{IN}$	SR	-100	–	+100	mA	

1) The port groups are defined in [Table 18](#).

**Figure 8** explains the input voltage ranges of  $V_{IN}$  and  $V_{AIN}$  and its dependency to the supply level of  $V_{DDP}$ . The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above  $V_{DDP}$ . For the range up to  $V_{DDP} + 1.0$  V also see the definition of the overload conditions in “**Pin Reliability in Overload**”.



**Figure 8 Absolute Maximum Input Voltage Ranges**

### 3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 15** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **“Operating Conditions”** are met for
  - pad supply levels ( $V_{DDP}$  or  $V_{DDA}$ )
  - temperature

If a pin current is outside of the **“Operating Conditions”** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

*Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

**Table 15 Overload Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	$I_{OV}$ SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition <sup>1)</sup>	$I_{OVG}$ SR	–	–	20	mA	$\Sigma I_{OVx} $ , for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma I_{OVx} $ , for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	$I_{OVS}$ SR	–	–	80	mA	$\Sigma I_{OVG}$

1) The port groups are defined in **Table 18**.

**Figure 9** shows the path of the input currents during overload via the ESD protection structures. The diodes against  $V_{DDP}$  and ground are a simplified representation of these ESD protection structures.

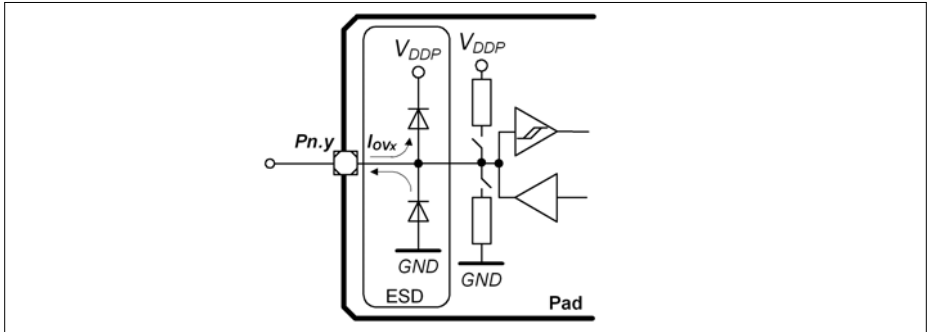


Figure 9 Input Overload Current via ESD structures

Table 16 and Table 17 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the “**Absolute Maximum Ratings**” must not be exceeded during overload.

Table 16 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}, T_J = -40 \text{ }^\circ\text{C}$	$I_{OV} = 5 \text{ mA}, T_J = 150 \text{ }^\circ\text{C}$
A1 / A1+	$V_{IN} = V_{DDP} + 1.0 \text{ V}$	$V_{IN} = V_{DDP} + 0.75 \text{ V}$
AN/DIG_IN	$V_{IN} = V_{DDP} + 1.0 \text{ V}$	$V_{IN} = V_{DDP} + 0.75 \text{ V}$

Table 17 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}, T_J = -40 \text{ }^\circ\text{C}$	$I_{OV} = 5 \text{ mA}, T_J = 150 \text{ }^\circ\text{C}$
A1 / A1+	$V_{IN} = V_{SS} - 1.0 \text{ V}$	$V_{IN} = V_{SS} - 0.75 \text{ V}$
AN/DIG_IN	$V_{IN} = V_{DDP} - 1.0 \text{ V}$	$V_{IN} = V_{DDP} - 0.75 \text{ V}$

Table 18 Port Groups for Overload and Short-Circuit Current Sum Parameters

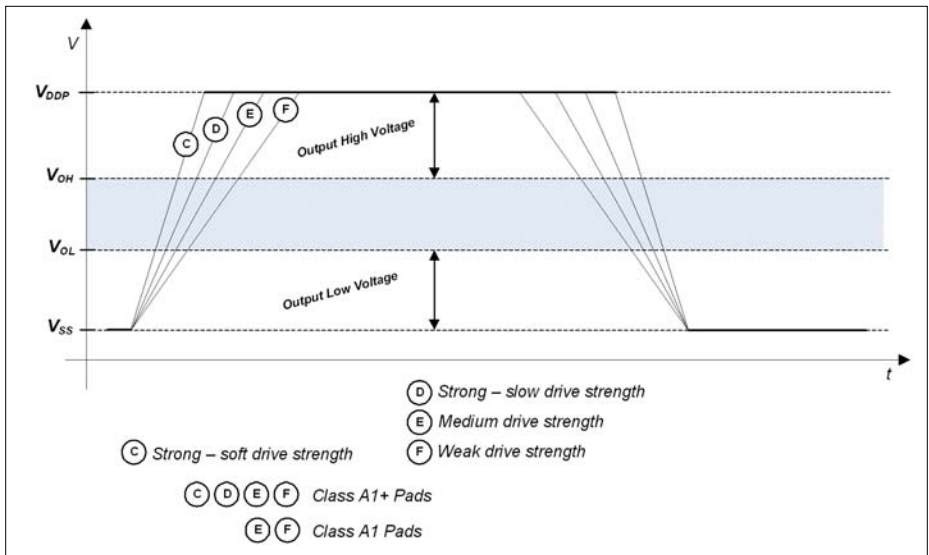
Group	Pins
1	P0.[12:0], P3.0
2	P14.[8:0]
3	P2.[15:0]
4	P1.[15:0]

### 3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **“Input/Output Pins”**.

**Table 19 Pad Driver and Pad Classes Overview**

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	A1 (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended



**Figure 10 Output Slopes with different Pad Driver Modes**

**Figure 10** is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **“Input/Output Pins”**.

### 3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4[12]00. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

**Table 20 Operating Conditions Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	$T_A$ SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	$V_{DDP}$ SR	3.13 <sup>1)</sup>	3.3	3.63 <sup>2)</sup>	V	
Core Supply Voltage	$V_{DDC}$ CC	– <sup>1)</sup>	1.3	–	V	Generated internally
Digital ground voltage	$V_{SS}$ SR	0	–	–	V	
ADC analog supply voltage	$V_{DDA}$ SR	3.0	3.3	3.6 <sup>2)</sup>	V	
Analog ground voltage for $V_{DDA}$	$V_{SSA}$ SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain <sup>3)</sup>	$V_{BAT}$ SR	1.95 <sup>4)</sup>	–	3.63	V	When $V_{DDP}$ is supplied $V_{BAT}$ has to be supplied as well.
System Frequency	$f_{SYS}$ SR	–	–	80	MHz	
Short circuit current of digital outputs	$I_{SC}$ SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group <sup>5)</sup>	$\Sigma I_{SC\_PG}$ SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	$\Sigma I_{SC\_D}$ SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, [Section 3.3.2](#).

2) Voltage overshoot to 4.0 V is permissible at Power-Up and  $\overline{PORST}$  low, provided the pulse duration is less than 100  $\mu$ s and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, [Section 3.2.6](#).

4) To start the hibernate domain it is required that  $V_{BAT} \geq 2.1$  V, for a reliable start of the oscillation of RTC\_XTAL in crystal mode it is required that  $V_{BAT} \geq 3.0$  V.

5) The port groups are defined in [Table 18](#).

### 3.2 DC Parameters

#### 3.2.1 Input/Output Pins

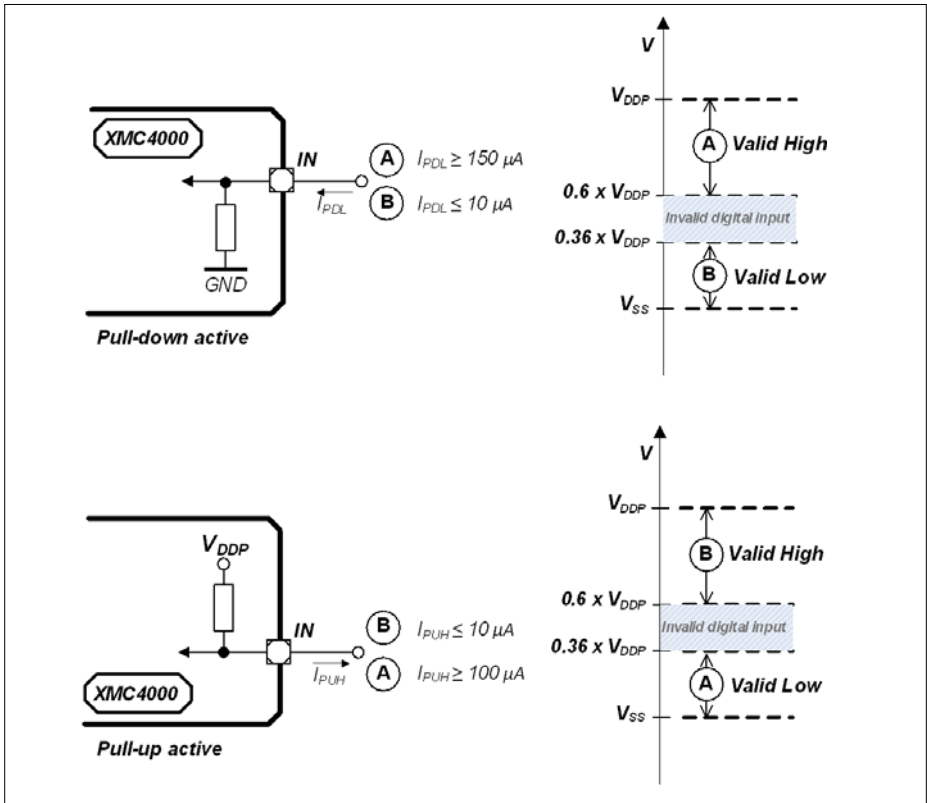
The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.

The pull-up characteristics ( $I_{PUH}$ ) and the input high and low voltage levels ( $V_{IH}$  and  $V_{IL}$ ) of the  $\overline{\text{PORST}}$  pin are identical to the respective values of the standard digital input/output pins.

**Table 21 Standard Pad Parameters**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	$C_{IO}$ CC	–	10	pF	
Pull-down current	$ I_{PDL} $ SR	150	–	$\mu\text{A}$	<sup>1)</sup> $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	$\mu\text{A}$	<sup>2)</sup> $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-up current	$ I_{PUH} $ SR	–	10	$\mu\text{A}$	<sup>2)</sup> $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	$\mu\text{A}$	<sup>1)</sup> $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes <sup>3)</sup>	$HYS_A$ CC	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	$t_{SF1}$ CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	$t_{SF2}$ CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$ I_{PPD} $ CC	13	–	mA	$V_i = 1.0 \text{ V}$

- 1) Current required to override the pull device with the opposite logic level ("force current").  
With active pull device, at load currents between force and keep current the input state is undefined.
- 2) Load current at which the pull device still maintains the valid logic level ("keep current").  
With active pull device, at load currents between force and keep current the input state is undefined.
- 3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.



**Figure 11 Pull Device Input Characteristics**

**Figure 11** visualizes the input characteristics with an active internal pull device:

- in the cases "A" the internal pull device is overridden by a strong external driver;
- in the cases "B" the internal pull device defines the input logical state against a weak external load.

**Table 22 Standard Pads Class\_A1**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZA1}$ CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	$V_{IHA1}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA1}$ SR	-0.3	$0.36 \times V_{DDP}$	V	
Output high voltage, POD <sup>1)</sup> = weak	$V_{OHA1}$ CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\ \mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\ \mu\text{A}$
Output high voltage, POD <sup>1)</sup> = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\ \text{mA}$
		2.4	–	V	$I_{OH} \geq -2\ \text{mA}$
Output low voltage	$V_{OLA1}$ CC	–	0.4	V	$I_{OL} \leq 500\ \mu\text{A}$ ; POD <sup>1)</sup> = weak
		–	0.4	V	$I_{OL} \leq 2\ \text{mA}$ ; POD <sup>1)</sup> = medium
Fall time	$t_{FA1}$ CC	–	150	ns	$C_L = 20\ \text{pF}$ ; POD <sup>1)</sup> = weak
		–	50	ns	$C_L = 50\ \text{pF}$ ; POD <sup>1)</sup> = medium
Rise time	$t_{RA1}$ CC	–	150	ns	$C_L = 20\ \text{pF}$ ; POD <sup>1)</sup> = weak
		–	50	ns	$C_L = 50\ \text{pF}$ ; POD <sup>1)</sup> = medium

1) POD = Pin Out Driver

**Table 23 Standard Pads Class\_A1+**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZA1+}$ CC	-1	1	$\mu\text{A}$	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	$V_{IHA1+}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA1+}$ SR	-0.3	$0.36 \times V_{DDP}$	V	

**Electrical Parameters**
**Table 23 Standard Pads Class\_A1+**

Parameter	Symbol	Values		Unit	Note / Test Condition	
		Min.	Max.			
Output high voltage, POD <sup>1)</sup> = weak	V <sub>OHA1+</sub> CC	V <sub>DDP</sub> - 0.4	–	V	I <sub>OH</sub> ≥ -400 μA	
		2.4	–	V	I <sub>OH</sub> ≥ -500 μA	
Output high voltage, POD <sup>1)</sup> = medium		V <sub>DDP</sub> - 0.4	–	V	I <sub>OH</sub> ≥ -1.4 mA	
		2.4	–	V	I <sub>OH</sub> ≥ -2 mA	
Output high voltage, POD <sup>1)</sup> = strong		V <sub>DDP</sub> - 0.4	–	V	I <sub>OH</sub> ≥ -1.4 mA	
		2.4	–	V	I <sub>OH</sub> ≥ -2 mA	
Output low voltage		V <sub>OLA1+</sub> CC	–	0.4	V	I <sub>OL</sub> ≤ 500 μA; POD <sup>1)</sup> = weak
			–	0.4	V	I <sub>OL</sub> ≤ 2 mA; POD <sup>1)</sup> = medium
	–		0.4	V	I <sub>OL</sub> ≤ 2 mA; POD <sup>1)</sup> = strong	
Fall time	t <sub>FA1+</sub> CC	–	150	ns	C <sub>L</sub> = 20 pF; POD <sup>1)</sup> = weak	
		–	50	ns	C <sub>L</sub> = 50 pF; POD <sup>1)</sup> = medium	
		–	28	ns	C <sub>L</sub> = 50 pF; POD <sup>1)</sup> = strong; edge = slow	
		–	16	ns	C <sub>L</sub> = 50 pF; POD <sup>1)</sup> = strong; edge = soft;	
Rise time	t <sub>RA1+</sub> CC	–	150	ns	C <sub>L</sub> = 20 pF; POD <sup>1)</sup> = weak	
		–	50	ns	C <sub>L</sub> = 50 pF; POD <sup>1)</sup> = medium	
		–	28	ns	C <sub>L</sub> = 50 pF; POD <sup>1)</sup> = strong; edge = slow	
		–	16	ns	C <sub>L</sub> = 50 pF; POD <sup>1)</sup> = strong; edge = soft	

1) POD = Pin Out Driver

**Table 24 HIB\_IO Class\_A1 special Pads**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZHIB}$ CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{BAT}$
Input high voltage	$V_{IHIB}$ SR	$0.6 \times V_{BAT}$	$V_{BAT} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILHIB}$ SR	-0.3	$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins <sup>1)</sup>	$HYSHIB$ CC	$0.1 \times V_{BAT}$	–	V	$V_{BAT} \geq 3.13\text{ V}$
		$0.06 \times V_{BAT}$	–	V	$V_{BAT} < 3.13\text{ V}$
Output high voltage, POD <sup>1)</sup> = medium	$V_{OHHIB}$ CC	$V_{BAT} - 0.4$	–	V	$I_{OH} \geq -1.4\text{ mA}$
Output low voltage	$V_{OLHIB}$ CC	–	0.4	V	$I_{OL} \leq 2\text{ mA}$
Fall time	$t_{FHIB}$ CC	–	50	ns	$V_{BAT} \geq 3.13\text{ V}$ $C_L = 50\text{ pF}$
		–	100	ns	$V_{BAT} < 3.13\text{ V}$ $C_L = 50\text{ pF}$
Rise time	$t_{RHIB}$ CC	–	50	ns	$V_{BAT} \geq 3.13\text{ V}$ $C_L = 50\text{ pF}$
		–	100	ns	$V_{BAT} < 3.13\text{ V}$ $C_L = 50\text{ pF}$

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

**3.2.2 Analog to Digital Converters (ADCx)**
**Table 25 ADC Parameters (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage	$V_{AREF}$ SR	–	–	–	V	$V_{AREF} = V_{DDA}$ shared analog supply and reference input pin
Alternate reference voltage <sup>5)</sup>	$V_{AREF}$ SR	$V_{AGND} + 1$	–	$V_{DDA} + 0.05^{1)}$	V	
Analog reference ground	$V_{AGND}$ SR	–	–	–	V	$V_{AGND} = V_{SSA}$ shared analog supply and reference input pin
Alternate reference voltage range <sup>2)5)</sup>	$V_{AREF} - V_{AGND}$ SR	1	–	$V_{DDA} + 0.1$	V	
Analog input voltage	$V_{AIN}$ SR	$V_{AGND}$	–	$V_{DDA}$	V	
Input leakage at analog inputs <sup>3)</sup>	$I_{OZ1}$ CC	–100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		–500	–	100	nA	$0 \text{ V} \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		–100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Internal ADC clock	$f_{ADCI}$ CC	2	–	30	MHz	$V_{DDA} = 3.3 \text{ V}$
Switched capacitance at the analog voltage inputs <sup>4)</sup>	$C_{AINSW}$ CC	–	4	6.5	pF	
Total capacitance of an analog input	$C_{AINTOT}$ CC	–	12	20	pF	
Switched capacitance at the alternate reference voltage input <sup>5)6)</sup>	$C_{AREFSW}$ CC	–	15	30	pF	

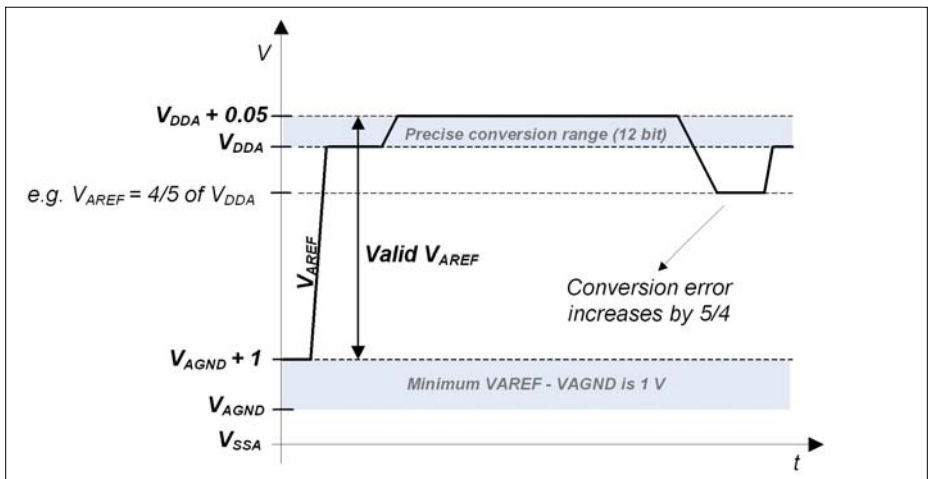
**Electrical Parameters**
**Table 25 ADC Parameters (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total capacitance of the alternate reference inputs <sup>5)</sup>	$C_{AREFTOT}$ CC	–	20	40	pF	
Total Unadjusted Error	$TUE$ CC	-6	–	6	LSB	12-bit resolution; $V_{DDA} = 3.3\text{ V}$ ; $V_{AREF} = V_{DDA}$ <sup>7)</sup>
Differential Non-Linearity Error <sup>8)</sup>	$EA_{DNL}$ CC	-4.5	–	4.5	LSB	
Gain Error <sup>8)</sup>	$EA_{GAIN}$ CC	-6	–	6	LSB	
Integral Non-Linearity <sup>8)</sup>	$EA_{INL}$ CC	-4.5	–	4.5	LSB	
Offset Error <sup>8)</sup>	$EA_{OFF}$ CC	-6	–	6	LSB	
RMS Noise <sup>9)</sup>	$EN_{RMS}$ CC	–	1	2 <sup>10)11)</sup>	LSB	
Worst case ADC $V_{DDA}$ power supply current per active converter	$I_{DDAA}$ CC	–	1.5	2	mA	during conversion $V_{DDP} = 3.6\text{ V}$ , $T_J = 150\text{ °C}$
Charge consumption on alternate reference per conversion <sup>5)</sup>	$Q_{CONV}$ CC	–	30	–	pC	$0\text{ V} \leq V_{AREF} \leq V_{DDA}$ <sup>12)</sup>
ON resistance of the analog input path	$R_{AIN}$ CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	$R_{AIN7T}$ CC	180	550	900	Ohm	

- 1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
- 2) If the analog reference voltage is below  $V_{DDA}$ , then the ADC converter errors increase. If the reference voltage is reduced by the factor  $k$  ( $k < 1$ ), TUE, DNL, INL, Gain, and Offset errors increase also by the factor  $1/k$ .
- 3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see [Figure 14](#)).
- 4) The sampling capacity of the conversion C-network is pre-charged to  $V_{AREF}/2$  before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from  $V_{AREF}/2$ .
- 5) Applies to AINx, when used as alternate reference input.
- 6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
- 7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than  $\pm 1$  LSB.

**Electrical Parameters**

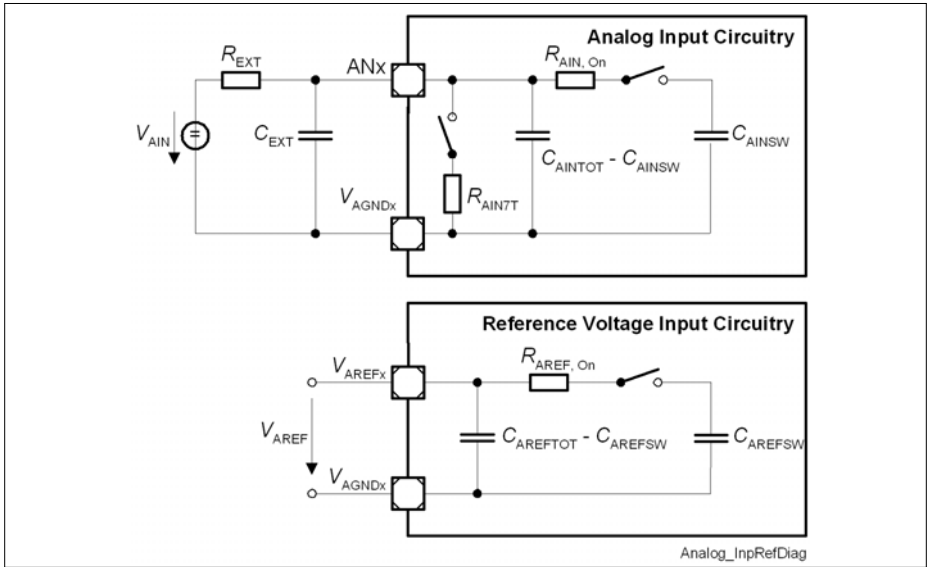
- 8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
- 9) This parameter is valid for soldered devices and requires careful analog board design.
- 10) Resulting worst case combined error is arithmetic combination of TUE and  $EN_{RMS}$ .
- 11) Value is defined for one sigma Gauss distribution.
- 12) The resulting current for a conversion can be calculated with  $I_{AREF} = Q_{CONV} / t_c$ .  
The fastest 12-bit post-calibrated conversion of  $t_c = 566$  ns results in a typical average current of  $I_{AREF} = 53 \mu A$ .



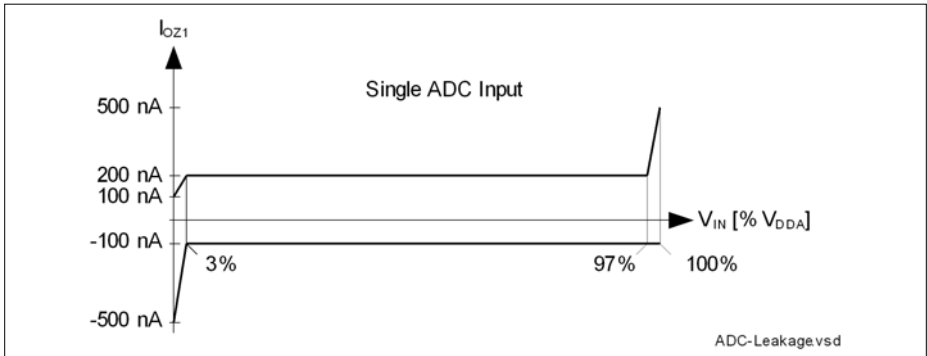
**Figure 12 VADC Reference Voltage Range**

**Electrical Parameters**

The power-up calibration of the ADC requires a maximum number of  $4 \cdot 352 \cdot f_{\text{ADCI}}$  cycles.



**Figure 13 ADCx Input Circuits**



**Figure 14 ADCx Analog Input Leakage Current**

**Conversion Time**
**Table 26 Conversion Time** (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	$t_C$ CC	$2 \times T_{ADC} + (2 + N + STC + PC + DM) \times T_{ADCI}$	$\mu\text{s}$	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

**Conversion Time Examples**

System assumptions (max.  $f_{ADC}$ ):

$$f_{ADC} = 80 \text{ MHz i.e. } t_{ADC} = 12.5 \text{ ns, DIVA} = 2, f_{ADCI} = 26.7 \text{ MHz i.e. } t_{ADCI} = 37.5 \text{ ns}$$

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):

$$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 37.5 \text{ ns} + 2 \times 12.5 \text{ ns} = 625 \text{ ns}$$

12-bit uncalibrated conversion:

$$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 37.5 \text{ ns} + 2 \times 12.5 \text{ ns} = 550 \text{ ns}$$

10-bit uncalibrated conversion:

$$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 37.5 \text{ ns} + 2 \times 12.5 \text{ ns} = 475 \text{ ns}$$

8-bit uncalibrated:

$$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 37.5 \text{ ns} + 2 \times 12.5 \text{ ns} = 400 \text{ ns}$$

System assumptions (max.  $f_{ADCI}$ ):

$$f_{ADC} = 60 \text{ MHz i.e. } t_{ADC} = 16.67 \text{ ns, DIVA} = 1, f_{ADCI} = 30 \text{ MHz i.e. } t_{ADCI} = 33.33 \text{ ns}$$

12-bit post-calibrated conversion (PC = 2):

$$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.33 \text{ ns} + 2 \times 16.67 \text{ ns} = 566 \text{ ns}$$

### 3.2.3 Digital to Analog Converters (DACx)

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 27 DAC Parameters** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMS supply current	$I_{DD}$ CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	$RES$ CC	–	12	–	Bit	
Update rate	$f_{URATE\_A}$ CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to $\pm 1$ LSB accuracy
Update rate	$f_{URATE\_F}$ CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to $\pm 4$ LSB accuracy
Settling time	$t_{SETTLE}$ CC	–	1	2	$\mu$ s	at full scale jump, output voltage reaches target value $\pm 20$ LSB
Slew rate	$SR$ CC	2	5	–	V/ $\mu$ s	
Minimum output voltage	$V_{OUT\_MIN}$ CC	–	0.3	–	V	code value unsigned: 000 <sub>H</sub> ; signed: 800 <sub>H</sub>
Maximum output voltage	$V_{OUT\_MAX}$ CC	–	2.5	–	V	code value unsigned: FFF <sub>H</sub> ; signed: 7FF <sub>H</sub>
Integral non-linearity <sup>1)</sup>	$INL$ CC	-5.5	$\pm 2.5$	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	$DNL$ CC	-2	$\pm 1$	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

**Electrical Parameters**
**Table 27 DAC Parameters (Operating Conditions apply) (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error	$ED_{OFF}$ CC		±20		mV	
Gain error	$ED_{G\_IN}$ CC	-5	0	5	%	
Startup time	$t_{STARTUP}$ CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	$f_{C1}$ CC	2.5	5	–	MHz	verified by design
Output sourcing current	$I_{OUT\_SOURCE}$ CC	–	-30	–	mA	
Output sinking current	$I_{OUT\_SINK}$ CC	–	0.6	–	mA	
Output resistance	$R_{OUT}$ CC	–	50	–	Ohm	
Load resistance	$R_L$ SR	5	–	–	kOhm	
Load capacitance	$C_L$ SR	–	–	50	pF	
Signal-to-Noise Ratio	SNR CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	THD CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	PSRR CC	–	56	–	dB	to $V_{DDA}$ verified by design

1) According to best straight line method.

**Conversion Calculation**

Unsigned:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT\_MIN}) / (V_{OUT\_MAX} - V_{OUT\_MIN})$$

Signed:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT\_MIN}) / (V_{OUT\_MAX} - V_{OUT\_MIN}) - 2048$$

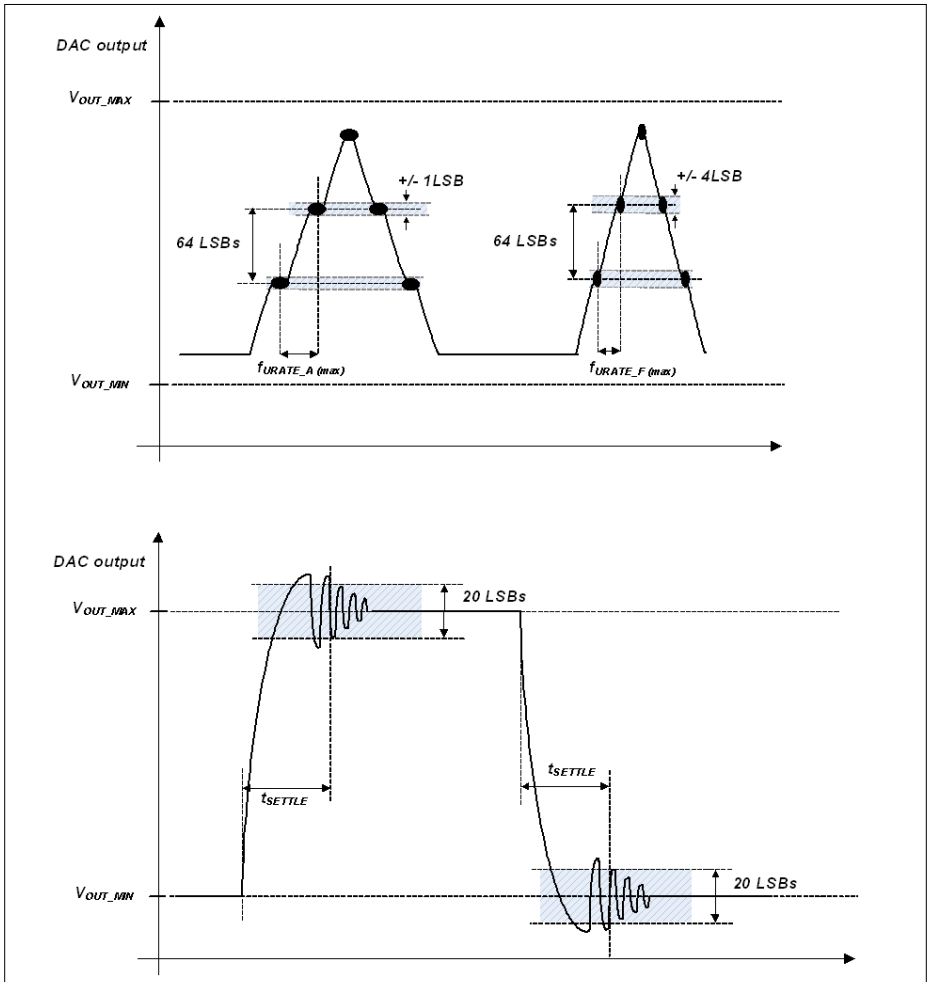


Figure 15 DAC Conversion Examples

### 3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages ( $V_{AIN}$ ) above the analog reference<sup>1)</sup> ( $V_{AREF}$ ) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

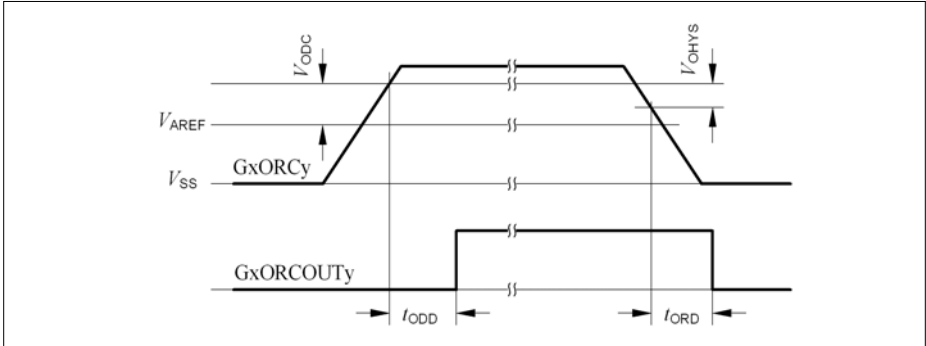
*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The parameters in **Table 28** apply for the maximum reference voltage  $V_{AREF} = V_{DDA} + 50$  mV.

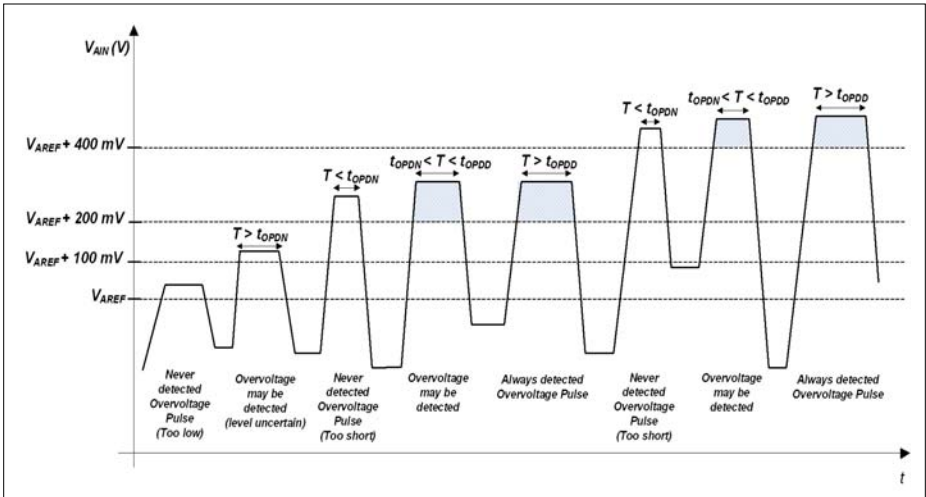
**Table 28 ORC Parameters** (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	$V_{ODC}$	CC	100	125	200	mV	Ax-marking devices $V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	$V_{OHYS}$	CC	50	–	$V_{ODC}$	mV	
Detection Delay of a persistent Overvoltage	$t_{ODD}$	CC	55	–	450	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	$t_{OPDD}$	CC	440	–	–	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	$t_{OPDN}$	CC	–	–	49	ns	Ax-marking devices $V_{AIN} \geq V_{AREF} + 200$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	$t_{ORD}$	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	$t_{OED}$	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.



**Figure 16 GxORCOUTy Trigger Generation**



**Figure 17 ORC Detection Ranges**

### 3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock,  $f_{hrpwm}$ .

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.2.5.1 HRC characteristics

**Table 29** summarizes the characteristics of the HRC units.

**Table 29 HRC characteristics** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High resolution step size <sup>1)2)</sup>	$t_{HRS}$ CC	–	150	–	ps	
Startup time (after reset release)	$t_{start}$ CC	–	–	2	μs	

1) The step size for clock frequencies equal to 180, 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 180, 120 and 80 MHz but within the range from 180 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

#### 3.2.5.2 CMP and 10-bit DAC characteristics

The **Table 30** summarizes the characteristics of the CSG unit.

The specified characteristics require that the setup of the HRPWM follows the initialization sequence as documented in the Reference Manual.

**Table 30 CMP and 10-bit DAC characteristics** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAC Resolution	$RES$ CC		10		bits	
DAC differential nonlinearity	$DNL$ CC	-1	–	1.5	LSB	Monotonic behavior See <b>Figure 18</b>
DAC integral nonlinearity	$INL$ CC	-3	–	3	LSB	See <b>Figure 18</b>

**Electrical Parameters**
**Table 30 CMP and 10-bit DAC characteristics (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSG Output Jitter	$D_{CSG}$ CC	–	–	1	clk	
Bias startup time	$t_{start}$ CC	–	–	98	us	
Bias supply current	$I_{DDbias}$ CC	–	–	400	μA	
CSGy startup time	$t_{CSGS}$ CC	–	–	2	μs	
Input operation current <sup>1)</sup>	$I_{DDCIN}$ CC	-10	–	33	μA	See <a href="#">Figure 19</a>
<b>High Speed Mode</b>						
DAC output voltage range	$V_{DOUT}$ CC	$V_{SS}$	–	$V_{DDP}$	V	
DAC propagation delay - Full scale	$t_{FShs}$ CC	–	–	80	ns	See <a href="#">Figure 20</a>
Input Selector propagation delay - Full scale	$t_{Dhs}$ CC	–	–	100	ns	See <a href="#">Figure 20</a>
Comparator bandwidth	$t_{Dhs}$ CC	20	–	–	ns	
DAC CLK frequency	$f_{clk}$ SR	–	–	30	MHz	
Supply current	$I_{DDhs}$ CC	–	–	940	μA	
<b>Low Speed Mode</b>						
DAC output voltage range	$V_{DOUT}$ CC	$0.1 \times V_{DDP}^{2)}$	–	$V_{DDP}$	V	
DAC propagation delay - Full Scale	$t_{FSls}$ CC	–	–	160	ns	See <a href="#">Figure 20</a>
Input Selector propagation delay - Full Scale	$t_{Dis}$ CC	–	–	200	ns	See <a href="#">Figure 20</a>
Comparator bandwidth	$t_{Dis}$ CC	20	–	–	ns	
DAC CLK frequency	$f_{clk}$ SR	–	–	30	MHz	
Supply current	$I_{DDls}$ CC	–	–	300	μA	

1) Typical input resistance  $R_{CIN} = 100k\Omega$ .

2) The INL error increases for DAC output voltages below this limit.

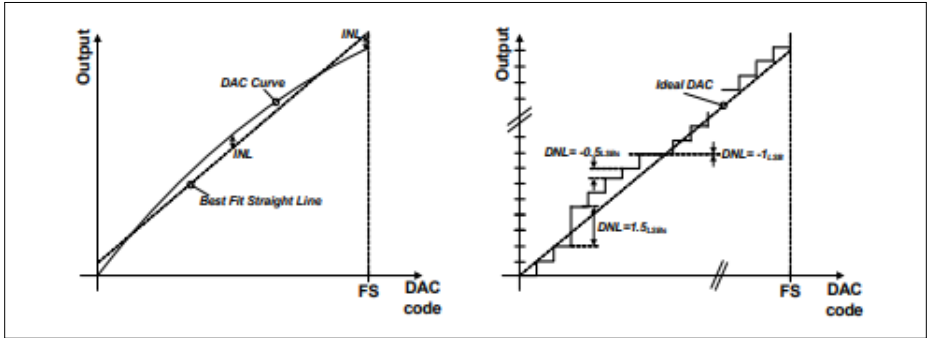


Figure 18 CSG DAC INL and DNL example

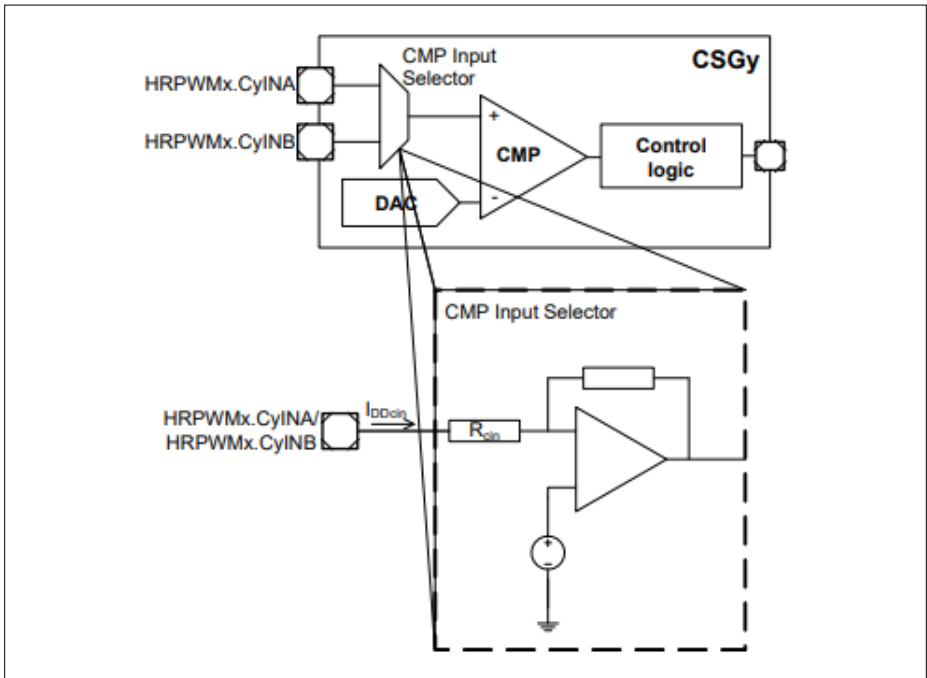


Figure 19 Input operation current

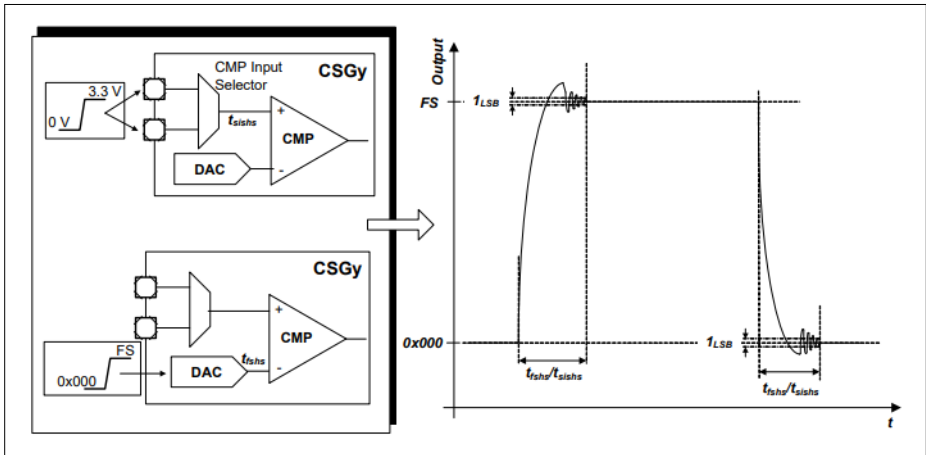


Figure 20 DAC and Input Selector Propagation Delay

### 3.2.5.3 Clocks

#### HRPWM DAC Conversion Clock

The DAC conversion clock can be generated internally or it can be controlled via a HRPWM module pin.

Table 31 External DAC conversion trigger operating conditions

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	$f_{etrg}$	SR	–	–	30 <sup>2)</sup>	MHz	
ON time	$t_{onetrg}$	SR	$2T_{ccu}^{1)2)}$	–	–	ns	
OFF time	$t_{offetrg}$	SR	$2T_{ccu}^{1)2)}$	–	–	ns	

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

#### CSG External Clock

It is possible to select an external source, that can be used as a clock for the slope generation, HRPWMx.ECLKy. This clock is synchronized internally with the module clock and therefore the external clock needs to meet the criterion described on [Table 32](#).

**Table 32 External clock operating conditions**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency	$f_{\text{eck}}$ SR	–	–	$f_{\text{hrpwm}}/4$	MHz	
ON time	$t_{\text{oneck}}$ SR	$2T_{\text{ccu}}^{1)2)}$	–	–	ns	
OFF time	$t_{\text{offeck}}$ SR	$2T_{\text{ccu}}^{1)2)}$	–	–	ns	Only the rising edge is used

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

### 3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing  $V_{\text{BAT}}$  or another external sensor voltage  $V_{\text{LPS}}$  with a pre-programmed threshold voltage.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 33 Low Power Analog Comparator Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$V_{\text{BAT}}$ supply voltage range for LPAC operation	$V_{\text{BAT}}$ SR	2.1	–	3.6	V	
Sensor voltage range	$V_{\text{LPCS}}$ CC	0	–	1.2	V	
Threshold step size	$V_{\text{th}}$ CC	–	18.75	–	mV	
Threshold trigger accuracy	$\Delta V_{\text{th}}$ CC	–	–	$\pm 10$	%	for $V_{\text{th}} > 0.4 \text{ V}$
Conversion time	$t_{\text{LPCC}}$ CC	–	–	250	$\mu\text{s}$	
Average current consumption over time	$I_{\text{LPCAC}}$ CC	–	–	15	$\mu\text{A}$	conversion interval 10 ms <sup>1)</sup>
Current consumption during conversion	$I_{\text{LPCC}}$ CC	–	150	–	$\mu\text{A}$	<sup>1)</sup>

1) Single channel conversion, measuring  $V_{\text{BAT}} = 3.3 \text{ V}$ , 8 cycles settling time

### 3.2.7 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature  $T_J$ .

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 34 Die Temperature Sensor Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature sensor range	$T_{SR}$ SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	$\Delta T_{LE}$ CC	–	$\pm 1$	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	$\Delta T_{OE}$ CC	–	$\pm 6$	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V <sup>1)</sup>
Measurement time	$t_M$ CC	–	–	100	μs	
Start-up time after reset inactive	$t_{TSST}$ SR	–	–	10	μs	

1) At  $V_{DDP\_max} = 3.63$  V the typical offset error increases by an additional  $\Delta T_{OE} = \pm 1$  °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

$$\text{Temperature } T_{DTS} = (\text{RESULT} - 605) / 2.05 \text{ [°C]}$$

This formula and the values defined in [Table 34](#) apply with the following calibration values:

- DTSCON.BGTRIM =  $8_H$
- DTSCON.REFTRIM =  $4_H$

### 3.2.8 USB Device Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification. High-Speed Mode is not supported.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 35 USB Device Data Line (USB\_DP, USB\_DM) Parameters (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage	$V_{IL}$ SR	–	–	0.8	V	
Input high voltage (driven)	$V_{IH}$ SR	2.0	–	–	V	
Input high voltage (floating) <sup>1)</sup>	$V_{IHZ}$ SR	2.7	–	3.6	V	
Differential input sensitivity	$V_{DIS}$ CC	0.2	–	–	V	
Differential common mode range	$V_{CM}$ CC	0.8	–	2.5	V	
Output low voltage	$V_{OL}$ CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	$V_{OH}$ CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	$R_{PUI}$ CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	$R_{PUA}$ CC	1 425	–	3 090	Ohm	
Input impedance DP, DM	$Z_{INP}$ CC	300	–	–	kOhm	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DM	$Z_{DRV}$ CC	28	–	44	Ohm	

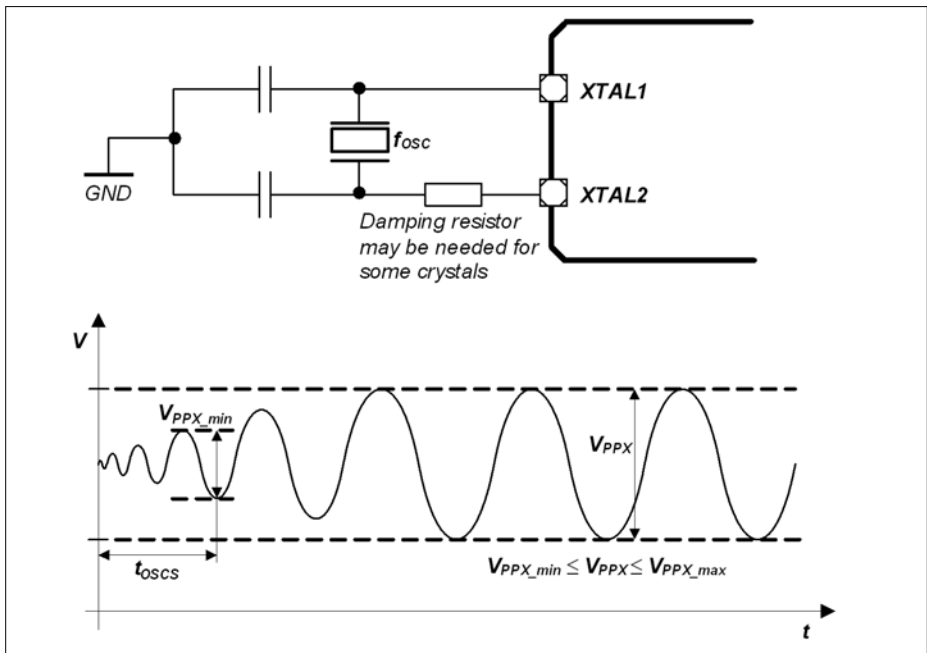
1) Measured at A-connector with 1.5 kOhm  $\pm$  5% to 3.3 V  $\pm$  0.3 V connected to USB\_DP or USB\_DM and at B-connector with 15 kOhm  $\pm$  5% to ground connected to USB\_DP and USB\_DM.

### 3.2.9 Oscillator Pins

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The oscillator pins can be operated with an external crystal (see [Figure 21](#)) or in direct input mode (see [Figure 22](#)).



**Figure 21 Oscillator in Crystal Mode**

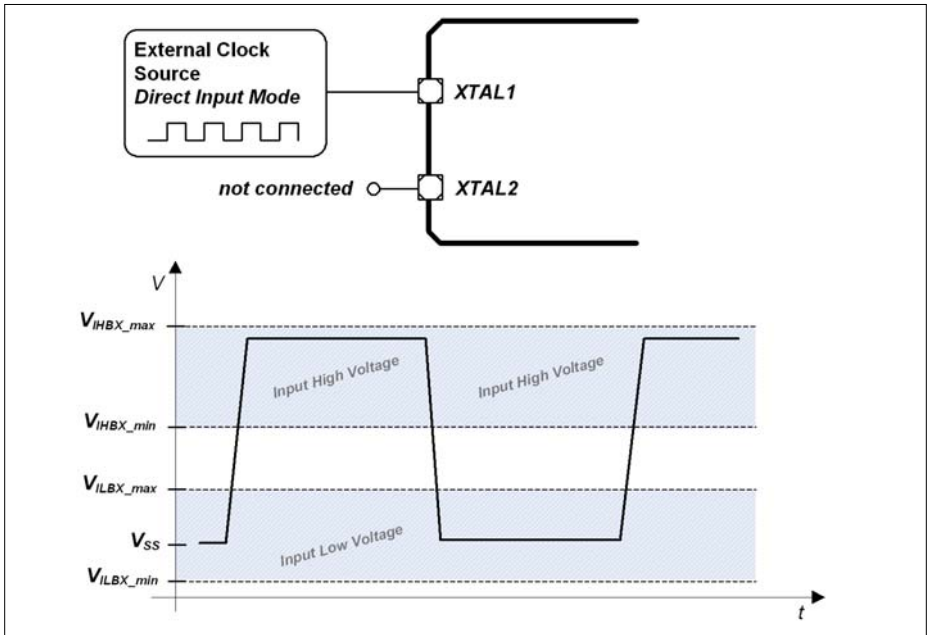


Figure 22 Oscillator in Direct Input Mode

**Table 36 OSC\_XTAL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{\text{OSC}}$ SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time <sup>1)2)</sup>	$t_{\text{OSCS}}$ CC	–	–	10	ms	
Input voltage at XTAL1	$V_{\text{IX}}$ SR	-0.5	–	$V_{\text{DDP}} + 0.5$	V	
Input amplitude (peak-to-peak) at XTAL1 <sup>2)3)</sup>	$V_{\text{PPX}}$ SR	$0.4 \times V_{\text{DDP}}$	–	$V_{\text{DDP}} + 1.0$	V	
Input high voltage at XTAL1 <sup>4)</sup>	$V_{\text{IHBX}}$ SR	1.0	–	$V_{\text{DDP}} + 0.5$	V	
Input low voltage at XTAL1 <sup>4)</sup>	$V_{\text{ILBX}}$ SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	$I_{\text{ILX1}}$ CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$

1)  $t_{\text{OSCS}}$  is defined from the moment the oscillator is enabled with SCU\_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of  $0.4 \times V_{\text{DDP}}$ .

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

**Table 37 RTC\_XTAL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{OSC}$ SR	–	32.768	–	kHz	
Oscillator start-up time <sup>1)2)3)</sup>	$t_{OSCS}$ CC	–	–	5	s	
Input voltage at RTC_XTAL1	$V_{IX}$ SR	-0.3	–	$V_{BAT} + 0.3$	V	
Input amplitude (peak-to-peak) at RTC_XTAL1 <sup>2)4)</sup>	$V_{PPX}$ SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1 <sup>5)</sup>	$V_{IHBX}$ SR	$0.6 \times V_{BAT}$	–	$V_{BAT} + 0.3$	V	
Input low voltage at RTC_XTAL1 <sup>5)</sup>	$V_{ILBX}$ SR	-0.3	–	$0.36 \times V_{BAT}$	V	
Input Hysteresis for RTC_XTAL1 <sup>3)6)</sup>	$V_{HYSX}$ CC	$0.1 \times V_{BAT}$		–	V	$3.0 \text{ V} \leq V_{BAT} < 3.6 \text{ V}$
		$0.03 \times V_{BAT}$		–	V	$V_{BAT} < 3.0 \text{ V}$
Input leakage current at RTC_XTAL1	$I_{ILX1}$ CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{IX} \leq V_{BAT}$

- 1)  $t_{OSCS}$  is defined from the moment the oscillator is enabled by the user with SCU\_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC\_XTAL1 of 400 mV.
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) For a reliable start of the oscillation in crystal mode it is required that  $V_{BAT} \geq 3.0 \text{ V}$ . A running oscillation is maintained across the full  $V_{BAT}$  voltage range.
- 4) If the shaper unit is enabled and not bypassed.
- 5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.
- 6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

### 3.2.10 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

If not stated otherwise, the operating conditions for the parameters in the following table are:

$$V_{DDP} = 3.3 \text{ V}, T_A = 25 \text{ }^\circ\text{C}$$

**Table 38 Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Active supply current <sup>1)</sup> Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPA}$ CC	-	80	-	mA	80 / 80 / 80
		-	75	-		80 / 40 / 40
		-	73	-		40 / 40 / 80
		-	59	-		24 / 24 / 24
		-	50	-		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPA}$ CC	-	24	-	mA	80 / 80 / 80
		-	19	-		80 / 40 / 40
Active supply current <sup>2)</sup> Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH}$ in MHz	$I_{DDPA}$ CC	-	63	-	mA	80 / 80 / 80
		-	62	-		80 / 40 / 40
		-	60	-		40 / 40 / 80
		-	54	-		24 / 24 / 24
		-	50	-		1 / 1 / 1

**Electrical Parameters**
**Table 38 Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current <sup>3)</sup> Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPS}$ CC	-	76	-	mA	80 / 80 / 80
		-	73	-		80 / 40 / 40
		-	70	-		40 / 40 / 80
		-	56	-		24 / 24 / 24
		-	47	-		1 / 1 / 1
		-	46	-		100 / 100 / 100
$f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz	$I_{DDPS}$ CC	-	59	-	mA	80 / 80 / 80
		-	58	-		80 / 40 / 40
		-	57	-		40 / 40 / 80
		-	51	-		24 / 24 / 24
		-	46	-		1 / 1 / 1
		-	46	-		100 / 100 / 100
Deep Sleep supply current <sup>5)</sup> Flash in Sleep mode Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPD}$ CC	-	6.9	-	mA	24 / 24 / 24
		-	4.3	-		4 / 4 / 4
		-	3.8	-		1 / 1 / 1
		-	4.5	-		100 / 100 / 100 <sup>6)</sup>
$f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz	$I_{DDPD}$ CC	-	6.9	-	mA	24 / 24 / 24
		-	4.3	-		4 / 4 / 4
		-	3.8	-		1 / 1 / 1
Hibernate supply current RTC on <sup>7)</sup>	$I_{DDPH}$ CC	-	10.8	-	$\mu$ A	$V_{BAT} = 3.3$ V
		-	8.0	-		$V_{BAT} = 2.4$ V
		-	6.8	-		$V_{BAT} = 2.0$ V
Hibernate supply current RTC off <sup>8)</sup>	$I_{DDPH}$ CC	-	10.3	-	$\mu$ A	$V_{BAT} = 3.3$ V
		-	7.5	-		$V_{BAT} = 2.4$ V
		-	6.3	-		$V_{BAT} = 2.0$ V
Worst case active supply current <sup>9)</sup>	$I_{DDPA}$ CC	-	-	140 <sup>10)</sup>	mA	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
$V_{DDA}$ power supply current	$I_{DDA}$ CC	-	-	- <sup>11)</sup>	mA	
$I_{DDP}$ current at PORST Low	$I_{DDP\_PORST}$ CC	-	-	24	mA	$V_{DDP} = 3.6$ V, $T_J = 150$ °C

**Table 38 Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Dissipation	$P_{DISS}$ CC	–	–	1	W	$V_{DDP} = 3.6\text{ V}$ , $T_J = 150\text{ °C}$
Wake-up time from Sleep to Active mode	$t_{SSA}$ CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode		–	–	–	ms	Defined by the wake-up of the Flash module, see <a href="#">Section 3.2.11</a>
Wake-up time from Hibernate mode		–	–	–	ms	Wake-up via power-on reset event, see <a href="#">Section 3.3.2</a>

- 1) CPU executing code from Flash, all peripherals idle.
- 2) CPU executing code from Flash. USB and CCU clock off.
- 3) CPU in sleep, all peripherals idle, Flash in Active mode.
- 4) CPU in sleep, Flash in Active mode.
- 5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
- 6) To wake-up the Flash from its Sleep mode,  $f_{CPU} \geq 1\text{ MHz}$  is required.
- 7) OSC\_ULP operating with external crystal on RTC\_XTAL
- 8) OSC\_ULP off, Hibernate domain operating with OSC\_SI clock
- 9) Test Power Loop:  $f_{SYS} = 80\text{ MHz}$ , CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.  
The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
- 10)  $I_{DDP}$  decreases typically by 3.5 mA when  $f_{SYS}$  decreases by 10 MHz, at constant  $T_J$
- 11) Sum of currents of all active converters (ADC and DAC)

**Peripheral Idle Currents**

Test conditions:

- $f_{sys}$  and derived clocks at 80 MHz
- $V_{DDP} = 3.3\text{ V}$ ,  $T_a = 25\text{ °C}$
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU)
- no I/O activity
- the given values are a result of differential measurements with asserted and deasserted peripheral reset and enabled clock of the peripheral under test

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. E.g. no timer is running in the CCUs, no communication active in the USICs, etc.

**Table 39 Peripheral Idle Currents**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORTS USB FCE WDT POSIFx <sup>1)</sup>	$I_{PER\ CC}$	–	≤ 0.3	–	mA	
MultICAN ERU LEDTSCU0 CCU4x <sup>1)</sup> CCU8x <sup>1)</sup>		–	≤ 1.0	–		
DAC (digital) <sup>2)</sup>		–	1.3	–		
USICx		–	3.0	–		
VADC (digital) <sup>2)</sup>		–	4.5	–		
DMAx		–	6.0	–		

1) Enabling the  $f_{CCU}$  clock for the POSIFx/CCU4x/CCU8x modules adds approximately  $I_{PER} = 1.8\text{ mA}$ , disregarding which and how many of those peripherals are enabled.

2) The current consumption of the analog components are given in the dedicated Data Sheet sections of the respective peripheral.

### 3.2.11 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 40 Flash Memory Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	$t_{ERP}$ CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	$t_{ERP}$ CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	$t_{ERP}$ CC	–	0.3	0.4	s	
Program time per page <sup>1)</sup>	$t_{PRP}$ CC	–	5.5	11	ms	
Erase suspend delay	$t_{FL\_ErSusp}$ CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	μs	
Wake-up time	$t_{WU}$ CC	–	–	270	μs	
Read access time	$t_a$ CC	20	–	–	ns	For operation with $1/f_{CPU} < t_a$ wait states must be configured <sup>2)</sup>
Data Retention Time, Physical Sector <sup>3)4)</sup>	$t_{RET}$ CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector <sup>3)4)</sup>	$t_{RETL}$ CC	20	–	–	years	Max. 100 erase/program cycles

**Table 40 Flash Memory Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Retention Time, User Configuration Block (UCB) <sup>3)4)</sup>	$t_{RTU}$ CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	$N_{EPS4}$ CC	10000	–	–	cycles	BA-marking devices only! Cycling distributed over life time <sup>5)</sup>

- 1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.
- 2) The following formula applies to the wait state configuration:  $FCON.WSPFLASH \times (1 / f_{CPU}) \geq t_a$ .
- 3) Storage and inactive time included.
- 4) Values given are valid for an average weighted junction temperature of  $T_J = 110^\circ\text{C}$ .
- 5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

### 3.3 AC Parameters

#### 3.3.1 Testing Waveforms

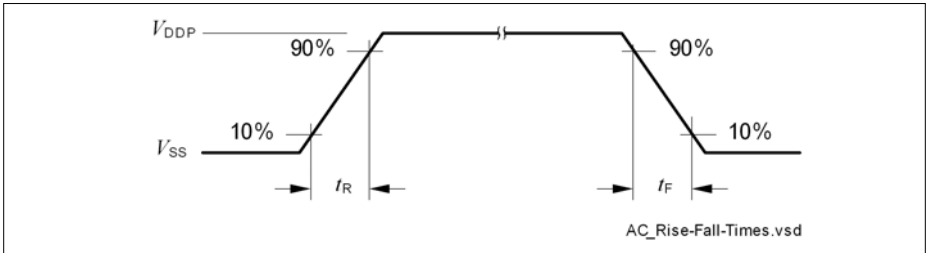


Figure 23 Rise/Fall Time Parameters

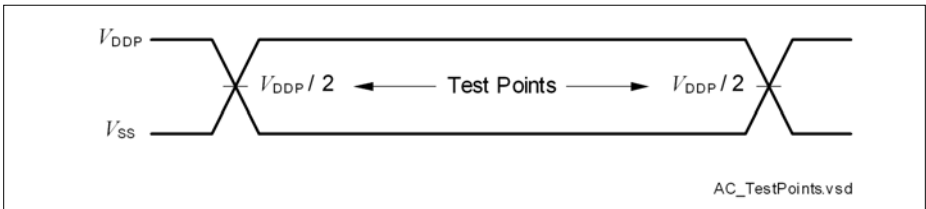


Figure 24 Testing Waveform, Output Delay

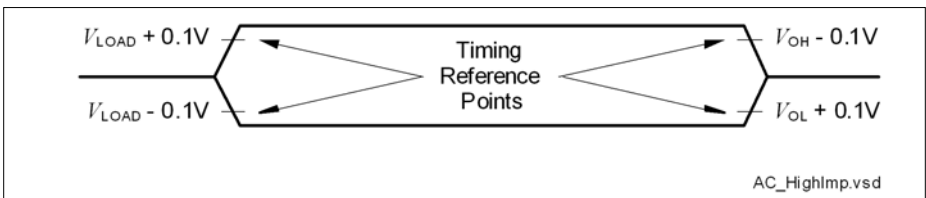
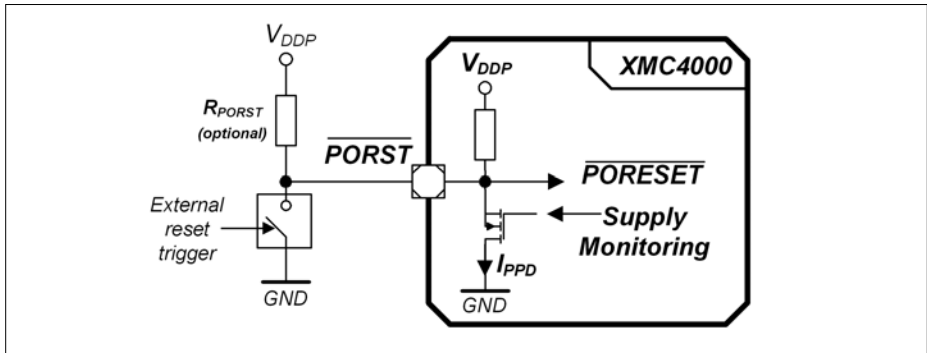


Figure 25 Testing Waveform, Output High Impedance

### 3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$  is always asserted when  $V_{\text{DDP}}$  and/or  $V_{\text{DDC}}$  violate the respective thresholds.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*



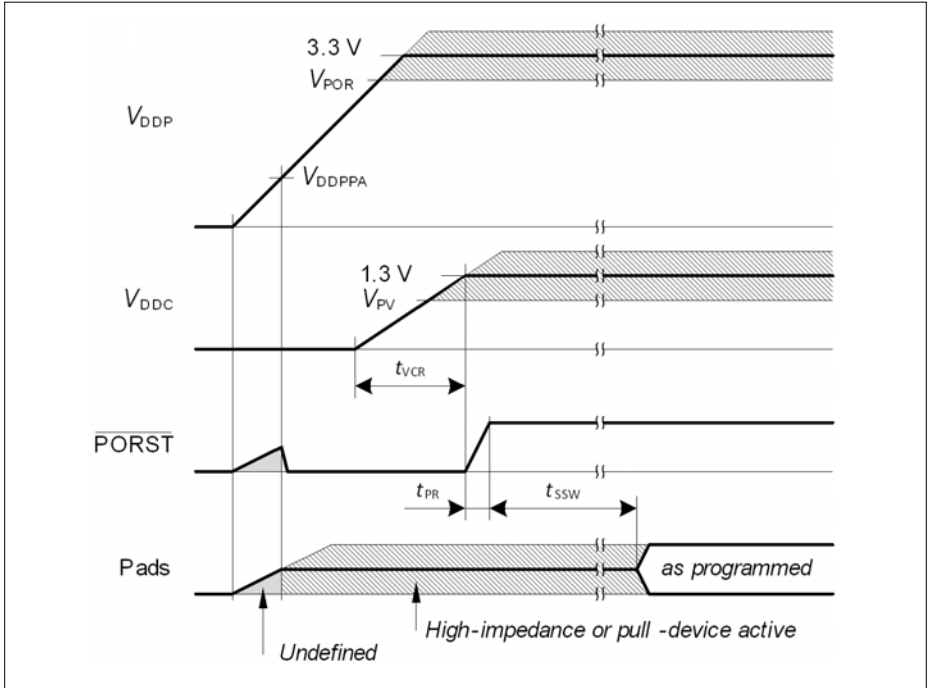
**Figure 26**  $\overline{\text{PORST}}$  Circuit

**Table 41** Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	$V_{\text{POR}}$ CC	2.79 <sup>1)</sup>	–	3.05 <sup>2)</sup>	V	3)
Core supply voltage reset threshold	$V_{\text{PV}}$ CC	–	–	1.17	V	
$V_{\text{DDP}}$ voltage to ensure defined pad states	$V_{\text{DDPPA}}$ CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	$t_{\text{PR}}$ SR	–	–	2	$\mu\text{s}$	
Startup time from power-on reset with code execution from Flash	$t_{\text{SSW}}$ CC	–	2.5	3.5	ms	Time to the first user code instruction
$V_{\text{DDC}}$ ramp up time	$t_{\text{VCR}}$ CC	–	550	–	$\mu\text{s}$	Ramp up after power-on or after a reset triggered by a violation of $V_{\text{POR}}$ or $V_{\text{PV}}$

1) Minimum threshold for reset assertion.

- 2) Maximum threshold for reset deassertion.
- 3) The  $V_{DDP}$  monitoring has a typical hysteresis of  $V_{PORHYS} = 180\text{ mV}$ .



**Figure 27 Power-Up Behavior**

### 3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency  $f_{CPU}$ . Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 42 Power Sequencing Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	$\Delta I_{PLS}$ SR	-	-	50	mA	Load increase on $V_{DDP}$ $\Delta t \leq 10$ ns
Negative Load Step Current	$\Delta I_{NLS}$ SR	-	-	150	mA	Load decrease on $V_{DDP}$ $\Delta t \leq 10$ ns
$V_{DDC}$ Voltage Over- / Undershoot from Load Step	$\Delta V_{LS}$ CC	-	-	$\pm 100$	mV	For maximum positive or negative load step
Positive Load Step Settling Time	$t_{PLSS}$ SR	50	-	-	$\mu$ s	
Negative Load Step Settling Time	$t_{NLSS}$ SR	100	-	-	$\mu$ s	
External Buffer Capacitor on $V_{DDC}$	$C_{EXT}$ SR	3	4.7	6	$\mu$ F	In addition $C = 100$ nF capacitor on each $V_{DDC}$ pin

### Positive Load Step Examples

System assumptions:

$f_{CPU} = f_{SYS}$ , target frequency  $f_{CPU} = 80$  MHz, main PLL  $f_{VCO} = 480$  MHz, stepping done by K2 divider,  $t_{PLSS}$  between individual steps:

24 MHz - 48 MHz - 80 MHz (K2 steps 20 - 10 - 6)

24 MHz - 60 MHz - 80 MHz (K2 steps 20 - 8 - 6)

### 3.3.4 Phase Locked Loop (PLL) Characteristics

#### Main and USB PLL

**Table 43 PLL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	$D_P$ CC	–	–	±5	ns	accumulated over 300 cycles $f_{SYS} = 80$ MHz
Duty Cycle <sup>1)</sup>	$D_{DC}$ CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	$f_{REF}$ CC	4	–	16	MHz	
VCO frequency range	$f_{VCO}$ CC	260	–	520	MHz	
PLL lock-in time	$t_L$ CC	–	–	400	μs	

1) 50% for even K2 divider values,  $50 \pm (10/K2)$  for odd K2 divider values.

### 3.3.5 Internal Clock Source Characteristics

#### Fast Internal Clock Source

**Table 44 Fast Internal Clock Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{\text{OFINC CC}}$	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	$\Delta f_{\text{OFI CC}}$	-0.5	–	0.5	%	automatic calibration <sup>1)2)</sup>
		-15	–	15	%	factory calibration, $V_{\text{DDP}} = 3.3 \text{ V}$
		-25	–	25	%	no calibration, $V_{\text{DDP}} = 3.3 \text{ V}$
		-7	–	7	%	Variation over voltage range <sup>3)</sup> $3.13 \text{ V} \leq V_{\text{DDP}} \leq 3.63 \text{ V}$
Start-up time	$t_{\text{OFIS CC}}$	–	50	–	$\mu\text{s}$	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the  $V_{\text{DDP}}$  supply voltage.

3) Deviations from the nominal  $V_{\text{DDP}}$  voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

**Slow Internal Clock Source**
**Table 45 Slow Internal Clock Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{OSI}$ CC	–	32.768	–	kHz	
Accuracy	$\Delta f_{OSI}$ CC	-4	–	4	%	$V_{BAT} = \text{const.}$ $0\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
		-5	–	5	%	$V_{BAT} = \text{const.}$ $T_A < 0\text{ }^{\circ}\text{C}$ or $T_A > 85\text{ }^{\circ}\text{C}$
		-5	–	5	%	$2.4\text{ V} \leq V_{BAT}$ , $T_A = 25\text{ }^{\circ}\text{C}$
		-10	–	10	%	$1.95\text{ V} \leq V_{BAT} < 2.4\text{ V}$ , $T_A = 25\text{ }^{\circ}\text{C}$
Start-up time	$t_{OSIS}$ CC	–	50	–	$\mu\text{s}$	

### 3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

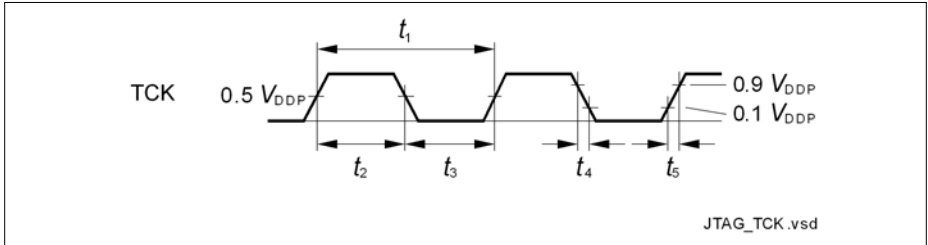
*Note: Operating conditions apply.*

**Table 46 JTAG Interface Timing Parameters**

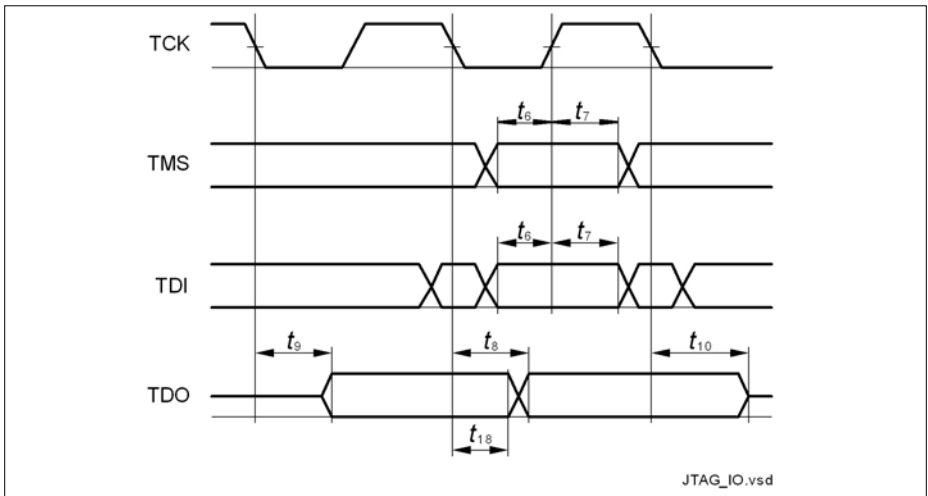
Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	$t_1$	SR	30	–	–	ns	For $C_L = 20$ pF on TDO
TCK clock period	$t_1$	SR	40	–	–	ns	For $C_L = 50$ pF on TDO
TCK high time	$t_2$	SR	10	–	–	ns	
TCK low time	$t_3$	SR	10	–	–	ns	
TCK clock rise time	$t_4$	SR	–	–	4	ns	
TCK clock fall time	$t_5$	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	$t_6$	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	$t_7$	SR	6	–	–	ns	
TDO valid after TCK falling edge <sup>1)</sup> (propagation delay)	$t_8$	CC	–	–	17	ns	$C_L = 50$ pF
			3	–	–	ns	$C_L = 20$ pF
TDO hold after TCK falling edge <sup>1)</sup>	$t_{18}$	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge <sup>1)2)</sup>	$t_9$	CC	–	–	14	ns	$C_L = 50$ pF
TDO valid to high imped. from TCK falling edge <sup>1)</sup>	$t_{10}$	CC	–	–	13.5	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.



**Figure 28 Test Clock Timing (TCK)**



**Figure 29 JTAG Timing**

### 3.3.7 Serial Wire Debug Port (SW-DP) Timing

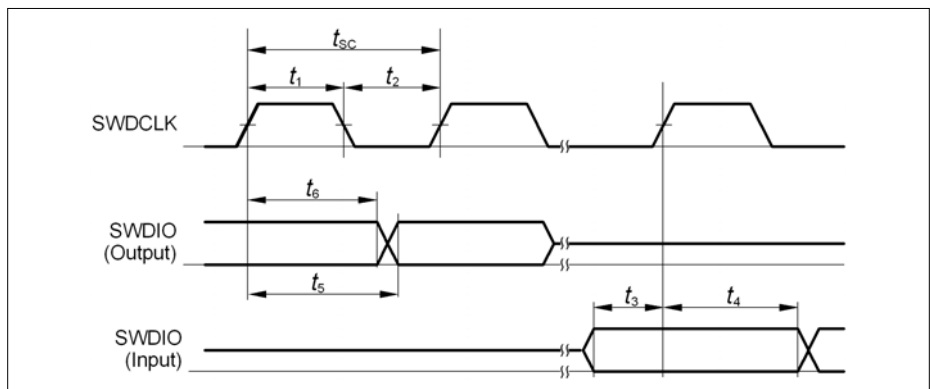
The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

**Table 47 SWD Interface Timing Parameters (Operating Conditions apply)**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	$t_{SC}$	SR	25	–	–	ns	$C_L = 30$ pF
			40	–	–	ns	$C_L = 50$ pF
SWDCLK high time	$t_1$	SR	10	–	500000	ns	
SWDCLK low time	$t_2$	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	$t_3$	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	$t_4$	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	$t_5$	CC	–	–	17	ns	$C_L = 50$ pF
			–	–	13	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	$t_6$	CC	3	–	–	ns	



**Figure 30 SWD Timing**

### 3.3.8 Peripheral Timing

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

#### 3.3.8.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: Operating Conditions apply.*

**Table 48 USIC SSC Master Mode Timing**

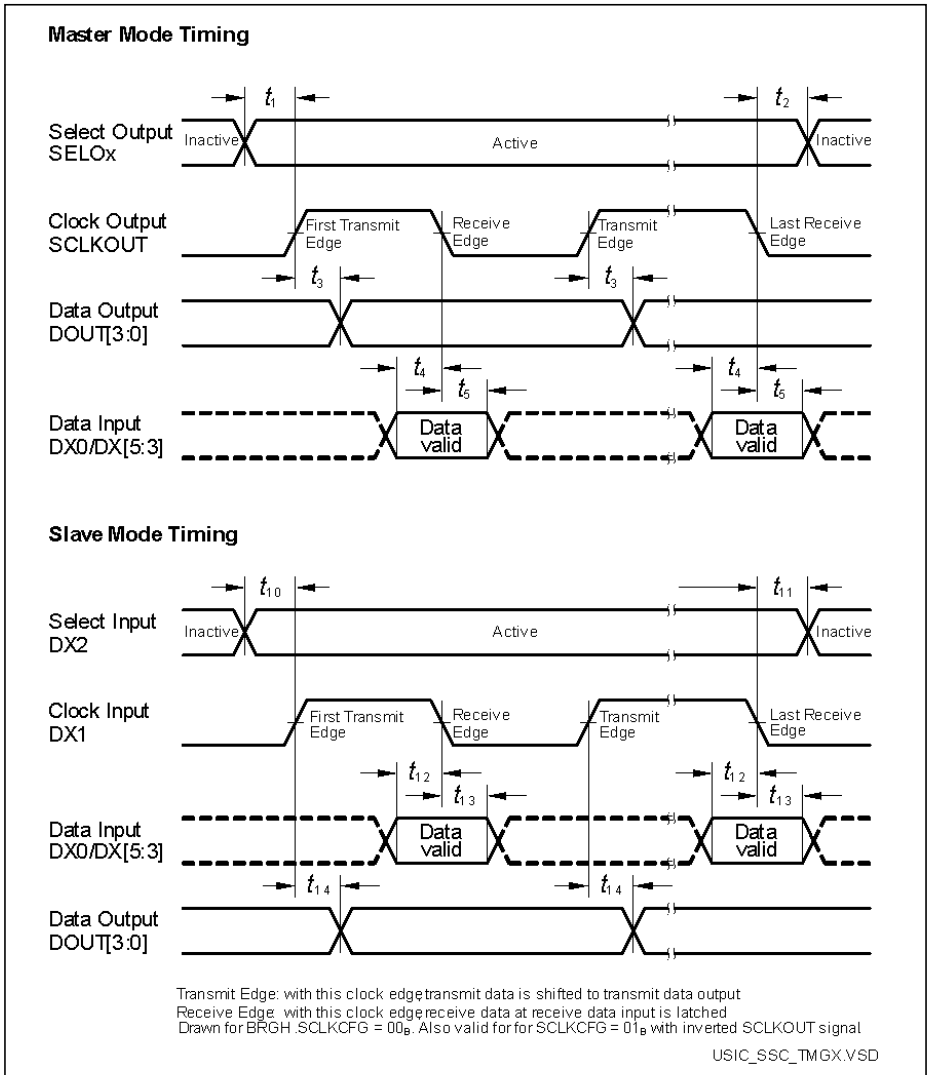
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	$t_{CLK}$ CC	40	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	$t_1$ CC	$t_{SYS} - 6.5^{1)}$	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	$t_2$ CC	$t_{SYS} - 8.5^{1)}$	–	–	ns	
Data output DOUT[3:0] valid time	$t_3$ CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	$t_4$ SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	$t_5$ SR	1	–	–	ns	

1)  $t_{SYS} = 1 / f_{PB}$

**Table 49 USIC SSC Slave Mode Timing**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	$t_{CLK}$	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge <sup>1)</sup>	$t_{10}$	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge <sup>1)</sup>	$t_{11}$	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge <sup>1)</sup>	$t_{12}$	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge <sup>1)</sup>	$t_{13}$	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	$t_{14}$	CC	0	–	24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).



**Figure 31 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

### 3.3.8.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

*Note: Operating Conditions apply.*

**Table 50 USIC IIC Standard Mode Timing<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$ CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	$t_2$ CC/SR	-	-	1000	ns	
Data hold time	$t_3$ CC/SR	0	-	-	μs	
Data set-up time	$t_4$ CC/SR	250	-	-	ns	
LOW period of SCL clock	$t_5$ CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	$t_6$ CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	$t_7$ CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	$t_8$ CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	$t_9$ CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	$t_{10}$ CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	

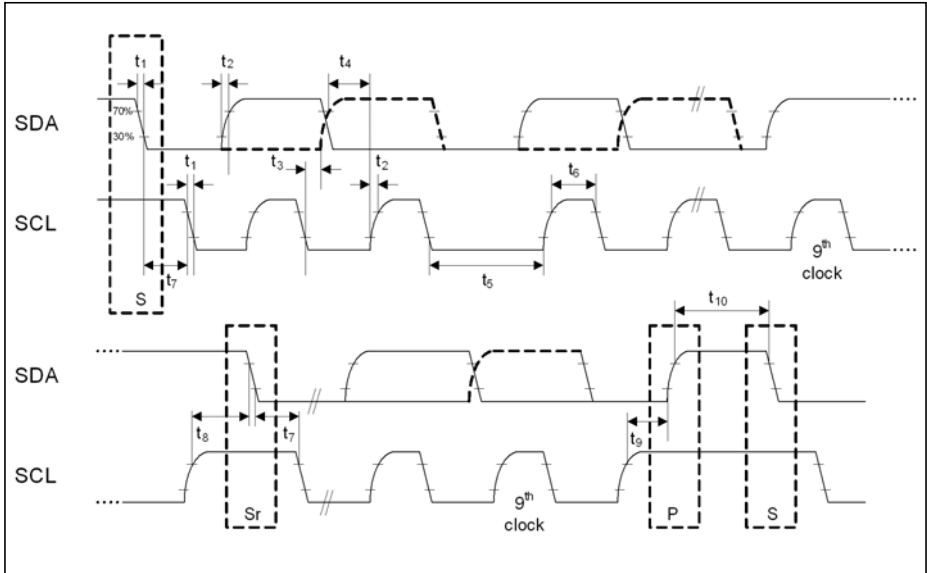
1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

**Table 51 USIC IIC Fast Mode Timing<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$ CC/SR	20 + $0.1 \cdot C_b$ <sup>2)</sup>	-	300	ns	
Rise time of both SDA and SCL	$t_2$ CC/SR	20 + $0.1 \cdot C_b$ <sup>2)</sup>	-	300	ns	
Data hold time	$t_3$ CC/SR	0	-	-	$\mu$ s	
Data set-up time	$t_4$ CC/SR	100	-	-	ns	
LOW period of SCL clock	$t_5$ CC/SR	1.3	-	-	$\mu$ s	
HIGH period of SCL clock	$t_6$ CC/SR	0.6	-	-	$\mu$ s	
Hold time for (repeated) START condition	$t_7$ CC/SR	0.6	-	-	$\mu$ s	
Set-up time for repeated START condition	$t_8$ CC/SR	0.6	-	-	$\mu$ s	
Set-up time for STOP condition	$t_9$ CC/SR	0.6	-	-	$\mu$ s	
Bus free time between a STOP and START condition	$t_{10}$ CC/SR	1.3	-	-	$\mu$ s	
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2)  $C_b$  refers to the total capacitance of one bus line in pF.



**Figure 32 USIC IIC Stand and Fast Mode Timing**

### 3.3.8.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 52 USIC IIS Master Transmitter Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_1$ CC	33.3	–	–	ns	
Clock high time	$t_2$ CC	0.35 x $t_{1min}$	–	–	ns	
Clock low time	$t_3$ CC	0.35 x $t_{1min}$	–	–	ns	
Hold time	$t_4$ CC	0	–	–	ns	
Clock rise time	$t_5$ CC	–	–	0.15 x $t_{1min}$	ns	

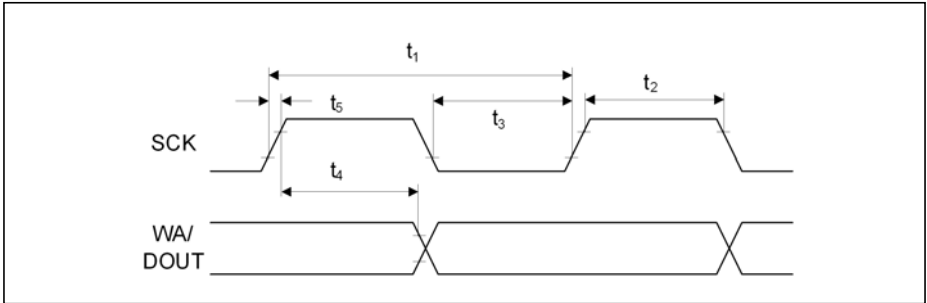


Figure 33 USIC IIS Master Transmitter Timing

Table 53 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_6$ SR	66.6	–	–	ns	
Clock high time	$t_7$ SR	$0.35 \times t_{6min}$	–	–	ns	
Clock low time	$t_8$ SR	$0.35 \times t_{6min}$	–	–	ns	
Set-up time	$t_9$ SR	$0.2 \times t_{6min}$	–	–	ns	
Hold time	$t_{10}$ SR	0	–	–	ns	

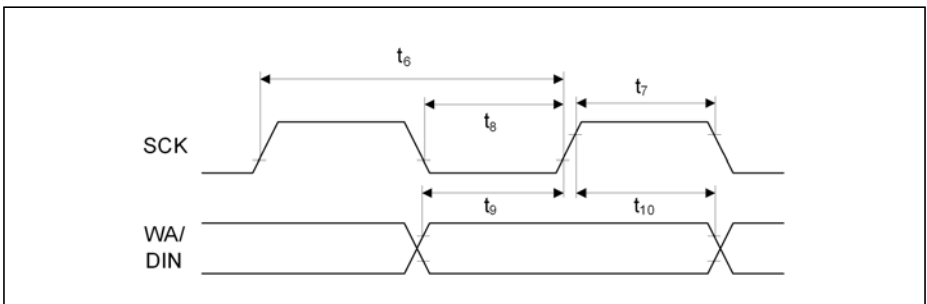


Figure 34 USIC IIS Slave Receiver Timing

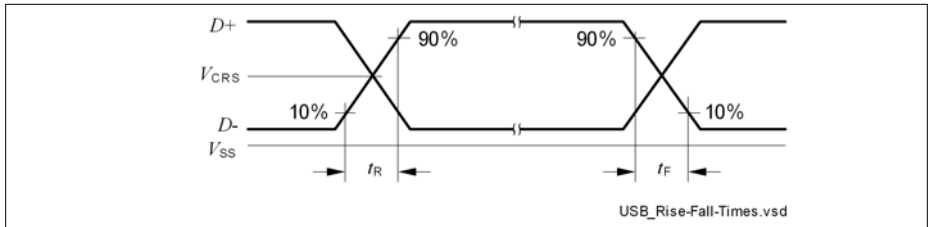
### 3.3.9 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification. High-Speed Mode is not supported.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 54 USB Timing Parameters** (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	$t_R$	CC	4	–	20	ns	$C_L = 50$ pF
Fall time	$t_F$	CC	4	–	20	ns	$C_L = 50$ pF
Rise/Fall time matching	$t_R/t_F$	CC	90	–	111.11	%	$C_L = 50$ pF
Crossover voltage	$V_{CRS}$	CC	1.3	–	2.0	V	$C_L = 50$ pF



**Figure 35 USB Signal Timing**

## 4 Package and Reliability

The XMC4[12]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

### 4.1 Package Parameters

**Table 55** provides the thermal characteristics of the packages used in XMC4[12]00. The availability of different packages for different markings is listed in **Table 2**.

**Table 55 Thermal Characteristics of the Packages**

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	5.7 × 5.7	mm	PG-TQFP-64-19 PG-TQFP-64-21
		-	5.2 × 5.2	mm	PG-VQFN-48-71
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	23.4	K/W	PG-TQFP-64-19 <sup>1)</sup> PG-TQFP-64-21 <sup>1)</sup>
		-	34.8	K/W	PG-VQFN-48-71 <sup>1)</sup>
Package thickness 1.0±0.05 mm	-	-	1.2 Max	mm	PG-TQFP-64-19 PG-TQFP-64-21

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

*Note: For electrical reasons, it is required to connect the exposed pad to the board ground  $V_{SS}$ , independent of EMC and thermal requirements.*

### 4.1.1 Thermal Considerations

When operating the XMC4[12]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance  $R_{\Theta JA}$ ” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by  $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$$P_{INT} = V_{DDP} \times I_{DDP} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

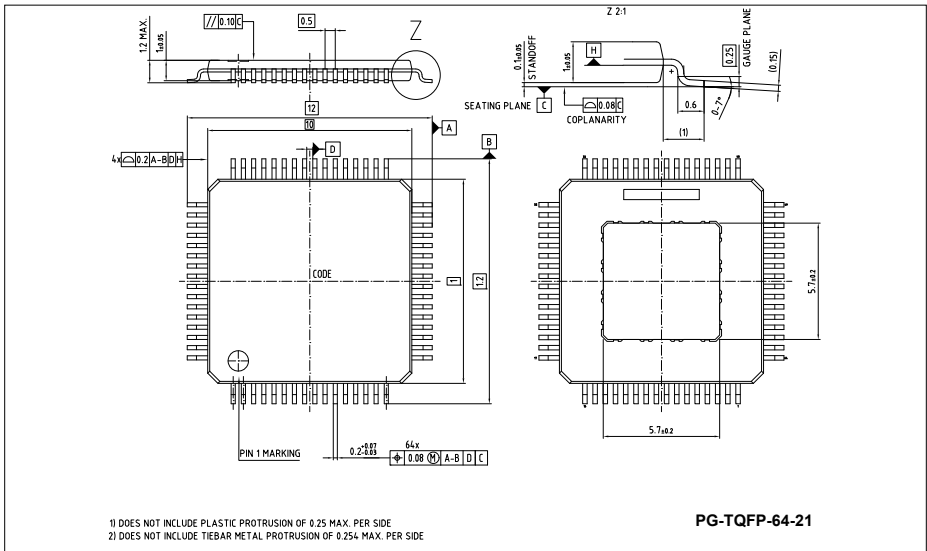
$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

The dynamic external power consumption caused by the output drivers ( $P_{IODYN}$ ) depends on the capacitive load connected to the respective pins and their switching frequencies.

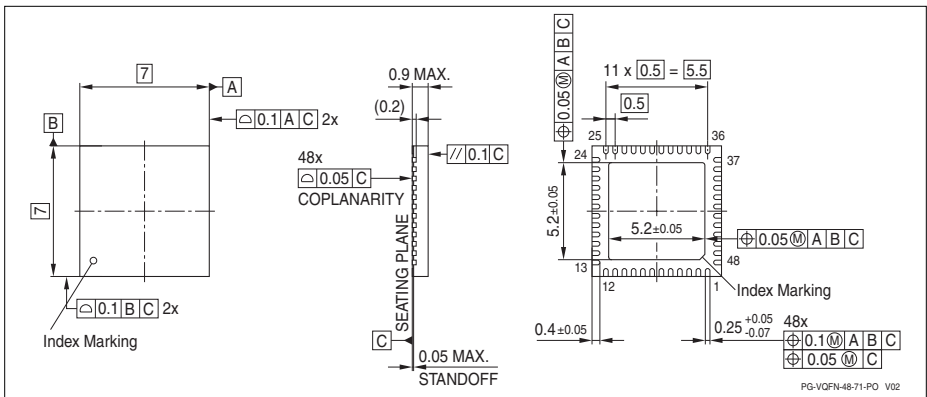
If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce  $V_{DDP}$ , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers





**Figure 37 PG-TQFP-64-21 (Plastic Green Thin Profile Quad Flat Package)**



**Figure 38 PG-VQFN-48-71 (Plastic Green Very Thin Profile Flat Non Ledged Package)**

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: <http://www.infineon.com/packages>

## 5 Quality Declarations

The qualification of the XMC4[12]00 is executed according to the JEDEC standard JESD47H.

*Note: For automotive applications refer to the Infineon automotive microcontrollers.*

**Table 56 Quality Parameters**



Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	$t_{OP}$ CC	20	–	–	a	$T_J \leq 109^\circ\text{C}$ , device permanent on
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM}$ SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	$V_{CDM}$ SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	$MSL$ CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	$T_{SDR}$ SR	–	–	260	$^\circ\text{C}$	Profile according to JEDEC J-STD-020D

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