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THE DATASHEET OF

SC18IM700IPW/S8HP

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SC18IM700

Master I²C-bus controller with UART interface

Rev. 4 — 9 October 2019 Product data sheet

1. General description

The SC18IM700 is designed to serve as an interface between the standard UART port of a microcontroller or microprocessor and the serial I²C-bus; this allows the microcontroller or microprocessor to communicate directly with other I²C-bus devices. The SC18IM700 can operate as an I²C-bus master. The SC18IM700 controls all the I²C-bus specific sequences, protocol, arbitration and timing. The host communicates with SC18IM700 with ASCII messages protocol; this makes the control sequences from the host to the SC18IM700 become very simple.

2. Features and benefits

- UART host interface
- I²C-bus controller
- Eight programmable I/O pins
- High-speed UART: baud rate up to 460.8 kbit/s
- High-speed I²C-bus: 400 kbit/s
- 16-byte TX FIFO
- 16-byte RX FIFO
- Programmable baud rate generator
- 2.4 V and 3.6 V operation
- Sleep mode (power-down)
- UART message format resembles I²C-bus transaction format
- I²C-bus master functions
- Multi-master capability
- 5 V tolerance on the input pins
- 8 N 1 UART format (8 data bits, no parity bit, 1 stop bit)
- Available in very small TSSOP16 package

3. Applications

- Enable I²C-bus master support in a system
- I²C-bus instrumentation and control
- Industrial control
- Medical equipment
- Cellular telephones
- Handheld computers

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SC18IM700IPW/S8	IM700 B	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SC18IM700IPW/S8	SC18IM700IPW/S8HP[1]	TSSOP16	REEL 13" Q4/T2 *STANDARD MARK SMD	2500	T_{amb} = –40 °C to +85 °C

[1] NXP plans to supply the /S8 device with an expected discontinuation in the 2024-2025 timeframe, but in the meantime, Failure Analysis for /S8 devices will consist of Automated Test Equipment (ATE) and electrical overstress verification along with package and wire bond validation only. Detailed device failure analysis will not be available; refer to CIN 201708035I.

5. Block diagram

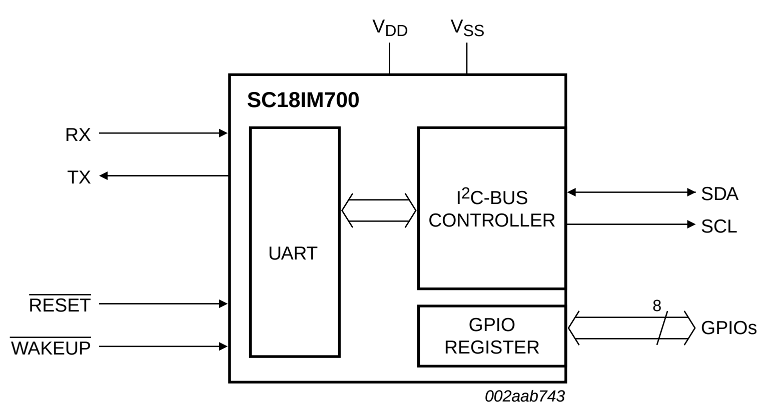


Fig 1. Block diagram of SC18IM700

6. Pinning information

6.1 Pinning

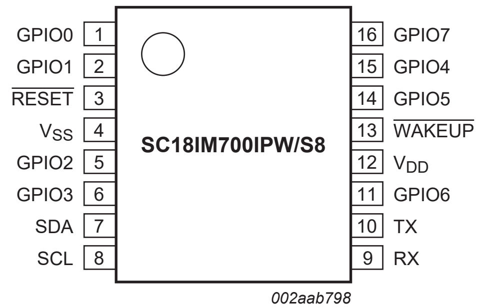


Fig 2. Pin configuration for TSSOP16

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
GPIO0	1	I/O	programmable I/O pin
GPIO1	2	I/O	programmable I/O pin
$\overline{\text{RESET}}$	3	I	hardware reset input
V_{SS}	4	-	ground
GPIO2	5	I/O	programmable I/O pin
GPIO3	6	I/O	programmable I/O pin
SDA	7	I/O	I²C-bus data pin
SCL	8	O	I²C-bus clock output
RX	9	I	RS-232 receive input
TX	10	O	RS-232 transmit input
GPIO6	11	I/O	programmable I/O pin
V_{DD}	12	-	power supply
$\overline{\text{WAKEUP}}$	13	I	Wake up SC18IM700 from Power-down mode. Pulling LOW by the host to wake up the device. A 1 kΩ resistor must be connected between V_{DD} and this pin.
GPIO5	14	I/O	programmable I/O pin
GPIO4	15	O	programmable I/O pin
GPIO7	16	O	programmable I/O pin

7. Functional description

The SC18IM700 is a bridge between a UART port and I²C-bus. The UART interface consists of a full-functional advanced UART. The UART communicates with the host through the TX and RX pins. The serial data format is fixed: one start bit, 8 data bits, and one stop bit. After reset the baud rate defaults to 9600 bit/s, and can be changed through the Baud Rate Generator (BRG) registers.

After a power-up sequence or a hardware reset, the SC18IM700 will send two continuous bytes to the host to indicate a start-up condition. These two bytes are 0x4F and 0x4B; 'OK' in ASCII.

7.1 UART message format

The host initiates an I²C-bus data transfer, reads from and writes to SC18IM700 internal registers through a series of ASCII commands. Table 4 lists the ASCII commands supported by SC18IM700, and also their hexadecimal value representation. Unrecognized commands are ignored by the device.

To prevent the host from handing the SC18IM700 due to an unfinished command sequence, the SC18IM700 has a time-out feature. The delay between any two bytes of data coming from the host should be less than 655 ms. If this condition is not met, the SC18IM700 will time-out and clear the receive buffer. The SC18IM700 then starts to wait for the next command from the host.

Table 4. ASCII commands supported by SC18IM700

ASCII command	Hex value	Command function
S	0x53	I²C-bus START
P	0x50	I²C-bus STOP
R	0x52	read SC18IM700 internal register
W	0x57	write to SC18IM700 internal register
I	0x49	read GPIO port
O	0x4F	write to GPIO port
Z	0x5A	power down

7.1.1 Write N bytes to slave device

The host issues the write command by sending an S character followed by an I²C-bus slave device address, the total number of bytes to be sent, and I²C-bus data which begins with the first byte (DATA 0) and ends with the last byte (DATA N). The frame is then terminated with a P character. Once the host issues this command, the SC18IM700 will access the I²C-bus slave device and start sending the I²C-bus data bytes.

Note that the second byte sent is the I²C-bus device slave address. The least significant bit (W) of this byte must be set to 0 to indicate this is an I²C-bus write command.

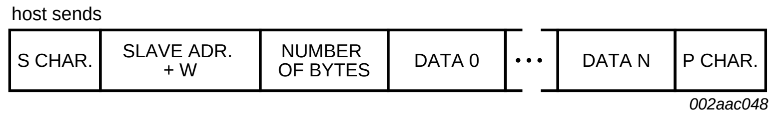


Fig 3. Write N bytes to slave device

7.1.2 Read N byte from slave device

The host issues the read command by sending an S character followed by an I²C-bus slave device address, and the total number of bytes to be read from the addressed I²C-bus slave. The frame is then terminated with a P character. Once the host issues this command, the SC18IM700 will access the I²C-bus slave device, get the correct number of bytes from the addressed I²C-bus slave, and then return the data to the host.

Note that the second byte sent is the I²C-bus device slave address. The least significant bit (R) of this byte must be set to 1 to indicate this is an I²C-bus write command.

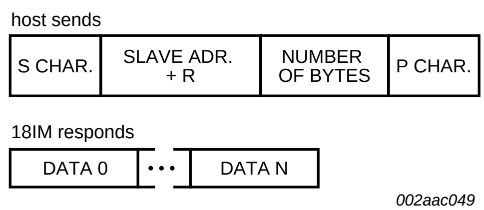


Fig 4. Read N byte from slave device

7.1.3 Write to 18IM internal register

The host issues the internal register write command by sending a W character followed by the register and data pair. Each register to be written must be followed by the data byte. The frame is then terminated with a P character.

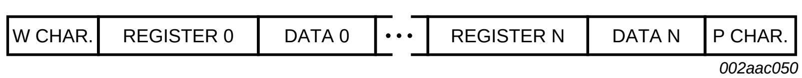


Fig 5. Write to 18IM internal register

Remark: Write and read from the internal 18IM register is processed immediately as soon as the intended register is determined by 18IM.

7.1.4 Read from 18IM internal register

The host issues the internal register read command by sending an R character followed by the registers to be read. The frame is then terminated with a P character.

Once the command is issued, SC18IM700 will access its internal registers and returns the contents of these registers to the host.

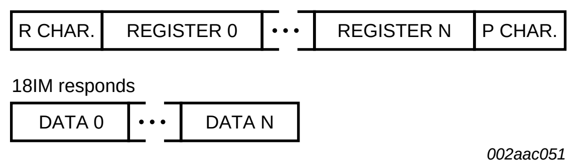


Fig 6. Read from 18IM internal register

7.1.5 Write to GPIO port

The host issues the output port write command by sending an O character followed by the data to be written to the output port. This command enables the host to quickly set any GPIO pins programmed as output without having to write to the SC18IM700 internal IOState register.

Fig 7. Write to output port

7.1.6 Read from GPIO port

The host issues the input port read command by sending an I character. This command enables the host to quickly read any GPIO pins programmed as input without having to read the SC18IM700 internal IOState register.

Once the command is issued, SC18IM700 will read its internal IOState register and returns its content to the host.

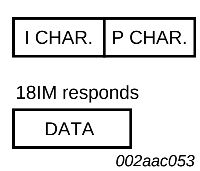


Fig 8. Read from output port

7.1.7 Repeated START: read after write

The SC18IM700 also supports 'read after write' command as specified in the NXP Semiconductors I²C-bus specification. This allows a read command to be sent after a write command without having to issue a STOP condition between the two commands.

The host issues a write command as normal, then immediately issues a read command without sending a STOP (P) character after the write command.

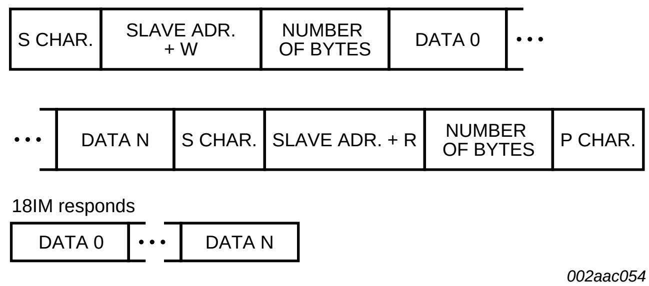


Fig 9. Repeated START: read after write

7.1.8 Repeated START: write after write

The SC18IM700 also supports 'write after write' command as specified in the NXP Semiconductors I²C-bus specification. This allows a write command to be sent after a write command without having to issue a STOP condition between the two commands.

The host issues a write command as normal, then immediately issues a second write command without sending a STOP (P) character after the first write command.

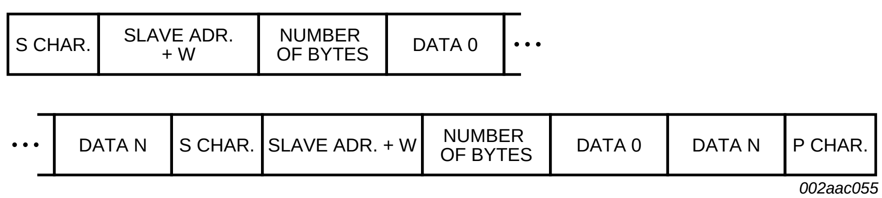


Fig 10. Repeated START: write after write

7.1.9 Power-down mode

The SC18IM700 can be placed in a low-power mode. In this mode the internal oscillator is stopped and SC18IM700 will no longer respond to the host messages. Enter the Power-down mode by sending the power-down character Z (0x5A) followed by the two defined bytes, which are 0x5A and followed by 0xA5. If the exact message is not received, the device will not enter the power-down state.

Upon entering the power-down state, SC18IM700 places the $\overline{\text{WAKEUP}}$ pin in a HIGH state. To have the device leave the power-down state, the $\overline{\text{WAKEUP}}$ pin should be brought LOW. A 1 kΩ resistor must be connected between the $\overline{\text{WAKEUP}}$ pin and V_{DD}.

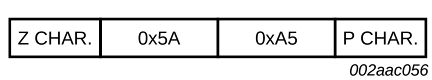


Fig 11. Power-down mode

8. I2C-bus serial interface

The I2C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

A typical I2C-bus configuration is shown in Figure 12. The SC18IM700 device provides a byte-oriented I2C-bus interface that supports data transfers up to 400 kHz.

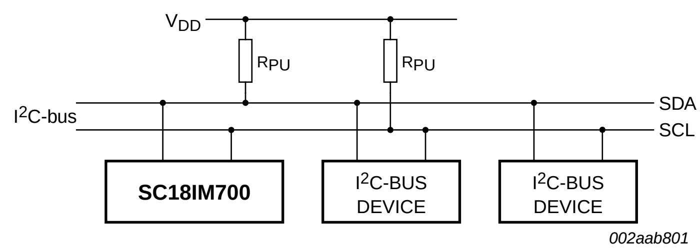


Fig 12. I2C-bus configuration

9. Internal registers available

9.1 Register summary

Table 5. Internal registers summary

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
General register set										
0x00	BRG0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x01	BRG1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x02	PortConf1	GPIO3.1	GPIO3.0	GPIO2.1	GPIO2.0	GPIO1.1	GPIO1.0	GPIO0.1	GPIO0.0	R/W
0x03	PortConf2	GPIO7.1	GPIO7.0	GPIO6.1	GPIO6.0	GPIO5.1	GPIO5.0	GPIO4.1	GPIO4.0	R/W
0x04	IOState	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	R/W
0x05	reserved	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	-
0x06	I2CAdr	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x07	I2CClkL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x08	I2CClkH	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x09	I2CTO	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TE	R/W
0x0A	I2CStat	1	1	1	1	I2CStat[3]	I2CStat[2]	I2CStat[1]	I2CStat[0]	R

[1] Since the GPIO pins are configured as inputs after reset, the default value of this register depends on the states of the GPIO

9.2 Register descriptions

9.2.1 Baud Rate Generator (BRG)

The baud rate generator is an 8-bit counter that generates the data rate for the transmitter and the receiver. The rate is programmed through the BRG register and the baud rate can be calculated as follows:

$$Baud\ rate = \frac{7.3728 \times 10^6}{16 + (BRG1,\ BRG0)} \qquad (1)$$

Remark: To calculate the baud rate the values in the BRG registers must first be converted from hex to decimal.

Remark: For the new baud rate to take effect, both BRG0 and BRG1 must be written in sequence (BRG0, BRG1) with new values. The new baud rate will be in effect once BRG1 is written.

9.2.2 Programmable port configuration (PortConf1 and PortConf2)

GPIO port 0 to port 7 may be configured by software to one of four types. These are: quasi-bidirectional, push-pull, open-drain, and input-only. Two bits are used to select the desired configuration for each port pin. PortConf1 is used to select the configuration for GPIO3 to GPIO0, and PortConf2 is used to select the configuration for GPIO7 to GPIO4. A port pin has Schmitt triggered input that also has a glitch suppression circuit.

Table 6. Port configurations

GPIOx.1	GPIOx.0	Port configuration
0	0	quasi-bidirectional output configuration
0	1	input-only configuration
1	0	push-pull output configuration
1	1	open-drain output configuration

9.2.2.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The SC18IM700 is a 3 V device, but the pins are 5 V tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

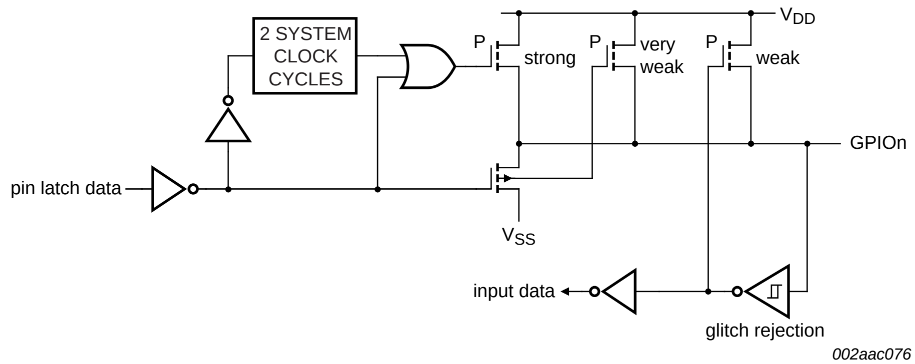


Fig 13. Quasi-bidirectional output configuration

9.2.2.2 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

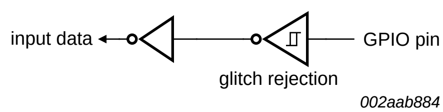


Fig 14. Input-only configuration

9.2.2.3 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

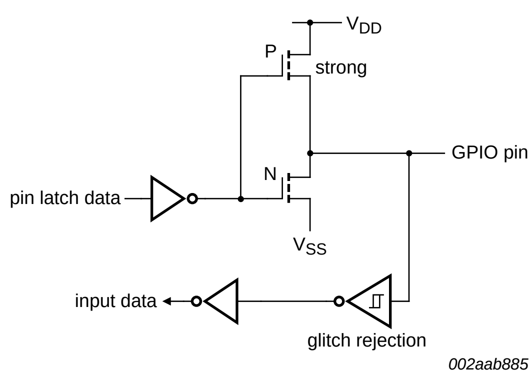


Fig 15. Push-pull output configuration

9.2.2.4 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

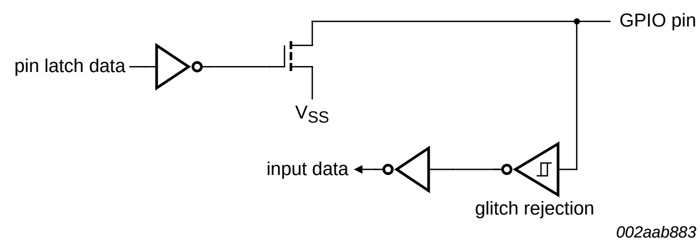


Fig 16. Open-drain output configuration

9.2.3 Programmable I/O pins state register (IOState)

When read, this register returns the actual state of all I/O pins. When written, each register bit will be transferred to the corresponding I/O pin programmed as output.

Table 7. IOState - Programmable I/O pins state register (address 0x04h) bit description

Bit	Symbol	Description
7:0	IOLevel	Set the logic level on the output pins. Write to this register: logic 0 = set output pin to zero logic 1 = set output pin to one Read this register returns states of all pins.

9.2.4 I²C-bus address register (I2CAdr)

The contents of the register represents the device's own I²C-bus address. The most significant bit corresponds to the first bit received from the I²C-bus after a START condition. A logic 1 in I2CAdr corresponds to a HIGH level on the I²C-bus, and a logic 0 corresponds to a LOW level on the I²C-bus. The least significant bit is not used, but should be programmed with a '0'.

I2CAdr is not needed for device operation, but should be configured so that its address does not conflict with an I²C-bus device address used by the bus master.

9.2.5 I²C-bus clock rates (I2CClk)

This register determines the serial clock frequency. The various serial rates are shown in Table 8. The frequency can be determined using the following formula:

$$bit\ frequency = \frac{7.3728 \times 10^6}{2 \times (I2CClkH + I2CClkL)} \quad (2)$$

I2CClkH determines the SCL HIGH period, and I2CClkL determines the SCL LOW period.

Table 8. I²C-bus clock frequency

I2CClk (I2CClkH + I2CClkL)	I²C-bus clock frequency
10 (minimum)	369 kHz
15	246 kHz
25	147 kHz
30	123 kHz
50	74 kHz
60	61 kHz
100	37 kHz

Remark: The numbers used in the formulas are in decimal, but the numbers to program I2CClkH and I2CClkL are in hex.

9.2.6 I²C-bus time-out (I2CTO)

The time-out register is used to determine the maximum time that SCL is allowed to be LOW before the I²C-bus state machine is reset.

When the I²C-bus interface is running, I2CTO is loaded after each I²C-bus state transition.

Table 9. I2CTO - I²C-bus time-out register (address 0x09h) bit description

Bit	Symbol	Description
7:1	TO[7:1]	time-out value
0	TE	enable/disable time-out function logic 0 = disable logic 1 = enable

The least significant bit of I2CTO (TE bit) is used as a time-out enable/disable. A logic 1 will enable the time-out function. The time-out period can be calculated as follows:

$$time\text{-}out\ period = \frac{I2CTO[7{:}1] \times 256}{57600}\ seconds \qquad (3)$$

The time-out value may vary, and it is an approximate value.

9.2.7 I²C-bus status register (I2CStat)

This register reports the I²C-bus transmit and receive frame status, whether the frame transmits correctly or not.

Table 10. I²C-bus status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I²C-bus status description
1	1	1	1	0	0	0	0	I2C_OK
1	1	1	1	0	0	0	1	I2C_NACK_ON_ADDRESS
1	1	1	1	0	0	1	0	I2C_NACK_ON_DATA
1	1	1	1	1	0	0	0	I2C_TIME_OUT

10. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1][2]

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature			–55	+125	°C
T_{stg}	storage temperature			–65	+150	°C
V_I	input voltage	referenced to V_{SS}		–0.5	+5.5	V
$I_{OH(I/O)}$	HIGH-level output current per input/output pin					
	GPIO3 to GPIO7			-	20	mA
	all other pins			-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin			-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current			-	120	mA
P_{tot}/pack	total power dissipation per package		[3]	-	1.5	W

[1] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[2] Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[3] Based on package heat transfer, not device power consumption.

11. Static characteristics

Table 12. Static characteristics

V_{DD} = 2.4 V to 3.6 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	V_{DD} = 3.6 V					
		Operating mode; f = 7.3728 MHz		-	9	15	mA
		Idle mode; f = 7.3728 MHz		-	3.25	5	mA
		Power-down mode (sleep); GPIO0 to GPIO7 as inputs; inputs at V_{DD}		-	50	70	µA
V_{POR}	power-on reset voltage			-	-	0.2	V
$V_{th(HL)}$	negative-going threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		–0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA	[2]	-	0.6	1.0	V
		I_{OL} = 3.2 mA	[2]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –20 mA; Push-pull mode; GPIO3 to GPIO7		$0.8V_{DD}$	-	-	V
		I_{OH} = –3.2 mA; Push-pull mode; GPIO0 to GPIO2		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = –20 mA; quasi-bidirectional mode; all GPIOs		V_{DD} – 0.3	V_{DD} – 0.2	-	V
C_{io}	input/output capacitance		[3]	-	-	15	pF
I_{IL}	LOW-level input current	logic 0; all ports; V_I = 0.4 V	[4]	-	-	–80	µA
I_{LI}	input leakage current	all ports; V_I = V_{IL} or V_{IH}	[5]	-	-	–10	µA
$I_{T(HL)}$	negative-going transition current	logic 1-to-0; all ports; V_I = 2.0 V at V_{DD} = 3.6 V	[6][7]	–30	-	–450	µA
$R_{RESET\_N(int)}$	internal pull-up resistance on pin $\overline{RESET}$			10	-	30	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] See Table 11 "Limiting values" for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[3] Pin capacitance is characterized but not tested.

[4] Measured with GPIO in quasi-bidirectional mode.

[5] Measured with GPIO in high-impedance mode.

[6] GPIO in quasi-bidirectional mode with weak pull-up (applies to all GPIO pins with pull-ups). Does not apply to open-drain pins.

[7] GPIO pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

12. Dynamic characteristics

Table 13. I²C-bus timing characteristics

All the timing limits are valid within the operating supply voltage and ambient temperature range; V_{DD} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions		Standard mode I²C-bus		Fast mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	μs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	μs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	μs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time			-	0.6	-	0.6	μs
$t_{VD;DAT}$	data valid time	LOW-level		-	0.6	-	0.6	μs
		HIGH-level		-	0.6	-	0.6	μs
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	μs
t_f	fall time of both SDA and SCL signals			-	0.3	-	0.3	μs
t_r	rise time of both SDA and SCL signals			-	1	-	0.3	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns

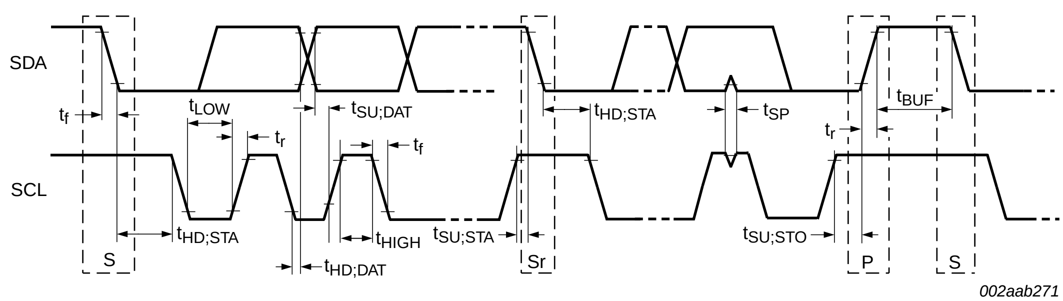
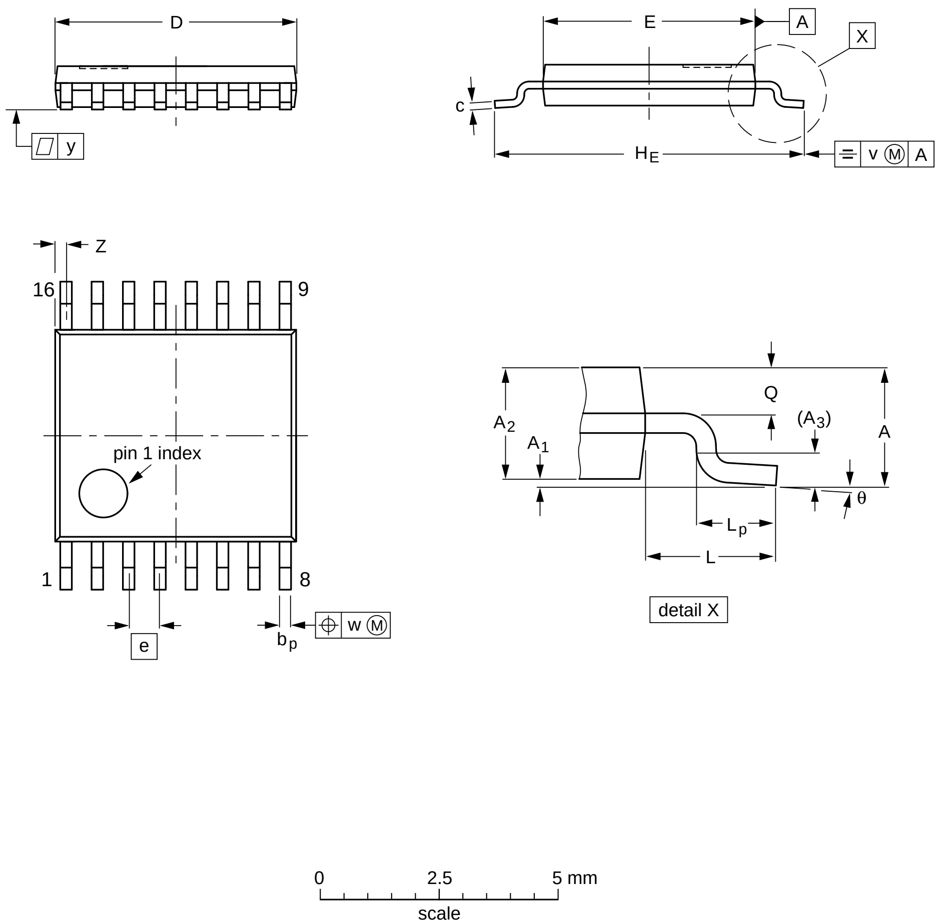


Fig 17. I²C-bus timing

13. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT403-1 (TSSOP16)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020C)

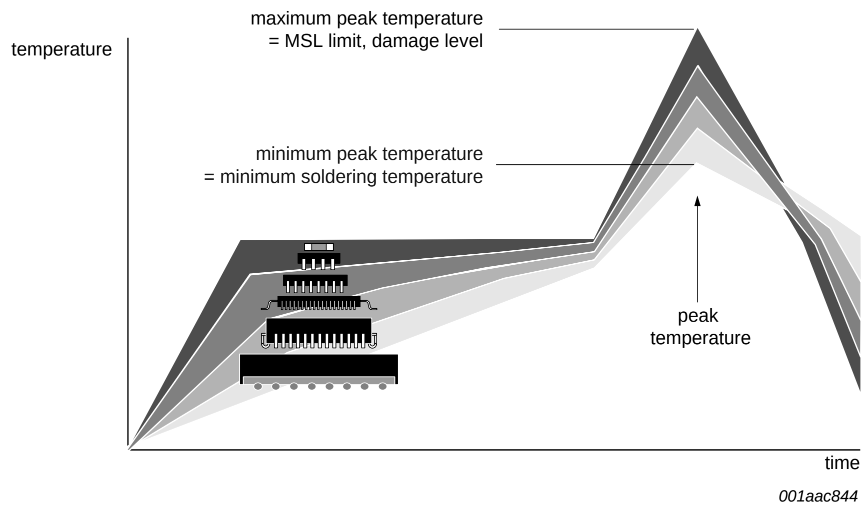
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Abbreviations

Table 16. Abbreviations

Acronym	Description
ASCII	American Standard Code for Information Interchange
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I^2C-bus	Inter Integrated Circuit bus
RX FIFO	Receive FIFO
TX FIFO	Transmit FIFO
UART	Universal Asynchronous Receiver/Transmitter

16. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC18IM700_4	20191009	Product data sheet	201910004I	SC18IM700_3
Modifications:	• Removed discontinued versions, and aligned pin 1 location in datasheet to ‘as-shipped’ configuration. Product and product orientation have not changed.			
SC18IM700_3	20171012	Product data sheet	201708035I	SC18IM700_2
Modifications:	• Added SC18IM700/S8 • Updated Section 4.1 “Ordering options” • Section 2 “Features and benefits”: 9th bullet item: changed from “2.3 V and 3.6 V operation” to “2.4 V and 3.6 V operation” • Table 5 “Internal registers summary”: – changed Default value for register IOState from “0x0F” to “-” – added Table note [1]			
SC18IM700_2	20070810	Product data sheet	-	SC18IM700_1
SC18IM700_1	20060228	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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