THE DATASHEET OF

A80601KESJSR-1

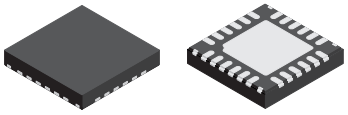
A80601 and A80601-1

High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Enhanced fault handling for ASIL B system compliance
- Wide input voltage range of 4.5 to 40 V for start/stop, cold crank, and load dump requirements
- Operate in Boost or SEPIC mode for flexible output
- Gate driver for external MOSFET to deliver higher output power
- Four integrated LED current sinks, up to 210 mA each
- Boost switching frequency synced externally or programmed from 260 kHz to 2.3 MHz
- Programmable boost frequency dithering to reduce EMI
- Advanced control allows minimum PWM on-time down to 0.3 µs, and avoids MLCC audible noises
- LED contrast ratio: 15,000:1 at 200 Hz using PWM dimming alone, 150,000:1 when combining PWM and analog dimming
- Excellent input voltage transient response even at lowest PWM duty cycle
- Gate driver for optional P-channel MOSFET input disconnect switch
- Extensive fault protection features

PACKAGE:



24-Pin 4 mm × 4 mm QFN with Wettable Flank

Not to scale

DESCRIPTION

The A80601 is a multi-output LED driver for automotive applications such as exterior lighting, heads-up display, and mid-size LCD backlighting. It implements a current-mode boost/SEPIC converter with gate driver for external N-channel MOSFET.

The A80601 provides four integrated current sinks driving up to 210 mA per string. Multiple sinks can be paralleled together to achieve higher LED currents up to 840 mA. The IC operates from single power supply from 4.5 to 40 V; once started, it can continue to operate down to 4 V. This allows it to withstand stop/start, cold crank, and load dump conditions encountered in automotive systems.

The A80601 can control LED brightness through an external PWM signal. By using the patented Pre-Emptive Boost control, an LED brightness contrast ratio of 15,000:1 can be achieved using PWM dimming at 200 Hz. A higher ratio of 150,000:1 is possible when using a combination of PWM and analog dimming.

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APPLICATIONS

- Automotive infotainment backlighting
- Automotive heads-up display
- Automotive interior and exterior lighting

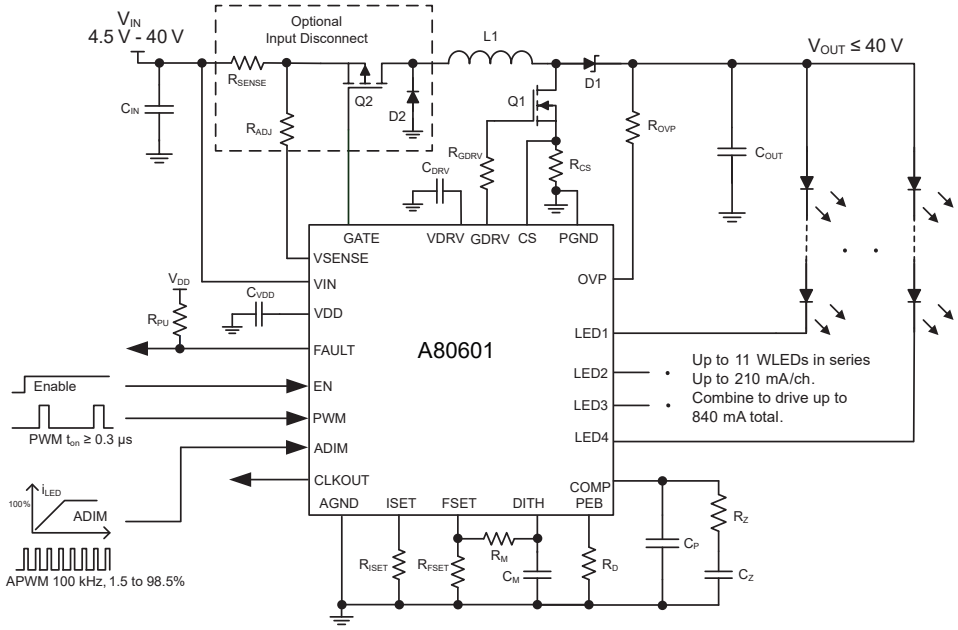

Figure 1: A80601 Simplified Circuit Configuration.
See Appendix A and B for detailed design examples.

DESCRIPTION (continued)

Switching frequency can be externally synchronized or programmed between 260 kHz and 2.3 MHz. This allows operation either above or below the AM band. A programmable dithering feature further reduces EMI. A Clock-Out is provided for other converters to sync to the A80601.

The A80601 provides protection against output short, overvoltage, open- or shorted-LED pin, and overtemperature. A cycle-by-cycle current limit protects the external boost switch against high current overloads. An external P-MOSFET can optionally be used to disconnect input supply in case of output to ground short fault. The A80601-1 is similar to A80601 except it adopts 'One-Out-All-Out' fault handling (See Fault Table section for details).

SELECTION GUIDE [1]

Part Number	Fault Handling	LED Driver	Package	Packing
A80601KESJSR	One-Out-Continue	4 × 210 mA	24-pin 4 × 4 mm wettable flank QFN with exposed thermal pad and sidewall plating	6000 pieces per reel
A80601KESJSR-1	One-Out-All-Out			

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pin	V_{LEDx}	x = 1..4	–0.3 to 40	V
OVP pin	V_{OVP}		–0.3 to 40	V
VIN	V_{IN}		–0.3 to 40	V
VSENSE, GATE	V_{SENSE}, V_{GATE}		Higher of –0.3 and (V_{IN} – 7.4) to V_{IN} +0.4	V
VDRV, GDRV	V_{DRV}, V_{GDRV}		–1.0 to 7.5	V
CS	V_{CS}		–0.3 to 7	V
EN, PWM, FAULT, ADIM, CLKOUT, COMP, DITH, PEB, FSET, ISET, VDD		External input signals must not be higher than V_{IN} + 0.4 V	–0.3 to 5.5	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	ES package measured on 4-layer PCB based on JEDEC standard	37	°C/W

[4] Additional thermal information available on the Allegro website.

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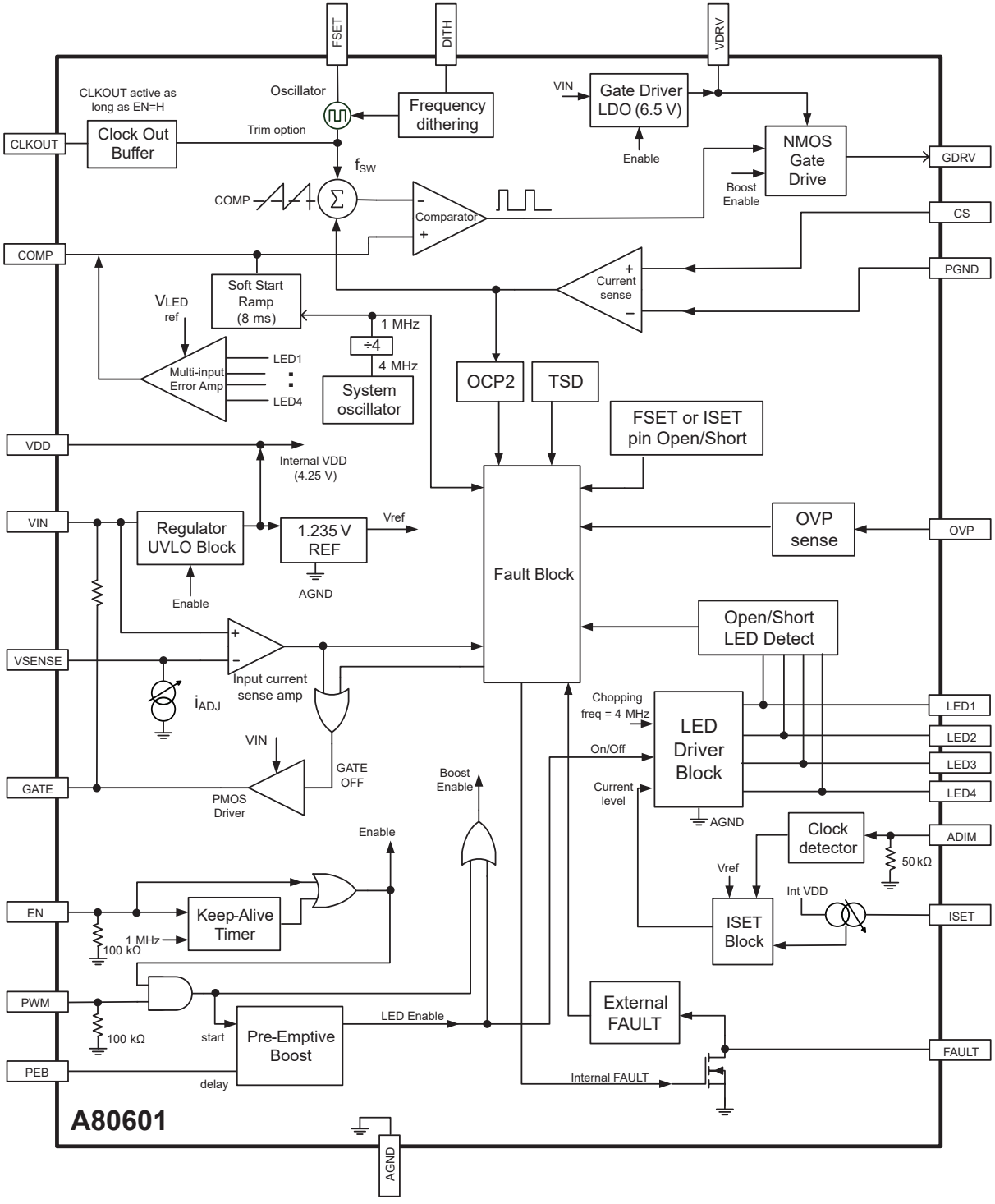

Figure 2: Functional Block Diagram

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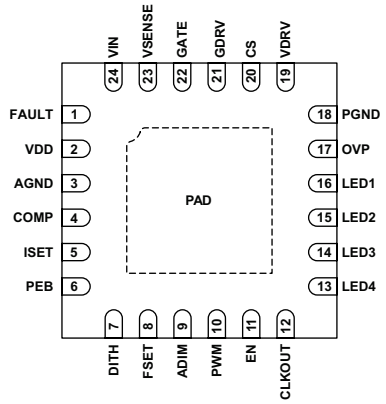
PINOUT DIAGRAM AND TERMINAL LIST



Package ES, 24-Pin QFN Pinouts

Terminal List Table

Number	Name	Function
1	FAULT	This pin is an open drain type configuration that will be pulled low when a fault occurs. Connect a pull-up resistor between this pin and desired logic level voltage.
2	VDD	Output of internal LDO (bias regulator). Connect a 1 µF decoupling capacitor between this pin and AGND. V_{DD} is regulated at ~4.25 V.
3	AGND	LED current Ground. Also serves as 'quiet' ground for analog signals.
4	COMP	Output of the error amplifier and compensation node. Connect a series RC network from this pin to AGND for control loop compensation.
5	ISET	Connect R_{ISET} resistor between this pin and AGND to set the 100% LED current.
6	PEB	Pre-Emptive Boost control: Connect resistor from PEB pin to AGND to fine-tune the delay between boost switch and LED current sinks. Leave pin open for minimum PEB delay of 1 µs.
7	DITH	Dithering control: connect a capacitor to AGND to set the dithering modulation frequency (1 to 22 kHz). Connect a resistor between DITH and FSET pins to set the dithering range (such as ±5% of f_{SW}).
8	FSET	Frequency/Synchronization pin. A resistor R_{FSET} from this pin to AGND sets the switching frequency f_{SW} (with dithering superimposed) between 200 kHz and 2.3 MHz. It can also be used to synchronize f_{SW} to an external frequency between 260 kHz and 2.3 MHz (frequency dithering is disabled in this case).
9	ADIM	Analog dimming. Apply a PWM clock (40 to 1000 kHz) to pin and the duty cycle of this clock determines the LED current. Alternatively, apply DC level between 0.2 and 2 V to vary LED current between 10% and 100%. If unused, pull pin above 2 V for 100%.
10	PWM	Controls the on/off state of LED current sinks to reduce the light intensity by using pulse-width modulation. Typical PWM dimming frequency is in the range of 200 Hz to 2 kHz. EN and PWM pins may be tied together to allow single-wire dimming control.
11	EN	Enables the IC when this pin is pulled high. If EN goes low, the IC remains in standby mode for up to 16 ms, then shuts down completely.
12	CLKOUT	Logic output representing the switching frequency of internal boost oscillator. This allows other converters to be synchronized to the same f_{SW} with the same dithering modulation, if applicable. Output is active as long as IC is enabled.
13-16	LED4..LED1	LED current sinks #4 to #1. Connect the cathode of each LED string to pin. Unused LED pin must be terminated to AGND through a 2.37 kΩ resistor.
17	OVP	Overvoltage Protection. Connect external resistor from VOUT to this pin to adjust the overvoltage protection threshold.
18	PGND	Power Ground for internal Gate Driver. Connect pin to external power GND with shortest path.
19	VDRV	Gate driver supply voltage (~6.5 V). Connect a 2.2 µF MLCC to PGND for buffer.
20	CS	Current Sense for peak current control of power switch. Connect to sense resistor at the Source terminal of external power MOSFET.
21	GDRV	Gate driver for power switch. Connect to Gate of external power MOSFET. (External FET must be fully enhanced at V_{GS} = 5 V).
22	GATE	Output gate driver pin for external P-channel MOSFET (input disconnect switch).
23	VSENSE	Connect this pin to the negative sense side of the input current sense resistor R_{SC}. The threshold voltage is measured as $V_{IN} - V_{SENSE}$. There is also fixed i_{ADJ} current sink to allow for trip threshold adjustment.
24	VIN	Input power to the IC as well as the positive side of input current sense resistor.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. Must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad.

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ELECTRICAL CHARACTERISTICS [1]: Unless otherwise noted, specifications are valid at V_{IN} = 12 V, T_J = 25°C, • indicates specifications guaranteed over the full operating temperature range with T_J = –40°C to 125°C, typical specifications are at T_J = 25°C

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage Range [3]	V_{IN}		•	4.5	–	40	V
VIN UVLO Start Threshold	$V_{UVLO(rise)}$	V_{IN} rising	•	–	–	4.45	V
VIN UVLO Stop Threshold	$V_{UVLO(fall)}$	V_{IN} falling	•	–	–	4.05	V
UVLO Hysteresis [2]	V_{UVLO_HYS}			300	400	500	mV
INPUT CURRENTS							
VIN Pin Operating Current	I_{OP}	EN and PWM = H, C_{GATE} = 1 nF from GDRV to PGND, f_{SW} = 2 MHz	•	–	22	32	mA
VIN Pin Quiescent Current	I_Q	EN = H and PWM = L, f_{CLKOUT} = 2 MHz	•	–	4	6	mA
VIN Pin Sleep Current	I_{SLEEP}	V_{IN} = 16 V, V_{EN} / V_{PWM} = V_{SYNC} = 0 V	•	–	1	5	µA
INPUT LOGIC LEVELS (EN/PWM, ADIM)							
Input Logic Level-Low	V_{IL}		•	–	–	0.4	V
Input Logic Level-High	V_{IH}		•	1.5	–	–	V
Input Pull-Down Resistor	R_{EN}, R_{PWM}	Input = 5 V		60	100	140	kΩ
	R_{ADIM}	Input = 5 V		30	50	70	kΩ
OUTPUT LOGIC LEVELS (CLKOUT)							
Output Logic Level-Low	V_{OL}	5 V < V_{IN} < 40 V, i_{LOAD} = 1 mA	•	–	–	0.3	V
Output Logic Level-High	V_{OH}	5 V < V_{IN} < 40 V, i_{LOAD} = 1 mA	•	1.8	–	–	V
CLKOUT Duty Cycle	D_{CLKOUT}	f_{SW} = 2 MHz, no external sync	•	33	50	67	%
CLKOUT Negative Pulse Width	t_{CLKNPW}	External sync = 260 kHz to 2.3 MHz		–	200	–	ns
ANALOG DIMMING (ADIM)							
Analog Dimming Current Level (shown as % of full-scale current)	i_{ADIM50}	DC 1.0 V applied to ADIM pin		–	50	–	%
	i_{ADIM25}	DC 0.5 V applied to ADIM pin		23	25	27	%
APWM Frequency Range [2]	f_{APWM}	Clock signal applied to ADIM pin	•	40	–	1000	kHz
APWM Duty Cycle Range [2]	D_{APWM}	f_{APWM} = 100 kHz	•	1.5	–	98.5	%
VDD REGULATOR							
Regulator Output Voltage	V_{DD}	V_{IN} > 6 V, i_{LOAD} < 1 mA		4.05	4.25	4.45	V
VDD UVLO Start Threshold	$V_{DDUVLOrise}$	V_{DD} rising, no external load		–	3.2	–	V
VDD UVLO Stop Threshold	$V_{DDUVLOfall}$	V_{DD} falling, no external load		–	2.65	–	V
ERROR AMPLIFIER							
Amplifier Gain [2]	gm	V_{COMP} = 1.5 V		–	900	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V, A80601 (symm COMP)		–	–500	–	µA
		V_{COMP} = 1.5 V, A80601-1 (asymm COMP)		–	–700	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 1.5 V		–	+500	–	µA
COMP Pin Pull Down Resistance	R_{COMP}	FAULT = 0, V_{COMP} = 1.5 V		–	1.4	–	kΩ

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
OVERVOLTAGE PROTECTION							
OVP Pin Voltage Threshold	$V_{OVP(th)}$	OVP pin connected to V_{OUT}	•	2.2	2.5	2.8	V
OVP Pin Sense Current Threshold	$i_{OVP(th)}$	Current into OVP pin at 125ºC		140	146.5	153	µA
		Measured over temperature	•	140	150	160	µA
OVP Sense Current Temperature Coefficient [2]	Δi_{OVP}	Current into OVP pin		–	–36	–	nA/ºC
OVP Pin Leakage Current	I_{OVPLKG}	V_{OUT} = 16 V, EN = L	•	–	0.1	1	µA
OVP Variation at Output	Δ_{OVP}	Measured at V_{OUT} when R_{OVP} = 188 kΩ		–	–	4	%
			•	–	–	7	%
Undervoltage Detection Threshold	$V_{UVP(th)}$	Measured at V_{OUT} when R_{OVP} = 188 kΩ [2]		2.4	2.55	2.7	V
		Measured at V_{OUT} when R_{OVP} = 0 Ω		0.13	0.20	0.25	V
BOOST SWITCH GATE DRIVER							
Gate Driver Supply Voltage	V_{DRV}	Measured at V_{IN} > 7.5 V		–	6.5	–	V
Gate Driver Pull-Up and Pull-Down	R_{GDRV}	Measured at i_{GDRV} = 100 mA		–	2.5	–	Ω
Gate Pull-Down When Disabled	R_{GDRV_OFF}	EN = L, V_{IN} = 0 V		–	100	–	kΩ
Peak Sink Current [2]	i_{SINK}	Measured at V_{GDRV} = V_{DRV}		–	2	–	A
Peak Source Current [2]	i_{SOURCE}	Measured at V_{GDRV} = 0 V		–	2	–	A
Gate Rise / Fall Time [2]	t_{RISE}, t_{FALL}	Measured with C_{LOAD} = 1.5 nF; V_{GDRV} between 10% and 90% of V_{DRV}		–	7	–	ns
Minimum Gate Driver On-Time	$t_{SW(ON)}$		•	–	–	100	ns
Minimum Gate Driver Off-Time	$t_{SW(OFF)}$		•	–	–	100	ns
BOOST SWITCH CURRENT SENSE							
Primary Current Sense Limit	$i_{CS(LIM1)}$	Exceeding $i_{CS(LIM1)}$ causes gate driver to truncate existing cycle, but does not shut down	•	175	210	245	mV
Secondary Current Sense Limit	$i_{CS(LIM2)}$	Exceeding $i_{CS(LIM2)}$ causes gate driver to shut down and latch off		–	300	–	mV
Secondary Current Sense Limit Propagation delay [2]	$t_{CSDELAY}$	Overdrive CS threshold by 10%, excluding leading edge blanking		–	32	–	ns
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	R_{FSET} = 10 kΩ	•	1.95	2.15	2.35	MHz
		R_{FSET} = 110 kΩ		–	200	–	kHz
FSET Pin Voltage	V_{FSET}	R_{FSET} = 10 kΩ		–	1.00	–	V
SYNCHRONIZATION							
Sync Input Logic Level	V_{SYNCL}	FSET/SYNC pin logic Low	•	–	–	0.4	V
	V_{SYNCH}	FSET/SYNC pin logic High	•	1.5	–	–	V
Synchronized PWM Frequency	f_{SWSYNC}		•	260	–	2300	kHz
Synchronization Input Min Off-Time	$t_{PWSYNCOFF}$		•	150	–	–	ns
Synchronization Input Min On-Time	$t_{PWSYNCON}$		•	150	–	–	ns

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Characteristics	Symbol	Test Conditions			Min.	Typ.	Max.	Unit
LED CURRENT SINKS								
LEDx Accuracy [4]	Err_{LED}	i_{ISET} = 120 µA (R_{ISET} = 8.33 kΩ)		•	–	0.7	3	%
LEDx Matching	Δ_{LEDx}	i_{ISET} = 120 µA		•	–	0.8	2	%
LEDx Regulation Voltage	V_{LED}	Measured individually with all other LED pins tied to ≥1 V, i_{ISET} = 120 µA, V_{ADIM} > 2.1 V	A80601	•	650	750	850	mV
			A80601-1	•	760	860	960	mV
I_{ISET} to I_{LEDx} Current Gain	A_{ISET}	i_{ISET} = 120 µA		•	1432	1466	1500	A/A
ISET Pin Voltage	V_{ISET}	V_{ADIM} > 2.1 V			0.955	0.985	1.015	V
Allowable ISET Current	i_{ISET}	V_{ADIM} > 2.1 V		•	20	–	144	µA
LED String Partial-Short Detect	V_{LEDSD}	Sensed from each LED pin to GND while its current sink is in regulation; all other LED pins tied to 1 V		•	4.9	5.5	6.1	V
LED Pin Shorted-to-GND Test Duration [2]	t_{LEDSTG}	Wait time before proceeding with Soft-Start (if no LED pin is shorted to GND)			–	1.5	–	ms
Soft-Start Ramp-Up Time [2]	t_{SSRU}	Maximum time duration before all LED channels come into regulation, or OVP is tripped, whichever comes first			6.6	8.2	9.8	ms
Enable Pin Shut Down Delay	$t_{EN(OFF)}$	EN goes from High to Low; exceeding $t_{EN(OFF)}$ results in IC shutdown		•	10	16	22	ms
Minimum PWM On-Time	t_{PWMH}	First and subsequent PWM pulses		•	–	0.3	0.4	µs
Minimum PWM Off-Time (for PWM ≠ 100%) [2]	t_{PWMLOW}	Externally pulsing PWM pin		•	–	–	1	µs
INPUT DISCONNECT GATE PIN								
Gate Pin Sink Current	I_{GSINK}	V_{GS} = V_{IN}, no input OCP fault			–	–113	–	µA
Gate Pin Source Current	$I_{GSOURCE}$	V_{GS} = V_{IN} – 6 V, input OCP fault tripped			–	6	–	mA
Gate Shutdown Delay When Over-Current Fault Is Tripped [2]	$t_{GATEFAULT}$	V_{IN} – V_{SENSE} = 200 mV; monitored at FAULT pin			–	–	3	µs
Gate Voltage	V_{GS}	PMOS Gate to source voltage measured when gate is on			–	–6.7	–	V
VSENSE PIN								
VSENSE Pin Sink Current	i_{ADJ}			•	16	20	24	µA
VSENSE Trip Point	$V_{SENSETRIP}$	Measured between V_{IN} and V_{SENSE}, R_{ADJ} = 0 Ω		•	88	98	108	mV
FAULT PIN								
FAULT Output Pull-Down Voltage	V_{FAULT}	i_{FAULT} = 1 mA			–	–	0.5	V
FAULT Pin Leakage Current	$I_{FAULT-LKG}$	V_{FAULT} = 5 V			–	–	1	µA
External FAULT Input Low	V_{FIL}	No internal faults; FAULT pin externally pulled down		•	–	–	0.8	V
External FAULT Input High	V_{FIH}	No internal faults		•	1.5	–	–	V
External FAULT Deglitch Timer	t_{FIL}	No internal faults; delay (in f_{SW} cycles) from FAULT pin externally pulled L to LED off; ignored if FAULT returns to H before that			–	8	–	cycles
THERMAL PROTECTION (TSD)								
Thermal Shutdown Threshold [2]	T_{SD}	Temperature rising			155	170	–	°C
Thermal Shutdown Hysteresis [2]	T_{SDHYS}				–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.
[3] Minimum V_{IN} = 4.5 V is only required at startup. After startup is completed, IC can continue to operate down to V_{IN} = 4 V.
[4] LED current is trimmed to cancel variations in both Gain and ISET voltage.

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FUNCTIONAL DESCRIPTION

The A80601 is a multi-string LED regulator with four precision current sinks and a gate driver for external boost MOSFET switch. It incorporates a patented Pre-Emptive Boost (PEB) control algorithm to achieve PWM dimming ratio over 15,000:1 at 200 Hz under nominal application conditions. PEB control also minimizes output ripple to avoid audible noise from output ceramic capacitors.

The switching frequency can be either synchronized to an external clock or generated internally. Spread-spectrum technique (with user-programmable dithering range and modulation frequency) is provided to reduce EMI. A clock-out signal (CLKOUT) allows other converters to be synchronized to the switching frequency of A80601.

Enabling the IC

The A80601 wakes up when EN pin is pulled above logic high level, provided that VIN pin voltage is over the VIN_UVLO threshold. The boost stage and LED channels are enabled separately by PWM = H signal after the IC powers up.

The IC performs a series of safety checks at power up, to determine if there are possible fault conditions that might prevent the system from functioning correctly. Power-up checks include:

- VOUT shorted to GND
- LED pin shorted to GND
- FSET pin open/shorted
- ISET pin open/shorted to GND, etc.

Only if no faults were detected, then the IC can proceed to start switching.

As long as EN = H, the PWM pin can be toggled to control the brightness of LED channels by using PWM dimming. Alternatively, EN and PWM can be tied together to allow single-wire control for both power on/off and PWM dimming. If EN is pulled low for longer than 16 ms, the IC shuts off.

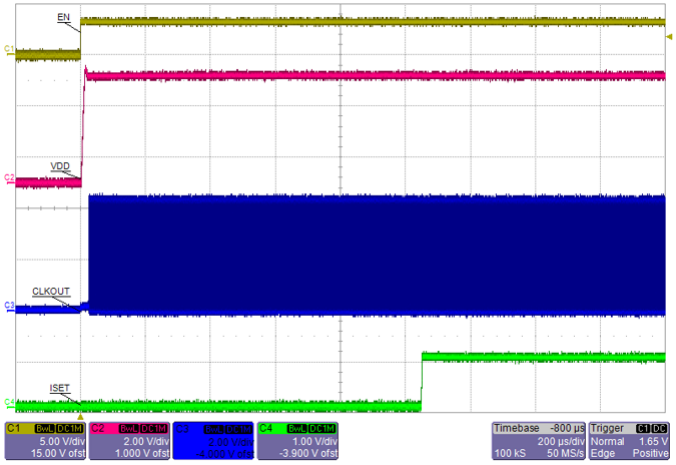

Figure 3: Startup showing EN, VDD, CLKOUT, and ISET (PWM = L). Note that CLKOUT is available as soon as V_{DD} ramps up, even though Boost stage and LED drivers are not yet enabled.

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Powering Up: LED Detection Phase

The VIN pin has an undervoltage lockout (UVLO) function that prevents the A80601 from powering up until the UVLO threshold is reached. Once the VIN pin goes above UVLO and a high signal is present on the EN pin, the IC proceeds to power up. At this point, the A80601 is going to enable the disconnect switch and will try to check if any LED pins are shorted to GND and/or are not used. The LED detection phase starts when PWM = H and the GATE voltage of the input disconnect PMOS switch is pulled down to 3.3 V below V_{IN}.

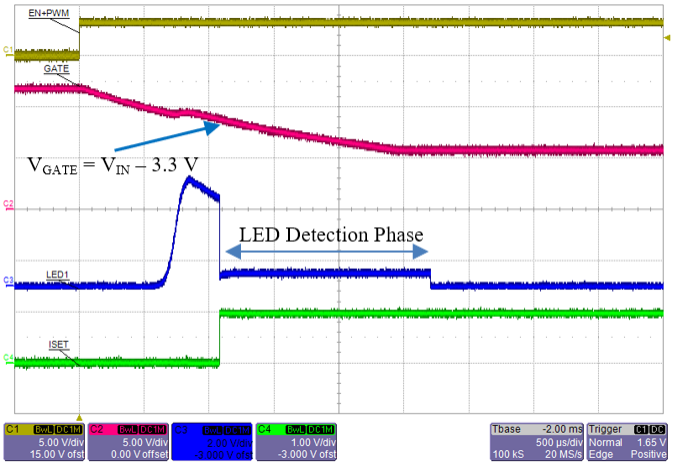

Figure 4: Startup showing EN+PWM, GATE, LED1, and ISET. Note that LED Detection Phase starts as soon as GATE pin is pulled down to 3.3 V below V_{IN} (provided that PWM = H).

Once the voltage threshold on VLED pins exceeds ~120 mV, a delay of approximately 1.5 ms is used to determine the status of the pins.

Unused LED pin should be terminated with a 2.37 kΩ resistor to GND. At the end of LED detection phase, any channel with pull down resistor is then disabled and will not contribute to the boost regulation loop.

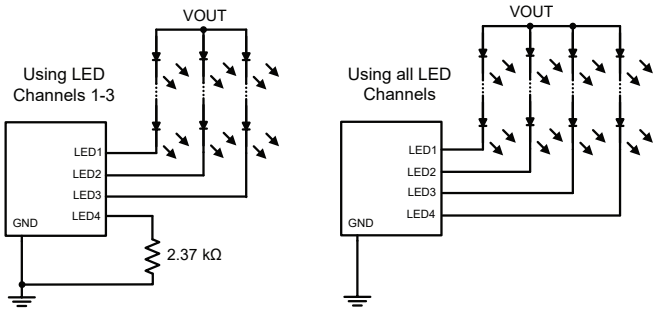

Figure 5: How to signal an unused LED channel during startup LED detection phase

Table 1: LED Detection phase voltage threshold levels

LED Pin Voltage Measured	Interpretation	Outcome
< 120 mV	LED pin shorted to GND fault	Cannot proceed with soft-start unless fault is removed
~ 230 mV	LED channel not in use	LED channel is removed from operation
> 340 mV	LED channel in use	Proceed with soft-start

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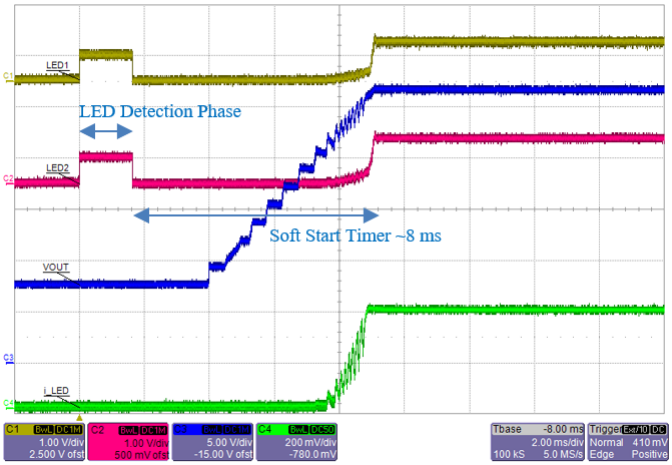

Figure 6: Normal startup showing all channels passed LED Detection phase (only LED1 and LED2 pin voltages are shown). Total LED current = 100 mA × 4.

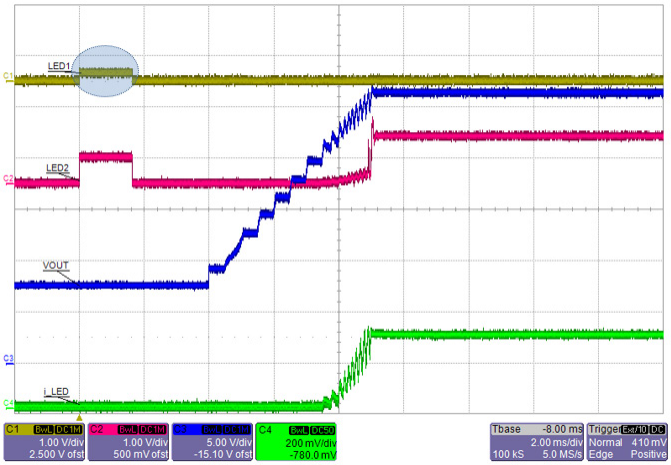

Figure 7: Normal startup showing LED1 channel is disabled with a 2.37 kΩ resistor to GND. Total LED current = 100 mA × 3.

If an LED pin is shorted to ground, the A80601 will not proceed with soft start until the short is removed from the LED pin. This prevents the A80601 from ramping up the output voltage and putting an uncontrolled amount of current through the LEDs.

The FAULT pin is pulled low in case of LED pin shorted-to-GND fault, but the IC continues to retry. Once the fault is removed, the soft-start process will continue. The same applies in case of FSET or ISET pin is shorted to GND.

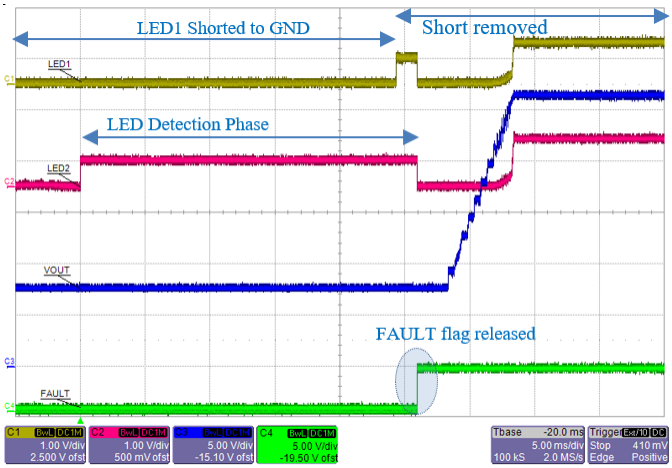

Figure 8: LED1 is shorted-to-GND initially, then released. After the fault is removed, the IC auto-recovers and proceeds with soft-start.

FAULT is released at the end of LED detection phase.

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Power Up: Boost Output Undervoltage

During startup, after the input disconnect switch has been enabled, the output voltage is checked through the OVP (over-voltage protection) pin. If the sensed voltage does not rise above $V_{UVP(th)}$, the output is assumed to be at fault and the IC will not proceed with soft start. Output UVP level is linked to the OVP level programmed according to the equation:

$$V_{UVP} = V_{OVP} / 12$$

Undervoltage protection may be caused by one of the following faults:

- Output capacitor shorted to GND
- Boost inductor or diode open
- OVP sense resistor open

After an UVP (undervoltage protection) fault, the A80601 is immediately shutdown and latched off. To enable the IC again, the latched fault must be cleared. This can be achieved by powering-cycling the IC, which means either:

- V_{IN} falls below falling UVLO threshold, or
- EN = L for >16 ms.

Alternatively, latched fault can be cleared by keeping EN = H but pulling PWM = L for >16 ms. This method has the advantage that it does not interrupt the CLKOUT signal.

Soft Start Function

During startup, the A80601 ramps up its boost output voltage following a fixed slope, as determined by OVP set point and Soft-Start Timer. This technique limits the input inrush current and ensures consistent startup time regardless of the PWM dimming duty cycle.

The soft-start process is completed when any one of the following conditions is met:

- All enabled LED channels have reached their regulation current,
- Output voltage has reached 93% of its OVP threshold, or
- Soft-start ramp time (t_{SS}) has expired.

To summarize, the complete startup process of A80601 consists of:

- Power-up error checking
- Enabling input disconnect switch
- LED pin open/short detection
- Soft-start ramp

This is illustrated by the following startup timing diagram (not to scale):

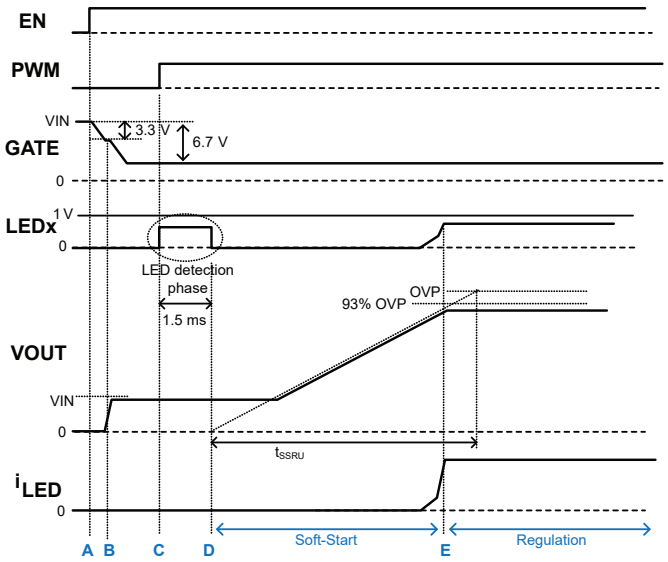

Figure 9: Complete startup process of A80601

Explanation of Events:

A: EN = H wakes up the IC. V_{DD} ramps up and CLKOUT becomes available. IC starts to pull down GATE slowly.

B: When GATE is pulled down to 3.3 V below V_{IN}, I_{SET} becomes enabled. IC is now waiting for PWM = H to startup.

C: Once PWM = H, the IC checks each LEDx pins to determine if it is in use, disabled, or shorted to GND.

D: Soft-Start begins at the completion of LED pin short-detect phase of ~1.5 ms. V_{OUT} ramps up following a fixed slope set by OVP and soft-start timer of ~8 ms.

E: Soft-start terminates when all LED currents reached regulation, V_{OUT} reached 93% OVP, or soft-start timer expired.

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Frequency Selection

The switching frequency of the boost regulator is programmed by a resistor connected to FSET pin. The switching frequency can be selected anywhere from 260 kHz to 2.3 MHz. The chart below shows the typical switching frequency verses FSET resistor value.

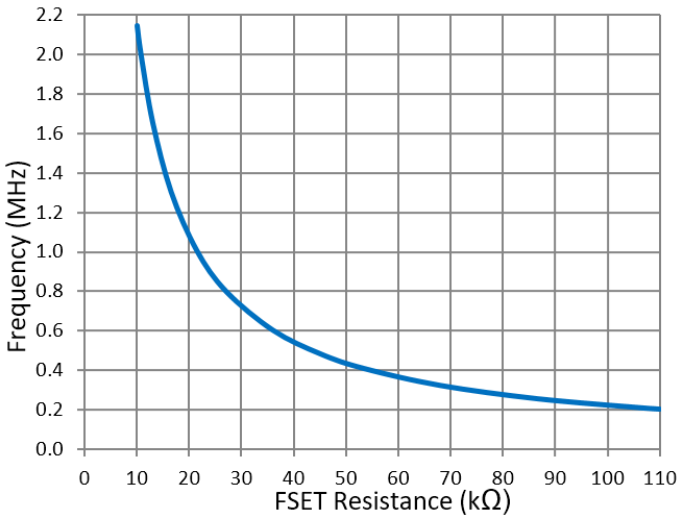

Figure 10: Switching Frequency as a function of FSET Resistance

Alternatively, the following empirical formula can be used:

Equation 1: $R_{FSET} = (21.5 / f_{SW}) - 0.2$

where f_{SW} is in MHz and R_{FSET} is in kΩ.

If a fault occurs during operation that will increase the switching frequency, the internal oscillator frequency is clamped to a maximum of 3.5 MHz. If the FSET pin is shorted to GND, the part will shut down. For more details, refer to the Fault Mode Table section.

Synchronization

The A80601 can also be synchronized using an external clock from 260 kHz to 2.3 MHz. At power up, if the FSET pin is held low, the IC will not start. Only when the FSET pin is tristated to allow for the pin to rise to about 1 V, or when a sync clock is detected, the A80601 will then try to power up.

The basic requirement of the external sync signal is 150 ns minimum on-time and 150 ns minimum off time. The diagram below shows the timing restrictions for a synchronization clock at 2.2 MHz.

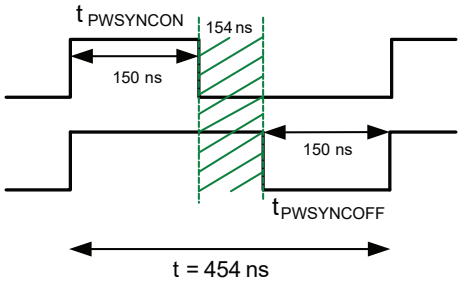

Figure 11: Pulse width requirements for an External Sync clock at 2.2 MHz

Based on the above, any clock with a duty cycle between 33% and 66% at 2.2 MHz can be used. The table below summarizes the allowable duty cycle range at various synchronization frequencies.

Table 2: Acceptable Duty Cycle range for External Sync clock at various frequencies

Sync. Pulse Frequency	Duty Cycle Range
2.2 MHz	33% to 66%
2 MHz	30% to 70%
1 MHz	15% to 85%
600 kHz	9% to 91%
300 kHz	4.5% to 95.5%

If it is necessary to switch over between internal oscillator and external sync during operation, ensure the transition takes place at least 500 ns after the previous PWM = H rising edge. Alternatively, execute the switchover during PWM = L only. This restriction does not apply if PWM dimming is not being used.

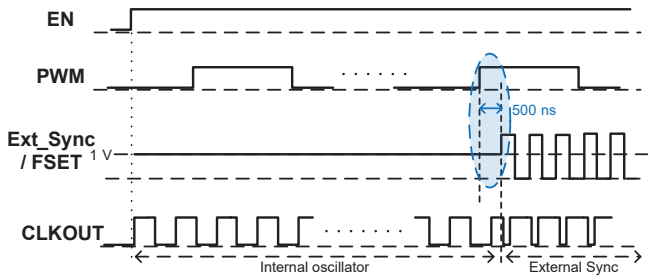

Figure 12: Avoid switching over between Internal Oscillator and External Sync in highlighted region

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Loss of External Sync Signal

Suppose the A80601 started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation. In that case, one of the following happens:

- If the external SYNC signal is high impedance (open), the IC continues normal operation after approximately 5 µs, at the switching frequency set by R_{FSET}. No FAULT flag is generated.
- If the external SYNC signal is stuck low (shorted to ground), the IC will detect an FSET-shorted-to-GND fault. FAULT pin is pulled low after approximately 10 µs, and switching is disabled. Once the FSET pin is released or SYNC signal is detected again, the IC will proceed to soft-start.

To prevent generating a fault when the external SYNC signal is stuck at low, the circuit shown below can be used. When the external SYNC signal goes low, the IC will continue to operate normally at the switching frequency set by the R_{FSET}. No FAULT flag is generated.

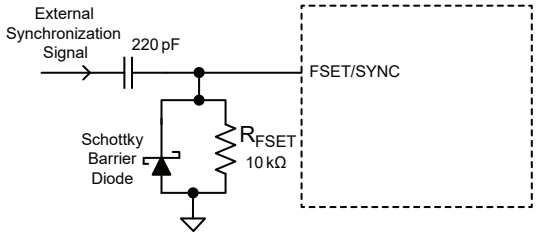

Figure 13: Countermeasure for External Sync Stuck-at-Low Fault

It is important to use a small capacitance for the AC-coupling capacitor (220 pF in the above example). If the capacitance is too large, the IC may incorrectly declare a FSET-shorted-to-GND fault and restart.

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Switching Frequency Dithering

To minimize the peak EMI spikes at switching frequency harmonics, the A80601 offers the option of frequency dithering, or spread-spectrum clocking. This feature simplifies the input filters needed to meet the automotive CISPR 25 conducted and radiated emission limits.

For maximum flexibility, the A80601 allows both dithering range and modulation frequency to be independently programmable using two external components.

The Dithering Modulation Frequency capacitor value is determined by using the approximate equation:

Equation 2: $C_{DITH}\,(nF) = 25 / f_{DM}\,(kHz)$

where C_{DITH} is the value of capacitor connected from DITH pin to GND.

The resistor that sets the dithering range is calculated using the approximate equation:

Equation 3: $R_{DITH} = (20 \times R_{FSET}) / Range\,(\pm\%)$

where R_{FSET} is the resistor from FSET pin to GND, R_{DITH} is the resistor between DITH and FSET pins.

As an example, by using R_{FSET} = 10 kΩ, R_{DITH} = 40.2 kΩ, and C_{DITH} = 22 nF, the resulted switching frequency is f_{SW} = 2.15 MHz ±5% modulated at 1.1 kHz. This is illustrated by the following diagram.

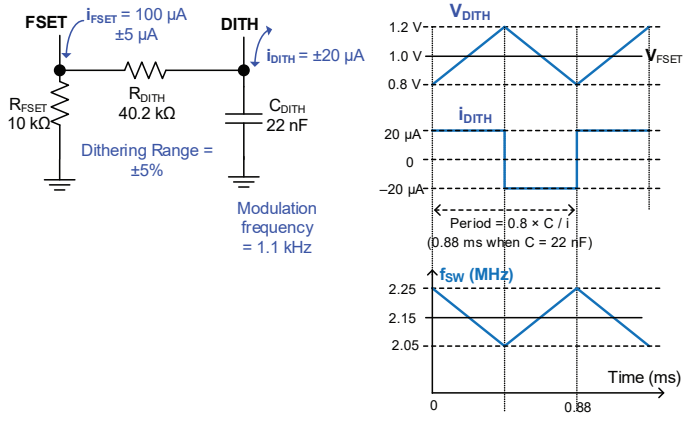

Figure 14: How to Program Switching Frequency Dithering Range and Modulation Frequency

There are no hard limits on dithering range and modulation frequency. As a general guideline, pick a dithering range between ±5% and 10%, with the modulation frequency between 1 kHz and 3 kHz. In practice, using a larger dithering range and/or higher modulation frequency do not generate any noticeable benefits.

If dithering function is not desired, it can be disabled by disconnecting the R_{DITH} between DITH and FSET pins. Connect DITH pin to VDD if C_{DITH} is not populated. Dithering is always disabled when f_{SW} is controlled by external sync. R_{DITH} and C_{DITH} have no effects in this case even if they were populated.

Clock Out Function

The A80601 allows other ICs to be synchronized to its internal switching frequency through the CLKOUT pin.

The CLKOUT signal is available as soon as the IC is enabled (EN = H), even when the boost stage is not active (PWM = L). Its frequency is the same as that of the internal oscillator. Its duty cycle, however, depends on how the switching frequency is generated:

- If f_{SW} is programmed by FSET resistor, the CLKOUT duty cycles is approximately 50%.
- If f_{SW} is controlled by external sync, the output signal has a fixed 200 ns negative pulse width (CLKOUT = L), regardless of the external sync frequency.

This is illustrated by the following waveforms:

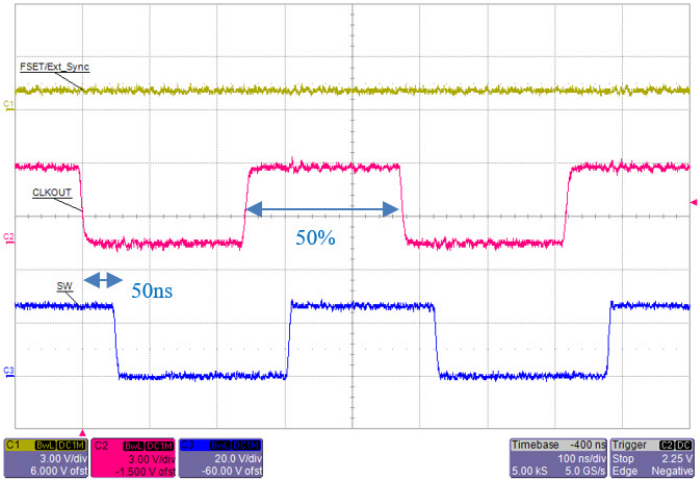

Figure 15: Without external sync, the CLKOUT signal has a fixed duty cycle of 50%. Delay from CLKOUT falling edge to SW falling edge is approximately 50 ns.

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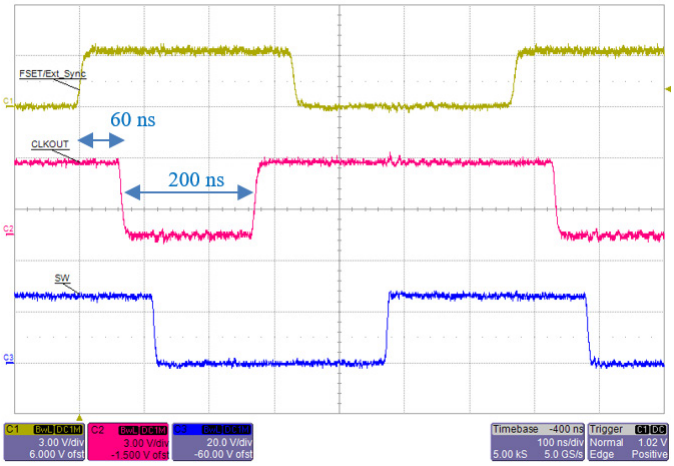

Figure 16: With external sync, the CLKOUT signal has a fixed negative pulse width of 200 ns. Delay from SYNC rising edge to CLKOUT falling edge is approximately 60 ns.

LED Current Setting

The maximum LED current can be up to 210 mA per channel and is set through the ISET pin. Connect a resistor R_{ISET} between this pin and GND. The relation between I_{LED} and R_{ISET} is given below:

Equation 4:

$$I_{LED} = I_{SET} \times A_{ISET}$$

$$I_{SET} = V_{ISET} / R_{ISET}$$

$$Therefore\ R_{ISET} = (V_{ISET} \times A_{ISET}) / I_{LED}$$

$$= 1444 / I_{LED}$$

where I_{LED} current is in mA and R_{ISET} is in kΩ.

This sets the maximum current through the LEDs, referred to as the '100% current'. The average LED current can be reduced from the 100% current level by using either PWM dimming or analog dimming.

Table 3: ISET resistor values vs. LED current. Resistances are rounded to the nearest E-96 (1%) resistor value.

Standard Closest RISET Resistor Value	LED current per channel
7.15 kΩ	200 mA
9.53 kΩ	150 mA
14.3 kΩ	100 mA
19.1 kΩ	75 mA
28.7 kΩ	50 mA

PWM Dimming

When both EN and PWM pins are pulled high, the A80601 turns on all enabled LED current sinks. When either EN or PWM is pulled low, all LED current sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active.

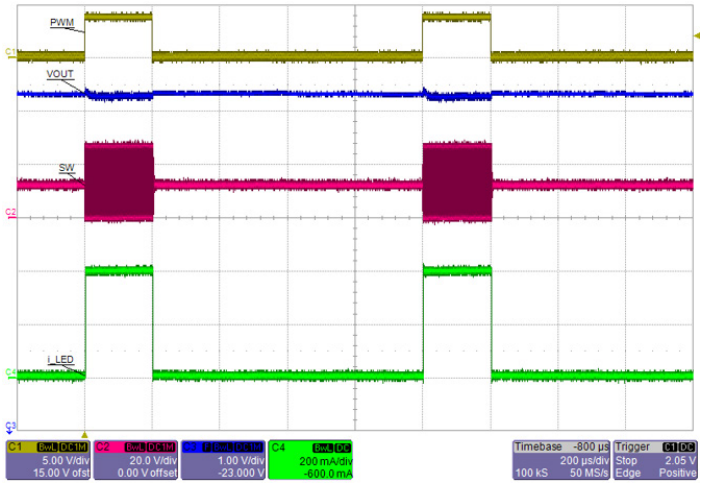

Figure 17: PWM dimming operation at 20% 1 kHz. CH1 = PWM (5 V/div), CH2 = SW (20 V/div), CH3 = V_{OUT}, CH4 = i_{LED} (200 mA/div).

By using the patented Pre-Emptive Boost (PEB) control algorithm, the A80601 can achieve minimum PWM dimming on-time down to 300 ns under nominal application conditions. This translates to PWM dimming ratio up to 15,000:1 at the PWM dimming frequency of 200 Hz. Technical details on PEB will be explained in the next section.

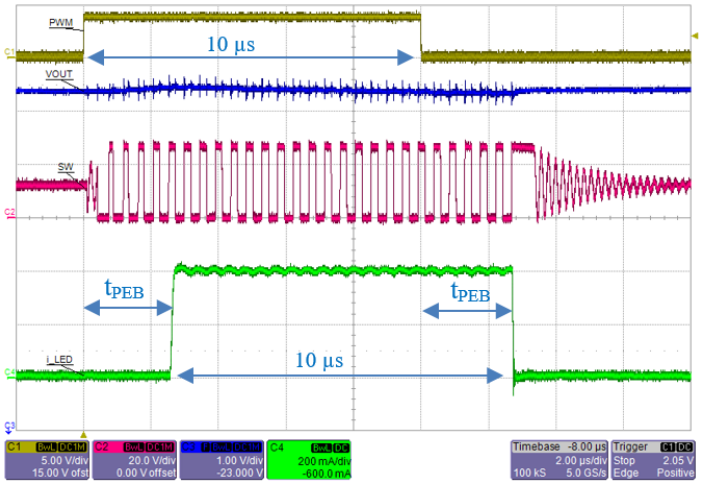

Figure 18: Zoom in view for PWM on-time = 10 µs. Notice that the LED current is shifted with respect to PWM signal. Ripple at V_{OUT} is ~0.2 V when using 2 × 4.7 µF MLCC as output capacitors.

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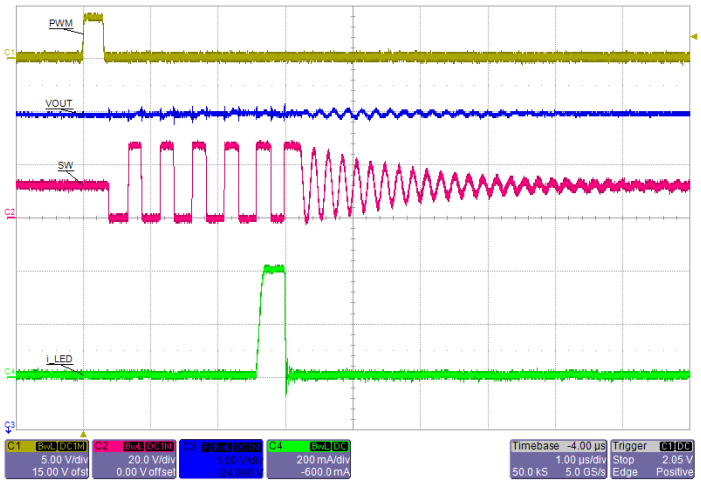

Figure 19: Zoom-in view showing A80601 is able to regulate LED current at PWM on-time down to 300 ns.

The typical PWM dimming frequencies fall between 200 Hz and 1 kHz. There is no hard limit on the highest PWM dimming frequency that can be used. However, at higher PWM frequency, the maximum PWM dimming ratio will be reduced. This is shown in the following table:

Table 4: Maximum PWM Dimming Ratio that can be achieved when operating at different PWM Dimming Frequency

PWM Frequency	PWM Period	Maximum PWM Dimming Ratio
200 Hz	5 ms	15,000:1
1 kHz	1 ms	3,000:1
3.3 kHz	300 µs	1,000:1
20 kHz	50 µs	150:1

While it is possible to operate with very high PWM duty cycle for subtle dimming, it is important to avoid PWM pulse low periods that are shorter than the Minimum PWM Off-Time ($t_{PWM-LOW}$), which is 1 µs. Driving PWM at 100% is acceptable.

Pre-Emptive Boost

The basic principle of pre-emptive boost (PEB) can be best explained by the following two waveforms. The first one shows how a conventional LED driver operates during PWM dimming operation. The second one shows that of the A80601.

Common test conditions for both cases:

PWM = 1% at 1 kHz (on-time = 10 µs), f_{SW} = 2.15 MHz, L = 10 µH, V_{IN} = 12 V, LED load = 8 series (V_{OUT} = ~25 V) at 100 mA × 4. C_{OUT} = 2 × 4.7 µF 50 V 1210 MLCC. COMP: R_Z = 280 Ω, C_Z = 68 nF.

Common scope settings:

CH1 (Yellow) = PWM (5 V/div); CH2 (Red) = Inductor current (500 mA/div); CH3 (Blue) = V_{OUT} (1 V/div); CH4 (Green) = LED current (200 mA/div); time scale = 2 µs/div.

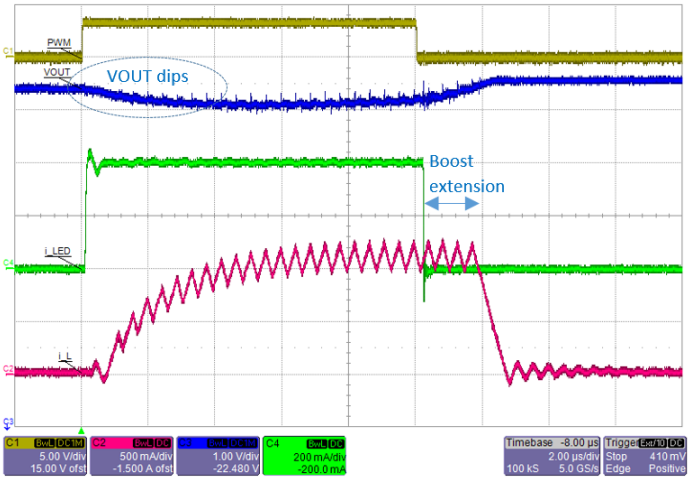

Figure 20: Traditional PWM Dimming operation where boost switch and LED current are enabled at the same time. Note that V_{OUT} shows overall ripple of ~0.5 V

When PWM signal goes high, a conventional LED driver turns on its boost switching at the time with LED current sinks. The problem is that the inductor current takes several switching cycles to ramp up to its steady-state value before it can deliver full power to the output load. During the first few cycles, energy to the LED load is mainly supplied by the output capacitor, which results in noticeable dip in output voltage.

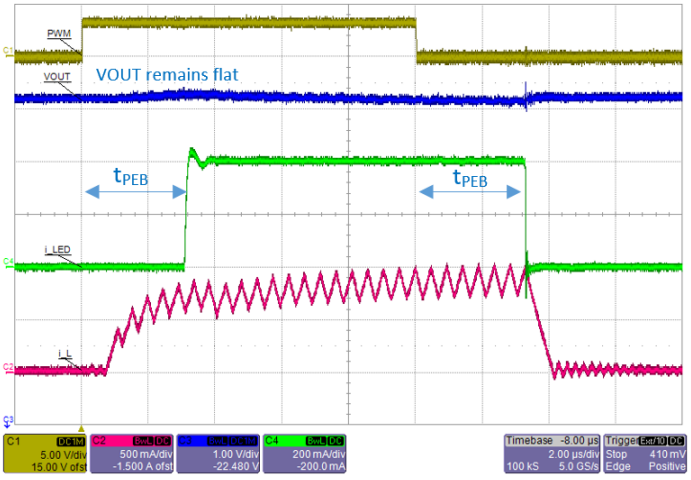

Figure 21: A80601 PWM dimming operation with PEB delay set to 3 µs. Note that V_{OUT} ripple is reduced to ~0.2 V.

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In the A80601, the boost switch is also enabled when PWM goes high. However, the LED current is not turned on until after a short delay of t_{PEB}. This allows the inductor current to build up before it starts to deliver the full power to LED load. During the pre-boost period, V_{OUT} bumps up very slightly, while the following dip is essentially eliminated. When PWM goes low, both boost switching and LED remains active for the same delay of t_{PEB}. Therefore, the PWM on-time is preserved in LED current.

PEB delay can be programmed using an external resistor, R_{PEB}, from PEB pin to GND. Their relationship is shown in the following chart:

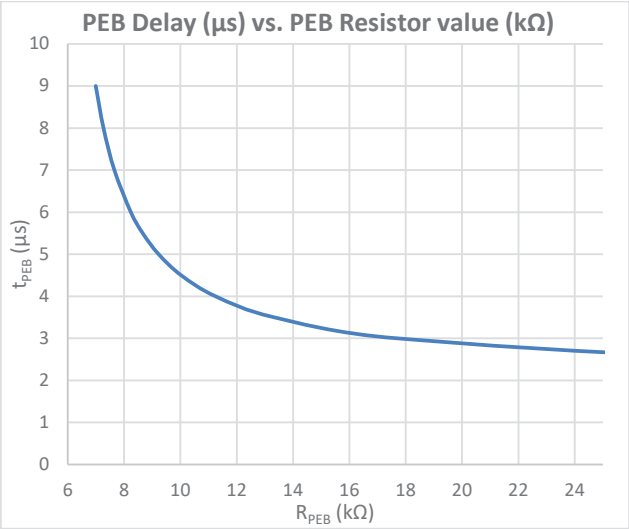

Figure 22: How PEB delay time varies with value of PEB pin resistor to GND.

Ideally, t_{PEB} is equal to the inductor current ramp up time. But the latter is affected by many external parameters, such as switching frequency, inductance, V_{IN} and V_{OUT} ratio, etc. Therefore, some experimentation is required to optimize the PEB delay time. In general, for switching frequency at 2 MHz, t_{PEB} = 2.5 to 4 µs is a good starting point.

The advantage of PEB is that even a non-optimized delay time can significantly reduce the output ripple voltage compared to a conventional LED driver.

Analog Dimming

The peak (100%) level of LED current is set by the R_{ISET} resistor. The actual peak LED current may also be adjusted continuously from approximately 10% up to 100%, by using the ADIM pin. There are two methods to do so:

1. In ADIM mode: apply a DC voltage between 0.2 V and 2 V at the pin.
2. In APWM mode: apply a clock signal with required duty cycle at the pin.

ADIM MODE

An analog voltage is applied at the ADIM pin. This DC voltage linearly controls the peak LED current, as illustrated by the chart below:

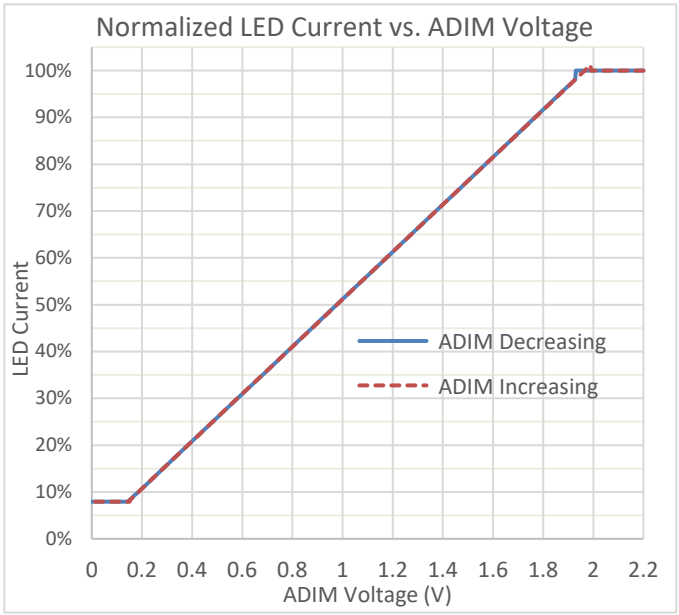

Figure 23: In analog dimming mode, the LED current is linearly proportional to ADIM voltage between 0.2 V and 2 V approximately

There is an internal pull-down resistor (50 kΩ typical) from ADIM pin to GND. When this pin is left floating, LED current is actually being dimmed down to ~10%. Therefore, if analog dimming is not required, the ADIM pin should be pulled to over 2 V (but below V_{DD}) to ensure 100% LED current. One simple technique is to pull up ADIM to VDD through a 30 kΩ resistor.

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APWM MODE

When a clock signal is detected at ADIM pin, the A80601 goes into APWM mode. The typical APWM signal frequency is between 40 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current delivered to the LED. The relationship is shown below:

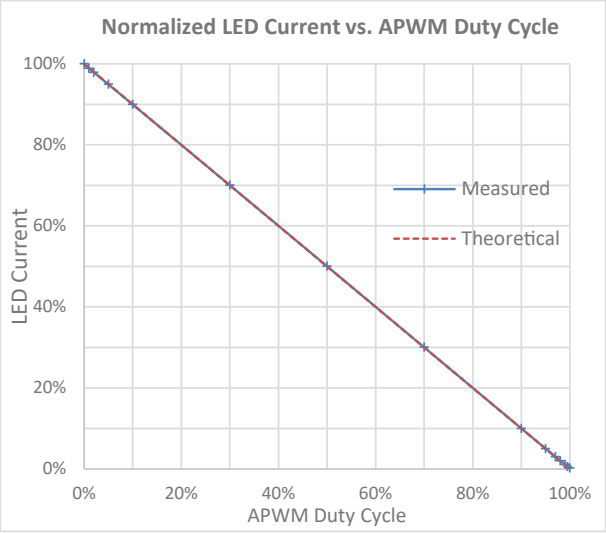

Figure 24: Showing LED current is inversely proportional to the APWM duty cycle. Test conditions: V_{IN} = 12 V, V_{OUT} = 25 V (8 × WLED), total LED current = 100 mA × 4, APWM frequency = 100 kHz

As an example, a system that delivers a full LED current of 100 mA per channel would deliver 75 mA when an APWM signal with a duty-cycle of 25% is applied (because analog dimming level is 100% – 25% = 75%). This is demonstrated by the following waveforms.

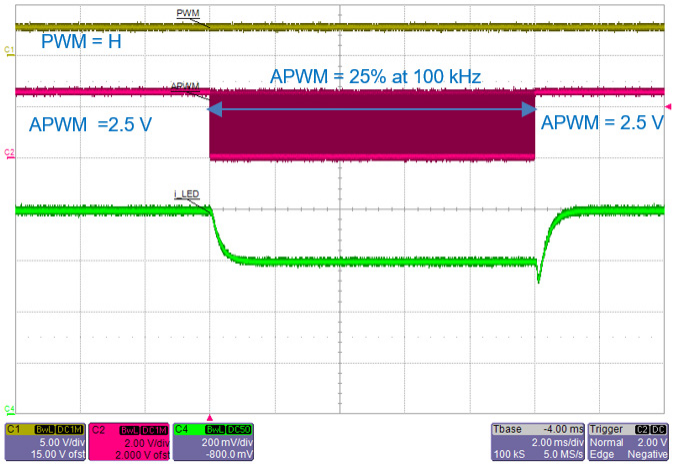

Figure 25: PWM = H. Total LED current drops from 400 mA (4 × 100 mA/ch) to 300 mA when APWM of 25% duty cycle is applied. Note that LED current takes ~0.5 ms to settle after change in APWM.

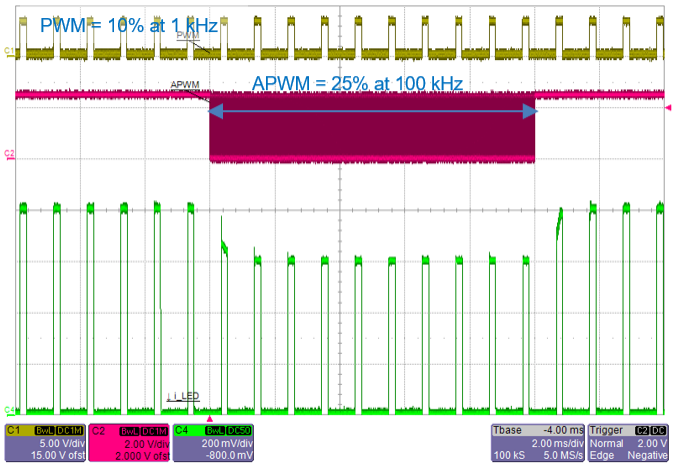

Figure 26: PWM = 25% at 1 kHz. Peak LED current drops from 400 mA (4 × 100 mA/ch) to 300 mA when APWM of 25% duty cycle is applied

While in APWM mode, if a clock pulse is not detected within ~50 µs, the IC will fall back to ADIM mode. To ensure reliable detection of APWM clock, its on-time and off-time must be at least 150 ns. Therefore, the allowable APWM duty cycle range is dependent on the APWM frequency, as shown in the table below:

Table 5: Acceptable Duty Cycle range for APWM clock at various frequencies

APWM Frequency	APWM Duty Cycle
40 kHz	0.6% to 99.4%
100 kHz	1.5% to 98.5%
300 kHz	4.5% to 95.5%
1 MHz	15% to 85%

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One popular application of analog dimming is for LED brightness calibration, commonly known as 'LED Binning'. LEDs from the same manufacturer and series are often grouped into different 'bins' according to their light efficacy (lumens per watt). It is therefore necessary to calibrate the '100% current' for each LED bin, in order to achieve uniform luminosity.

To use ADIM pin as a trim function, the user should first set the 100% current based on efficacy of LED from the lowest bin. When using LED with higher efficacy, the required current is then trimmed down to the appropriate level using APWM duty cycle.

As an example, assume that:

- LED from lowest bin has an efficacy of 80 lm/W
- LED highest bin has an efficacy of 120 lm/W

Suppose the maximum LED current was set at 100 mA based on LEDs from lowest bin. When using LEDs from highest bin, the current should then be reduced to 67% (80/120). This can be achieved by sending APWM clock with 33% duty cycle.

Extending LED Dimming Ratio

The dynamic range of LED brightness can be further extended, by using a combination of PWM duty cycle, APWM duty cycle, and analog dimming method.

For example, the following approach can be used to achieve a 100,000:1 dimming ratio at 200 Hz:

- Vary PWM duty cycle from 100% down to 0.01% to give 10,000:1 dimming. This requires PWM dimming on-time be reduced down to 0.5 µs.

With PWM dimming on-time fixed at 0.5 µs, reduce peak LED current from 100% down to 10%. This can be achieved by either:

- Apply a clock signal at ADIM pin, and vary its duty cycle from 1.5% to 90% (at 100 kHz), or
- Apply a DC voltage at ADIM pin, and vary its level from 2 V down to 0.2 V.

The net result of using both PWM and APWM is 100,000:1 dimming ratio, as shown in the chart below

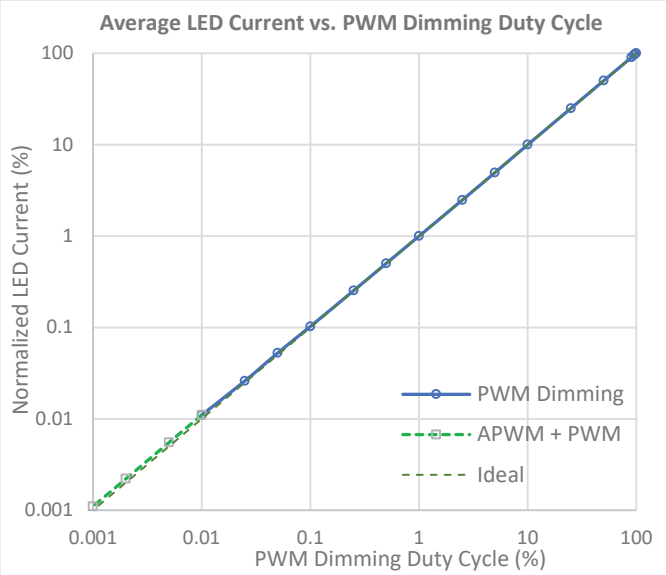

Figure 27: How to achieve 100,000:1 dimming ratio by using both PWM and APWM. Test conditions: V_{IN} = 12 V, V_{OUT} = 25 V (8 × WLED), total LED current = 400 mA, PWM frequency = 200 Hz, APWM frequency = 100 kHz.

Note that the A80601 is capable of providing analog dimming range greater than 10:1. By applying APWM with 96% duty cycle, for example, an analog dimming range of 25:1 can be achieved. However, this requires the external APWM signal source to have very fine pulse-width resolution. At 200 kHz APWM frequency, a resolution of 50 ns is required to adjust its duty cycle by 1%.

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Analog Dimming with External Voltage

Besides using ADIM pin, the LED current can also be reduced by using an external voltage source applied through a resistor to the ISET pin. The dynamic range of this type of dimming is dependent on the ISET pin current. The recommended i_{SET} range is from 20 µA to 144 µA for the A80601. Note that the IC will continue to work at i_{SET} below 20 µA, but the relative error in LED current becomes larger at lower dimming level.

Below is a typical application circuit using a DAC (digital-analog converter) to control the LED current. The ISET current (which directly controls the LED current) is normally set as V_{ISET}/R_{ISET}. The DAC voltage can be higher or lower than V_{ISET}, thus adjusting the LED current to a lower or higher value.

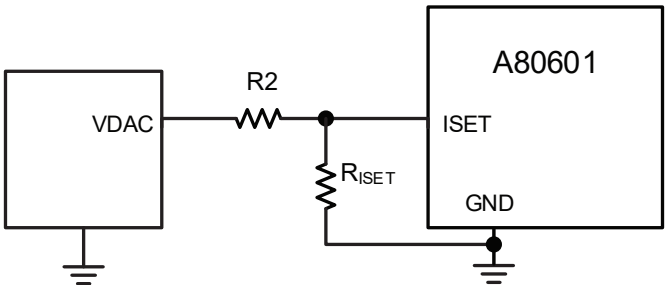

Figure 28: Adjusting LED current with an external voltage source

Equation 5:

$$i_{ISET} = \frac{V_{ISET}}{R_{ISET}} - \left[\frac{VDAC - V_{ISET}}{R2}\right]$$

where V_{ISET} is the ISET pin voltage (typically 1.0 V), and VDAC is the DAC output voltage.

When VDAC is higher than 1.00 V, the LED current is reduced. When VDAC is lower than 1.00 V, the LED current is increased.

Some common applications for the above scheme include:

- LED binning
- Thermal fold-back using external NTC (negative temperature coefficient) thermistor

In the following application example, the thermistor used is NTCS0805E3684JXT (680 kΩ @ 25°C). R1 = 336 kΩ, R2 = 20 kΩ, and R3 = 8.45 kΩ. The LED current per channel is reduced from 97 mA at 25°C to 34 mA at 125°C.

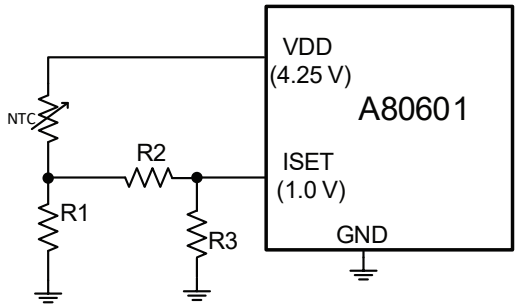

Figure 29: Thermal foldback of LED current using NTC thermistor

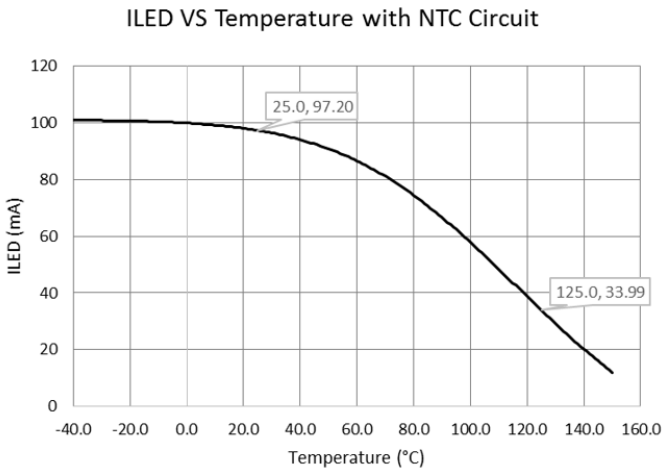

Figure 30: LED current varies with temperature when using thermistor NTCS0805E3684JXT for thermal foldback

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VDD

The VDD pin provides regulated bias supply for internal circuits. Connect a C_{VDD} capacitor with a value of 1 µF or greater to this pin. The internal LDO can deliver up to 2 mA of current externally with a typical VDD voltage of about 4.25 V. This allows it to serve as the pull up voltage for FAULT pin.

VDRV

The VDRV pin provides a regulated gate driver supply for external boost power MOSFET. Connect a C_{VDRV} capacitor with a typical value of 2.2 µF to this pin. The gate driver can deliver up to 2 A of peak sink and source current, with a typical V_{DRV} voltage of 6.5 V. However, its average output current is limited to approximately 36 mA. Note that average gate driver current is:

Equation 6: $$i_{VDRV} = f_{SW} \times Q_G$$

where f_{SW} is the switching frequency and Q_G is the total gate charge of the power MOSFET for V_{GS} = 0 to 6.5 V.

At higher switching frequency, it is important to select a power MOSFET with low Q_G to limit the average gate driver current. Refer to the appendix section for details on MOSFET selection.

Shutdown

If EN pin is pulled low for longer than $t_{EN(OFF)}$ (~16 ms), the A80601 enters shutdown (sleep mode). The next time EN pin goes high, all internal fault registers are cleared. The IC needs to go through a complete soft start process after PWM goes high.

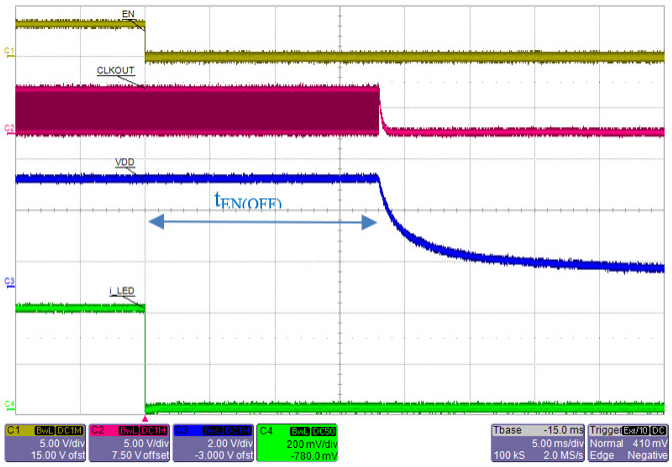

Figure 31: After EN = L for ~16 ms, the IC completely shuts down so VDD (Blue) decays.

There is an alternative way to reset the internal fault status registers. By keeping EN = H and PWM = L for longer than 16 ms, the A80601 clears all internal fault registers but does not go into sleep mode. The next time PWM pin goes high, the IC will still go through soft start process. The difference is that VDD voltage and CLKOUT signal are always available as long as EN = H.

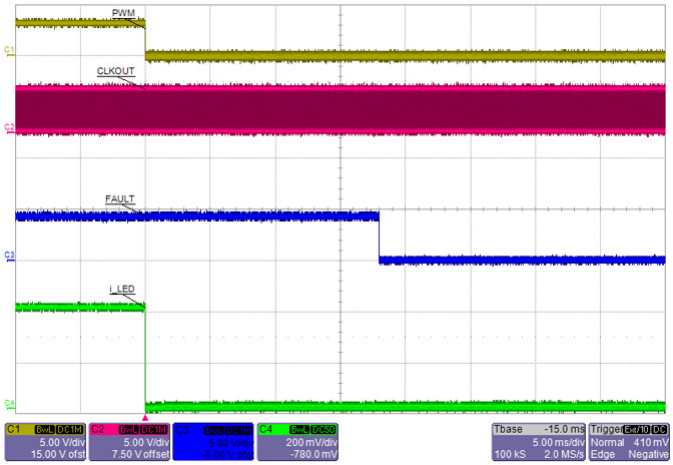

Figure 32: As long as EN = H, the IC does not shut down VDD and CLKOUT. But internal latched faults are cleared by PWM = L for ~16 ms.

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FAULT DETECTION AND PROTECTION

FAULT Status

The FAULT pin is an open-drain output that will be pulled low when a fault occurs. A pull-up resistor (typically around 10 kΩ) is required between this pin and desired logic level voltage (typically 3.3 to 5 V). Multiple devices with open-drain FAULT pins can be connected in parallel to form a wired-AND configuration. This way, when any device reports a fault, the system FAULT signal is pulled low.

The A80601-1 (One-Out-All-Out option) has a bidirectional FAULT pin. This means the same pin also serves as an input to monitor the status of system FAULT signal. When the FAULT pin is pulled low externally for >8 f_{SW} cycles by another device, the A80601-1 disables its own boost switch and all LED current sinks in response. This feature is required in Master/Slave configuration, for example.

The following two simplified flow charts demonstrate the difference between A80601 (unidirectional FAULT pin) and A80601-1 (bidirectional FAULT pin).

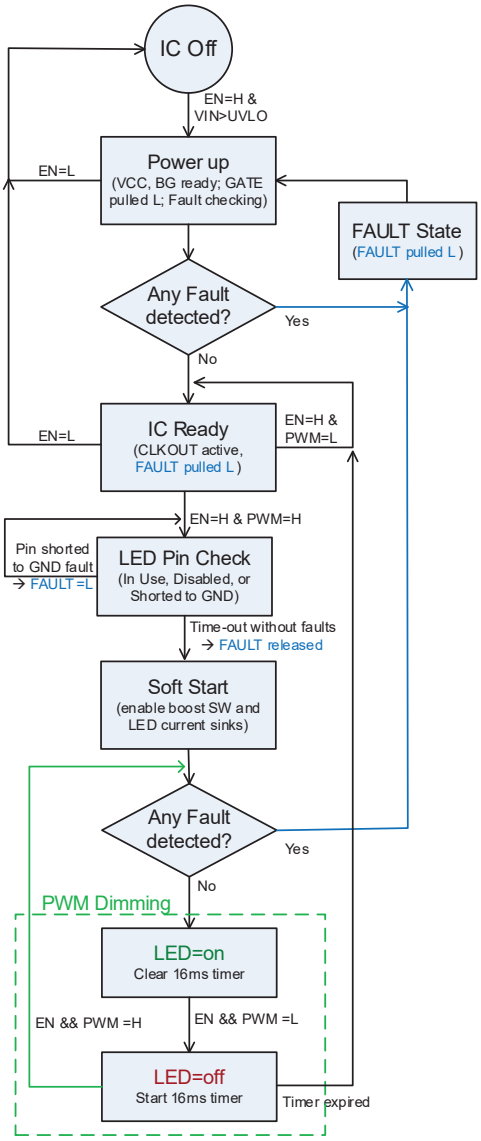

Figure 33: Simplified A80601 Startup Flowchart

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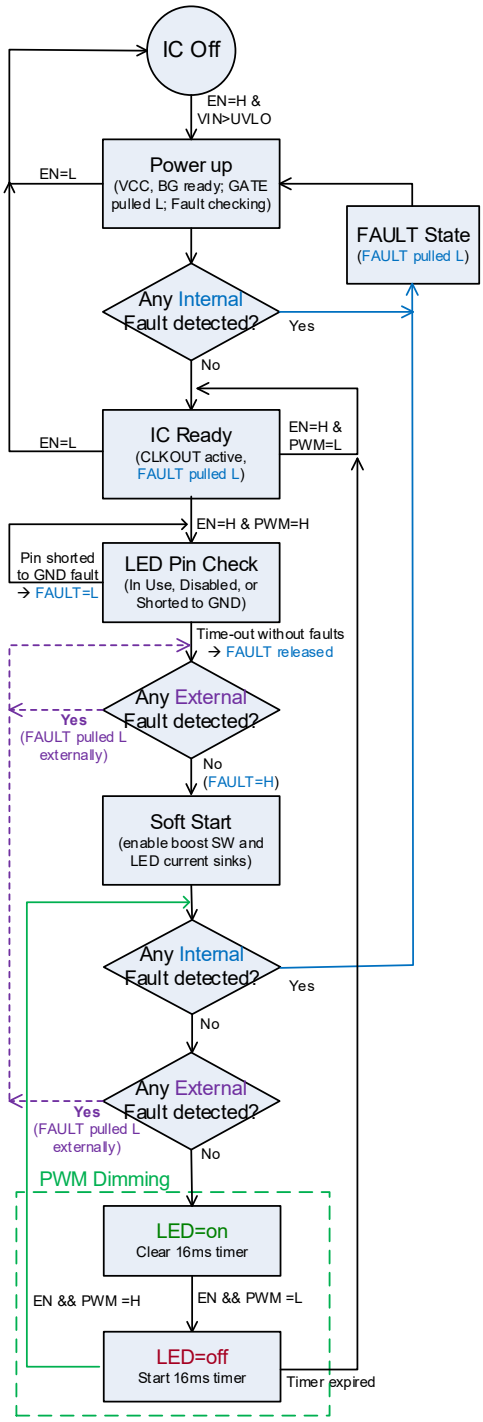

Figure 34: Simplified startup flow chart for A80601-1, showing responses to both Internal and External FAULT signals

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LED String Partial-Short Detect

All LED current sink pins (LED1 to LED4) are designed to withstand the maximum output voltage, as specified in the Absolute Maximum Ratings table. This prevents the IC from being damaged if V_{OUT} is directly applied to an LED pin due to an output connector short.

In case of direct-short or partial-shorted fault in any LED string during operation, the LED pin with voltage exceeding V_{LEDSD} will be removed from regulation. This prevents the IC from dissipating too much power due to large voltage drop across the LED current sink.

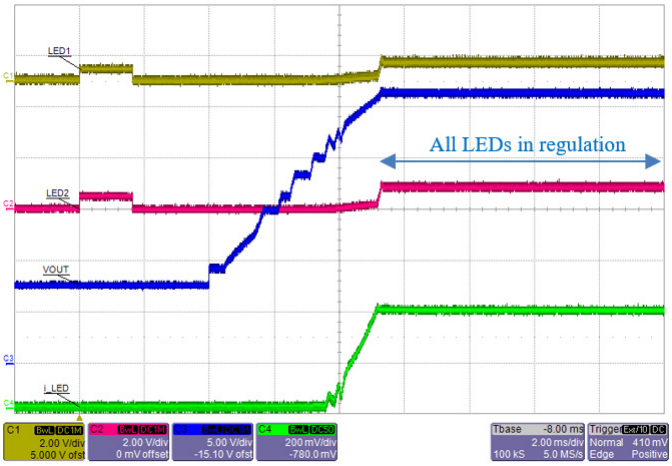

Figure 35: A80601 Normal startup sequence showing voltage at LED1 and LED2 pins. V_{IN} = 6 V, output = 8 × WLED in series, current = 4 × 100 mA

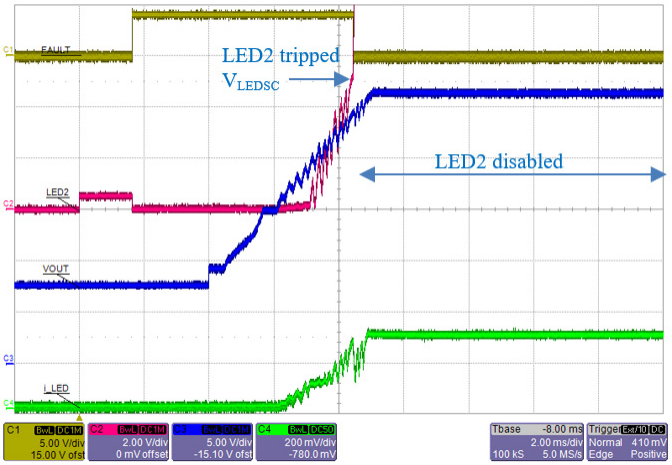

Figure 36: A80601 startup sequence when LED string#2 has a partial-short fault (6 × WLED instead of 8). As soon as LED2 pin rises above V_{LEDSC} (~5 V), the channel is disabled and FAULT = Low.

For A80601, the FAULT pin is pulled low in case any LED string is directly or partially shorted. The suspect LED string is disabled, while the rest of the LED strings continue to operate. FAULT pin is latched at low until it is reset by either EN = L or PWM = L for >16 ms

For A80601-1, all LED strings are turned off in case any LED string has detected a partial short. FAULT pin is latched at low until the IC is reset.

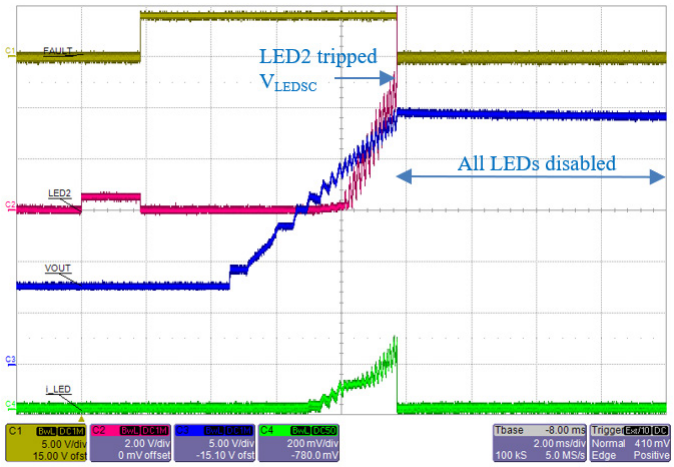

Figure 37: A80601-1 startup sequence when LED string#2 has a partial-short fault (6 × WLED instead of 8). As soon as LED2 pin rises above V_{LEDSD} (~5 V), the channel is disabled but FAULT remains High.

At least one LED pin must be at regulation voltage (below ~1.2 V) for the LED string partial-short detection to activate. In case all the LED pins are above regulation voltage (this could happen when the input voltage rises too high for the LED strings), they will continue to operate normally.

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Overvoltage Protection

The A80601 offers a programmable output overvoltage protection (OVP). The OVP pin has a threshold level of 2.5 V typical. Overvoltage protection is tripped when current into this pin exceeds ~150 µA. A resistor can be used to set the OVP threshold up to 40 V approximately. This is sufficient for driving 11 white LEDs in series.

The formula for calculating the OVP resistor is shown below:

Equation 7: $$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / i_{OVP(th)}$$

where V_{OVP} is the desired OVP threshold, $V_{OVP(th)}$ = 2.5 V typical, $i_{OVP(th)}$ = 150 µA typical.

To determine the desired OVP threshold, take the maximum LED string voltage at cold and add ~10% margin on top of it.

The OVP event is not a latched fault and, by itself, does not pull the FAULT pin to low. If the OVP condition occurs during a load dump, for example, the IC will stop switching but not shut down.

OVP condition is typically caused by an open LED fault, or disconnected output connector. It may be detected either at startup or during normal operation. This is explained separately below.

CASE 1: OVP AT STARTUP

During soft start period, the A80601 tries to boost V_{OUT} until it becomes high enough for all LED string to come into regulation. But if any LED string is open, V_{OUT} will eventually hit OVP. At this point, the A80601 will disable any LED string that is still not in regulation. The FAULT pin is pulled low and boost switching is stopped to allow V_{OUT} to fall. Once V_{OUT} falls below ~97% OVP, switching resumes to power the remaining LED strings.

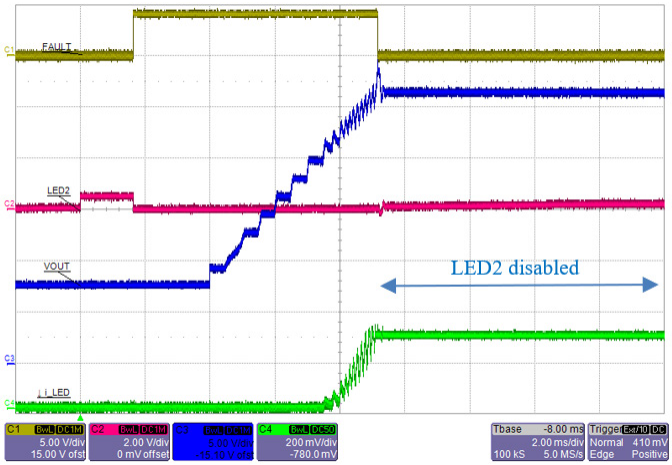

Figure 38: A80601 startup with LED2 string open. V_{OUT} hits OVP at ~28 V and LED2 is removed from regulation. FAULT pin goes Low but remaining LED strings continue to operate.

For A80601-1, all LED strings are disabled in case any string is not in regulation when V_{OUT} hits OVP. FAULT pin is pulled low and switching is stopped. The IC remains in latched off state until it is reset.

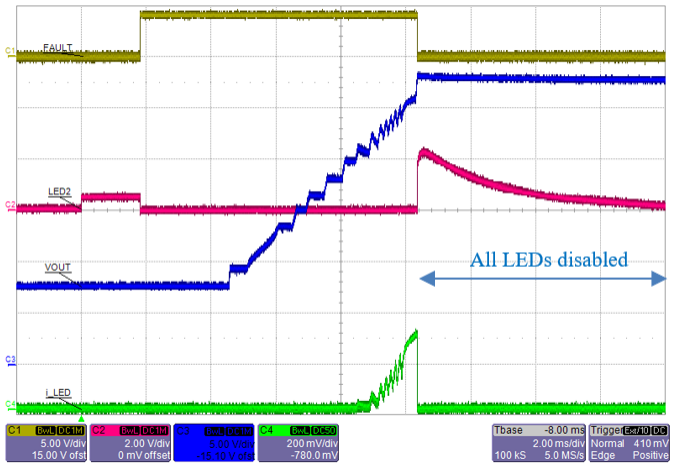

Figure 39: A80601-1 startup with LED2 string open. V_{OUT} hits OVP and all LED string are disabled. FAULT pin goes Low and IC remains latched off until reset.

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CASE 2: OVP DURING NORMAL OPERATION

When one LED string becomes open during operation, current through its LED driver drops to zero. The A80601 responds by boosting the output voltage higher. When output reaches OVP threshold, the LED string without current is removed from regulation. The rest of LED strings continue to draw current and drain down V_{OUT}. Once V_{OUT} falls below ~97% OVP, boost will resume switching to power the remaining LED strings.

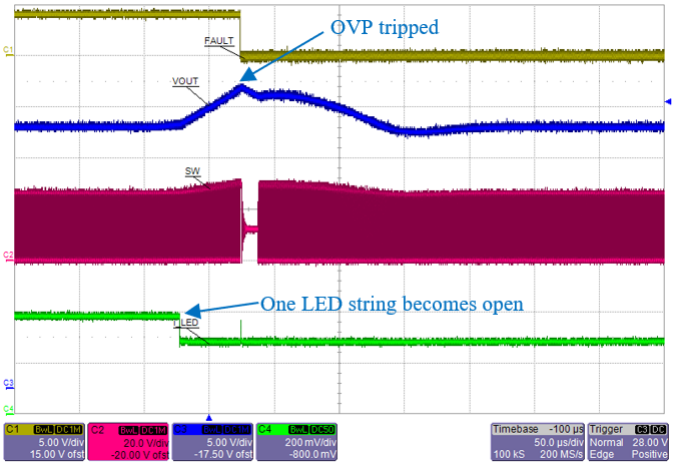


Figure 40: An open-LED string faults causes VOUT to ramp up and trip OVP. The A80601 then disables the open LED string and continues with remaining strings.

The A80601-1, in contrast, will disable all LED strings in case any LED string becomes open. The IC remains in latched off state until it is reset.

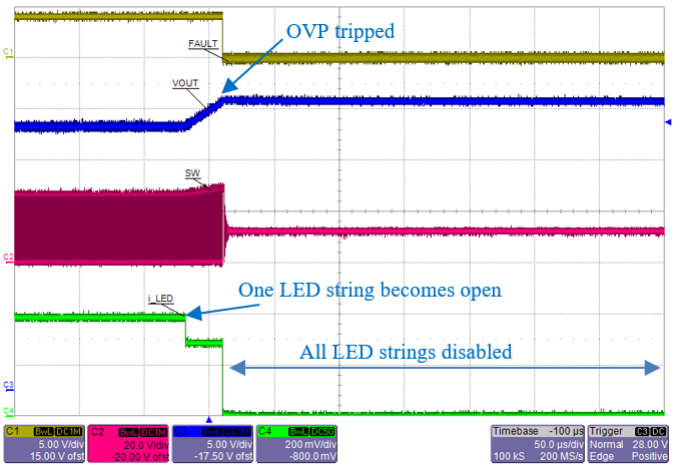


Figure 41: An open-LED string faults causes VOUT to ramp up and trip OVP. The A80601-1 then disables all LED string and remains in latched off state until reset.

Boost Switch Overcurrent Protection

The external boost switch is protected with a cycle-by-cycle primary current limit. When the voltage sensed at CS pin exceeds $V_{CS(LIM1)}$ (typically 210 mV), the existing switching cycle is truncated. For a desired peak switch current limit, $I_{SW(LIM1)}$, the current sense resistor, R_{CS}, can be calculated with the following:

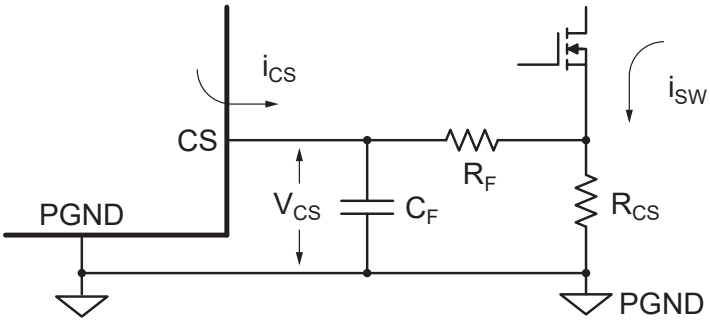
Equation 8: $$R_{CS} = V_{CS(LIM1)} / I_{SW(LIM1)}$$

R_{CS} is connected from source of boost MOSFET to power ground and must be adequately sized to handle the power dissipation.

As an example, if R_{CS} = 39 mΩ, then $i_{SW(LIM1)}$ = 5.4 A approximately.

EFFECTS OF ADDING CS PIN RC FILTER

With proper PCB layout, no external filtering is required for CS pin. If desired, however, a simple RC filter may be added to CS pin as shown below:



$$V_{CS} = i_{CS} \times R_F + i_{SW} \times R_{CS}$$

$$R_{CS} = \frac{V_{CS(LIM)} - i_{CS} \times R_F}{i_{SW(LIM)}}$$

Figure 42: Adding CS pin RC filter

Note that there is a bias current (approximately 100 µA) flowing out of CS pin. This introduces an offset to the boost switch OCP limit. Therefore the following guidelines are recommended:

- Keep $R_F \leq 100\ \Omega$ to minimize its effect on OCP limit.
- Keep $R_F \times C_F \leq 100$ ns (that means max C = 1 nF when R = 100 Ω).

EXAMPLE SWITCHING CURRENT WAVEFORMS

The waveform below shows normal switching at V_{IN} = 6 V, V_{OUT} = ~26 V and total LED current 800 mA. Average input current is around 4.5 A.

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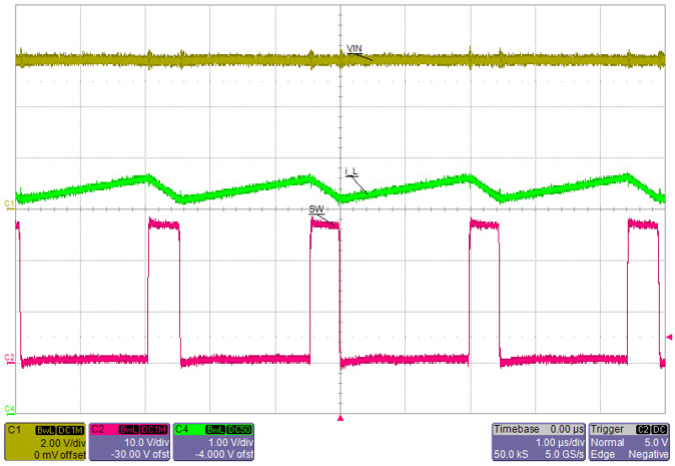


Figure 43: Normal 400 kHz switching waveform at V_{IN} = 6 V. Red trace is the SW node voltage at 10 V/div. Green trace is the inductor current at 1 A/div.

When the input voltage is reduced further to 5.6 V, input current increases and peak switch current reaches 5.4 A. Overcurrent protection is tripped to limit the peak SW current.

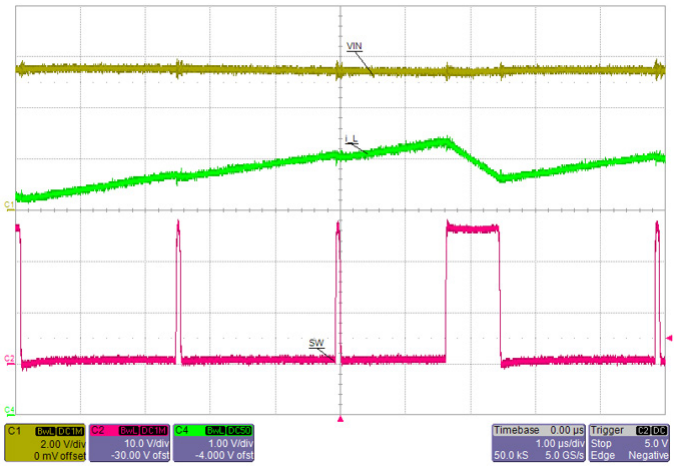
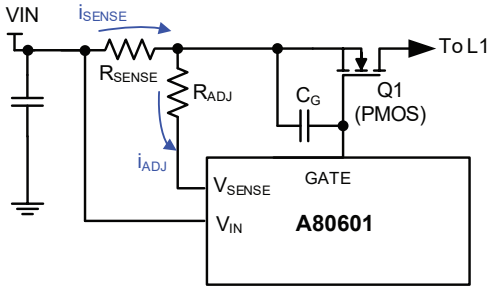


Figure 44: When peak current through the inductor reaches ~5.4 A, overcurrent protection kicks in to truncate the present switching cycle.

There is also a secondary current sense limit $V_{CS(LIM2)}$, set at about 40% higher than the cycle-by-cycle current limit. It is to protect the external MOSFET from destructive current spikes in case the boost inductor or boost diode is shorted. Once this limit is tripped, the A80601 will immediately shut down and latch off.

Input Overcurrent Protection and Disconnect Switch



$$V_{IN} - V_{SENSE} = R_{SC} \times i_{SENSE} + R_{ADJ} \times i_{ADJ}$$

Figure 45: Optional input disconnect switch using a PMOSFET

The primary function of the input disconnect switch is to protect the system and the device from excessive input currents during a fault condition.

If the input current level goes above the preset threshold, the part will be shut down in less than 3 µs. The FAULT pin is pulled Low and the IC remains in latched off state until it is reset. This feature prevents catastrophic failure in the system when there is a direct short from VOUT to GND (caused by a shorted output connector or cable, for example).

The waveform below illustrates the input overcurrent fault condition during startup. As soon as input OCP limit is reached, the part disables the gate of the disconnect switch Q1 and latches off.

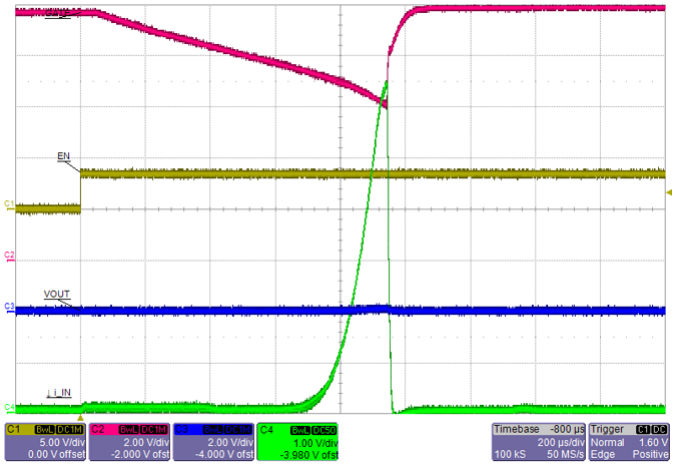


Figure 46: Startup into an output shorted-to-GND fault. Input OCP is tripped when current (Green trace) exceeds ~6.5 A. PMOS Gate (Red) is turned off immediately and IC latches off.

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During startup when Q1 first turns on, an inrush current flows through Q1 into the output capacitance. If Q1 turns on too fast (due to its low gate capacitance), the inrush current may trip input OCP limit. In this case, an external gate capacitance C_G is added to slow down the turn-on transition. Typical value for C_G is around 4.7 to 22 nF. Do not make C_G too large, since it also slows down the turn-off transient during a real input OCP fault.

Setting the Input Current Sense Resistor

The input disconnect switch threshold is typically 98 mV, measured between VIN and VSENSE pins when R_{ADJ} is 0 Ω. This threshold can be trimmed slightly using the R_{ADJ} resistor.

To avoid false tripping, the input disconnect switch overcurrent limit should be set higher than the boost switch cycle-by-cycle current limit. For example, the boost switch OCP is set at 5.4 A, so the input disconnect switch OCP may be set 25% higher at 6.75 A. The input current sense resistor is then calculated as below.

When R_{ADJ} is not used:

$$V_{IN} - V_{SENSE} = R_{SENSE} \times i_{SENSE} = 98\ mV$$

The desired sense resistor is R_{SENSE} = 98 mV / 6.75 A = 14.5 mΩ. But this is not a standard E-24 resistor value. Pick the closest lower value which is 13 mΩ.

When R_{ADJ} is used:

$$V_{IN} - V_{SENSE} = R_{SENSE} \times i_{SENSE} + R_{ADJ} \times i_{ADJ}$$

Therefore

$$R_{ADJ} = [(V_{IN} - V_{SENSE}) - (R_{SENSE} \times i_{SENSE})] / i_{ADJ}$$
$$= [98\ mV - 88\ mV] / 20\ \mu A = 500\ \Omega$$

Pick the closest E-96 resistor value of 499 Ω.

Input UVLO

When V_{IN} rises above $V_{UVLOrise}$ threshold, the A80601 is enabled. The IC is disabled when V_{IN} falls below $V_{UVLOfall}$ threshold for more than 50 µs. This small delay is used to avoid shutting down because of momentary glitches in the input power supply.

Fault Protection During Operation

The A80601 constantly monitors the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in the table below. It is important to note that there are several points at which the A80601 monitors for faults during operation. The locations are input current, switch current, output voltage, switch voltage, and LED pins. Some of the protection features might not be active during startup to prevent false triggering of fault conditions.

The possible fault conditions that the part can detect include:

- Open LED Pin or open LED string
- Shorted or partially shorted LED string
- LED pin shorted to GND
- Open or shorted boost diode
- Open or shorted boost inductor
- VOUT short to GND
- SW shorted to GND
- ISET shorted to GND
- FSET shorted to GND
- Input disconnect switch drain shorted to GND

Note that some of these faults will not be protected if the input disconnect switch is not being used. An example of this is VOUT short to GND fault.

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Table 6: A80601 Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost Switch	Disconnect Switch	LED Sink drivers
Primary Switch Overcurrent Protection (Cycle-By-Cycle Current Limit)	Auto-restart	Always	NO	This fault condition is triggered when the SW current exceeds the cycle-by-cycle current limit, $I_{SW(LIM)}$.The present SW on-time is truncated immediately to limit the current. Next switching cycle starts normally.	Off for a single cycle	ON	ON
Secondary Switch Current Limit	Latched Off	Always	YES	When current through boost switch exceeds secondary SW current limit ($i_{SW(LIM2)}$) the device immediately shuts down the disconnect switch, LED drivers and boost. The Fault flag is set. To reset the fault the EN or PWM pin needs to be pulled low for ~16 ms.	OFF	OFF	OFF
Input Disconnect Current Limit	Latched Off	Always	YES	The device is immediately shut off if the voltage across the input sense resistor is above the $V_{SENSEtrip}$ threshold. To reset the fault the EN or PWM pin must be pulled low for ~16 ms.	OFF	OFF	OFF
LEDx Pin Shorted to GND	Auto-restart	Startup	YES	If any of the LED pins is determined to be shorted to GND when PWM first goes high, soft-start process is halted. Only when the short is removed, then soft-start is allowed to proceed.	OFF	ON	OFF
LEDx Pin Open (One-Out-Continue option)	Auto-restart	Normal operation	YES	If an LED string is not getting enough current, the device will first respond by increasing the output voltage until OVP is reached. Any LED string that is still not in regulation will be disabled. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	ON	ON	OFF for open pins. ON for all others.
LEDx Pin Open (One-Out-All-Out option)	Latched	Normal operation	YES	If an LED string is not getting enough current, the device will first respond by increasing the output voltage until OVP is reached. If any LED string is still not in regulation, all LED strings will be disabled and the device latched off. To reset the fault the EN or PWM pin must be pulled low for ~16 ms.	OFF	OFF	OFF
ISET Short Protection	Auto-restart	Always	YES	Fault occurs when the ISET current goes above 150% of max current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to regulate to the preset LED current.	OFF	ON	OFF
FSET/SYNC Short Protection	Auto-restart	Always	YES	Fault occurs when the FSET current goes above 150% of max current. The boost will stop switching, Disconnect switch will turn off and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to restart with soft-start.	OFF	ON	OFF
Overvoltage Protection	Auto-restart	Always	NO	Fault occurs when current into OVP pin exceeds $i_{OVP(th)}$ (typically 150 µA). The IC will immediately stop switching but keep the LED drivers active, to drain down the output voltage. Once the output voltage decreases to ~94% OVP level, the IC will restart switching to regulate the output current.	STOP during OVP event.	ON	ON
Undervoltage Protection	Auto-restart	Always	YES	Device immediately shuts off boost and current sinks if the voltage at VOUT is below $V_{UVP(th)}$. This may happen if VOUT is shorted to GND, or boost diode is open before startup. It will auto-restart once the fault is removed.	OFF	ON	OFF
LED String Partial Short Detection (One-Out-Continue option)	Auto-restart	Always	YES	Fault occurs if an LED pin voltage exceeds V_{LEDSC} with its current sink in regulation, while at least one other LED pin is below ~1.2 V. This may happen when two or more LEDs are shorted within a string. The LED string exceeding the threshold will be disabled and removed from operation. Device will re-enable the LED string when its pin voltage falls below threshold, or at the next PWM = H.	ON	ON	OFF for shorted string, ON for all others.
LED String Partial Short Detection (One-Out-All-Out option)	Latched	Always	YES	If two or more LEDs are shorted within a string, all LED strings will be disabled and the device latched off. To reset the fault, EN or PWM pin must be pulled low for ~16 ms.	OFF	OFF	OFF
Overtemperature Protection	Auto-restart	Always	YES	Fault occurs when the die temperature exceeds the over-temperature threshold, typically 170°C. IC will restart after temperatures drops lower by T_{SDHYS}	OFF	OFF	OFF
V_{IN} UVLO	Auto-restart	Always	NO	Fault occurs when V_{IN} drops below $V_{UVLO(fall)}$. This fault resets all latched faults.	OFF	OFF	OFF

Continued on next page...

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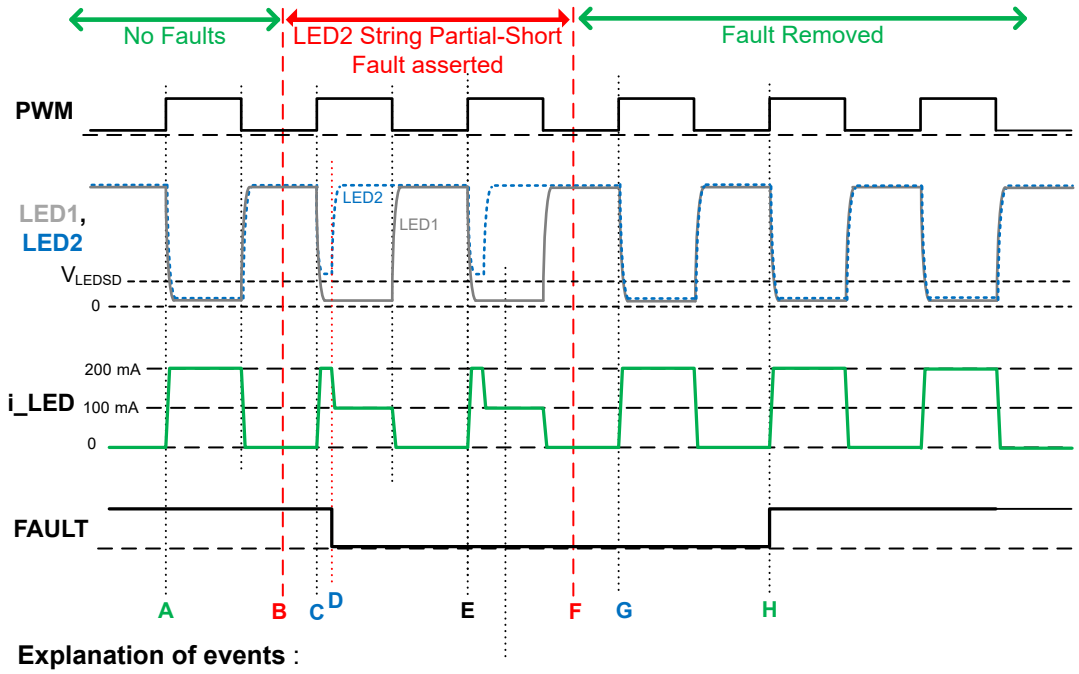
Table 6: A80601 Fault Mode Table (continued)

Fault Name	Type	Active	Fault Flag Set	Description	Boost Switch	Disconnect Switch	LED Sink drivers
FAULT pin pulled Low Externally (One-Out-Continue option)	Always ignored	Always ignored	No change	In One-Out-Continue mode (with unidirectional FAULT pin), external status of FAULT pin does not affect the operation of the IC in any way.	No change	No change	No change
FAULT pin pulled Low Externally (One-Out-All-Out option)	Auto-restart	Always	No change	In One-Out-All-Out mode (with bidirectional FAULT pin), if FAULT pin is externally pulled Low, the IC immediately shuts off its boost and LED current sinks. IC can only restart when external fault status is cleared AND there is no internal fault status pending. That means local latching faults cannot be cleared by externally forcing FAULT pin to High.	OFF	ON	OFF

LED String Partial-Short Detection in One-Out-Continue mode (A80601)



Explanation of events :

A: PWM goes High and all LED drivers operate normally. (For simplicity, assume only LED 1 and LED 2 are in use, each sinking 100 mA.)

B: A partial-short fault is asserted to LED 2 string. Nothing happens yet since PWM = L.

C: At the next PWM = H, LED2 pin voltage stays above V_{LEDSD} while LED 1 pin is at regulation voltage.

D: After partial-short detection time (~2 µs), LED2 string is disabled and FAULT pin pulled Low. LED1 string continues to operate.

E: At subsequent PWM = H, IC retries LED 1 but shuts it off again since the fault is still present. FAULT flag remains Low.

F: Partial Short fault is removed from LED 2 string. Nothing happens yet since PWM = L.

G: At the next PWM = H, IC retries LED 1 and it passes. But FAULT flag is not cleared

H: FAULT flag is cleared at the second PWM = H after Partial Short fault was removed.

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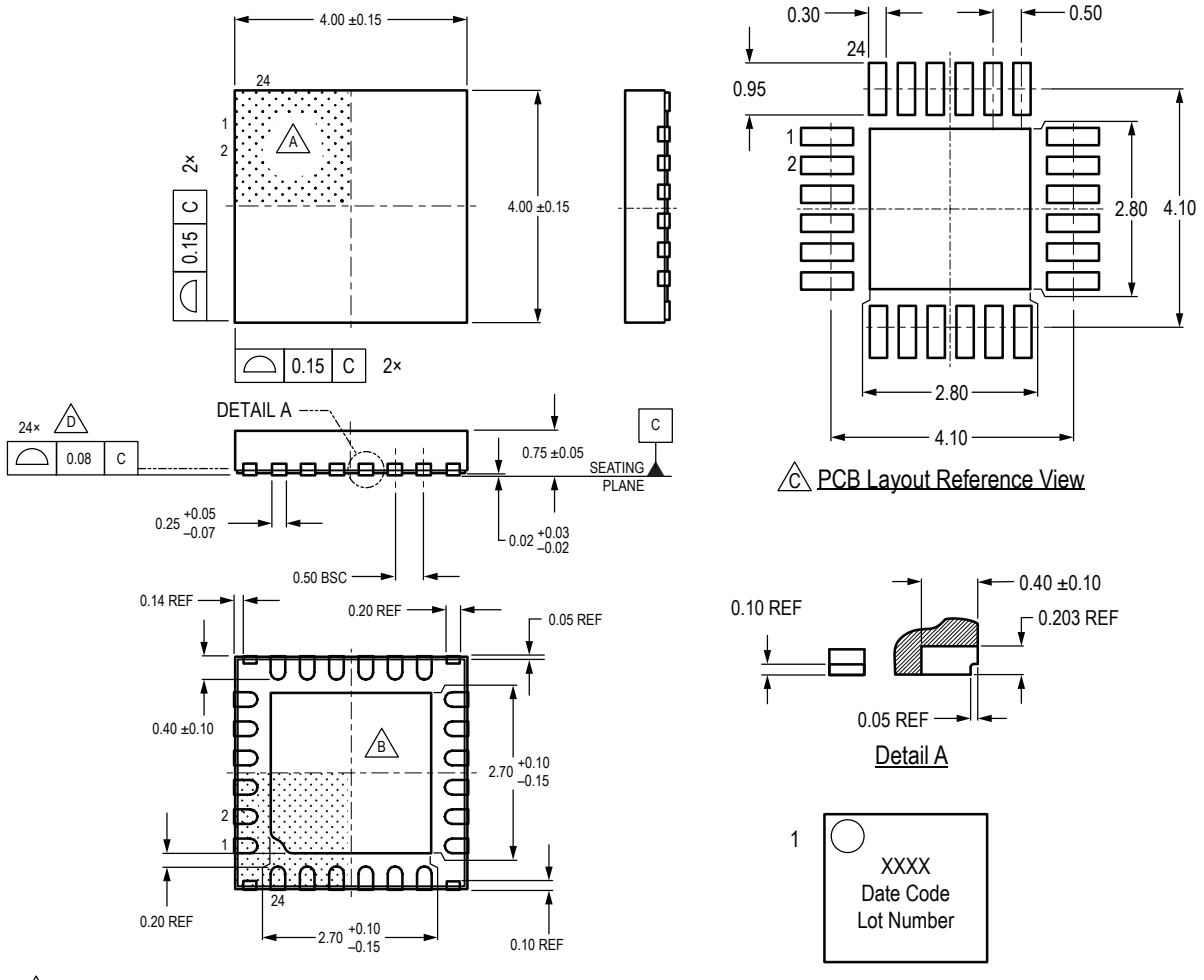
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 6 or JEDEC MO-220WGGD)
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Line 1: Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 47: Package ES, 24-Pin 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank

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APPENDIX A: DESIGN EXAMPLE

This section provides step-by-step instructions to select component values for an A80601 application.

For the purposes of this example, the following operating conditions are assumed:

- V_{IN} = 12 V nominal (6 V min, 18 V max)
- Number of LED channels nc = 4
- Number of series LEDs per channel n = 7
- LED current per channel I_{LED} = 150 mA
- LED forward drop V_f = 3.2 V max at cold
- Switching frequency f_{SW} = 2.15 MHz
- Dithering modulation frequency f_{DITH} = 1 kHz
- Dithering frequency range Δf_{SW} = ±5%
- Max ambient temperature $T_{A(max)}$ = 65°C
- PWM dimming frequency f_{PWM} = 200 Hz

Step 1: Program the Switching Frequency from Equation 1:

$$R_{FSET} = (21.5 / f_{SW}) - 0.2$$

where f_{SW} is in MHz and R_{FSET} is in kΩ.

Substitute f_{SW} = 2.15 MHz to get R_{FSET} = 9.8 kΩ (pick 10 kΩ).

Step 1a: Program the Dithering Modulation Frequency from Equation 2:

$$C_{DITH}\,(nF) = 25 / f_{DM}\,(kHz)$$

Substitute f_{DM} = 1 kHz to get C_{DITH} = 25 nF (pick 22 nF).

Step 1b: Select Dithering Range from Equation 3:

$$R_{DITH} = 20 \times R_{FSET} / Range\ (\pm\%)$$

Substitute Range = 5 and R_{FSET} = 10 kΩ to get R_{DITH} = 40 kΩ (pick 40.2 kΩ). The switching frequency now linearly sweeps between 2.04 and 2.26 MHz.

Step 2: Determine the LED current set Resistor R_{ISET} from Equation 4:

$$R_{ISET} = 1444 / I_{LED}$$

Substitute I_{LED} = 150 mA to get R_{ISET} = 9.63 kΩ (pick 9.53 kΩ).

Step 3: Determining the OVP resistor according to Equation 5:

$$R_{OVP} = (V_{OVP} - V_{OVP(th)}) / i_{OVP(th)}$$

The nominal output voltage is:

$$V_{OUT\_nom} = n \times V_f + V_{REG}$$

where V_{REG} is the LED pin regulation voltage. Substitute n = 7, V_f = 3.2 V, $V_{OVP(th)}$ = 2.5 V, and V_{REG} = 0.85 V to get V_{OUT_nom} = 23.25 V.

Set the OVP threshold voltage approximately 10% higher, to account for error margin and component tolerances:

$$V_{OVP} = V_{OUT\_nom} \times 1.1 = 25.6\ V$$

The OVP resistor is therefore:

$$R_{OVP} = (25.6\ V - 2.5\ V) / 150\ \mu A$$
$$= 154\ k\Omega\ (pick\ 154\ k\Omega)$$

Step 3a: Check to ensure the maximum boost duty cycle is sufficient to achieve the required conversion ratio.

$$D_{MAX(boost)} = 1 - t_{SW(off)} \times f_{SW(max)}$$

where $t_{SW(off)}$ is the worst-case minimum SW on-time, and $f_{SW(max)}$ is the maximum switching frequency with dithering.

Substitute $t_{SW(off)}$ = 100 ns and $f_{SW(max)}$ = 2.26 MHz to get $D_{MAX(boost)}$ = 0.774.

Theoretical maximum output voltage at the lowest input voltage is:

$$V_{OUT(max)} = V_{IN(min)} / (1 - D_{MAX(boost)}) - V_D$$

where V_D is the forward drop of boost Schottky diode.

Substitute $V_{IN(min)}$ = 6 V, $D_{MAX(boost)}$ = 0.774, and V_D = 0.4 V to get $V_{OUT(max)}$ = 26.15 V.

Theoretical $V_{OUT(max)}$ has to be greater than V_{OVP}. If this is not the case, then switching frequency of the boost converter must be reduced to meet the maximum duty cycle requirement.

Step 4 – Inductor selection: The inductor must be chosen based on ripple current requirement. In most applications due to stringent EMI requirements, the system also needs to operate in continuous conduction mode (CCM) throughout the whole input voltage range. A simple guideline is to start with 30% peak-to-peak ripple current at nominal input and output voltages.

Step 4a: Determine the Boost Duty Cycle:

$$D = 1 - V_{IN} / (V_{OUT} + V_D)$$

For nominal operation, substitute V_{IN_nom} = 12 V, V_{OUT_nom} = 23.25 V and V_D = 0.4 V to get D_{nom} = 0.493.

Step 4b: Calculate the nominal Input Current based on estimated efficiency:

$$i_{IN} = V_{OUT} \times i_{OUT} / (V_{IN} \times \eta)$$

where η = efficiency of the converter (typically in the 85% to 90% range).

For nominal operation, substitute V_{OUT} = 23.25 V, i_{OUT} = 0.6 A, V_{IN} = 12 V, and η = 0.9 to get i_{IN} = 1.29 A.

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Step 4c: Select Boost Inductance based on 30% Ripple Current.

For nominal operation, $\Delta i_L = 0.3 \times i_{IN} = 0.39$ A.

$$\Delta i_L = t_{ON} \times V_{IN} / L = D \times V_{IN} / (f_{SW} \times L)$$

Therefore:

$$L = D \times V_{IN} / (f_{SW} \times \Delta i_L)$$

Substitute $D_{nom} = 0.493$, $V_{IN\_nom} = 12$ V, and $f_{SW} = 2.15$ MHz to get L = 7.1 µH (pick 6.8 µH).

STEP 4d: Determine the maximum and minimum input current to the system. The maximum current determines the inductor's saturation current rating. The minimum current determines its critical inductance.

Maximum input current occurs at minimum V_{IN} and maximum V_{OUT} (OVP).

$$i_{IN\_max} = V_{OVP} \times i_{OUT} / (V_{IN\_min} \times \eta)$$

Substitute $V_{OVP} = 25.6$ V, $V_{IN\_min} = 6$ V, and $\eta = 0.85$ to get $i_{IN\_max} = 3.01$ A.

Peak inductor current:

$$i_{L\_peak} = i_{IN\_max} + \Delta i_L / 2$$

At minimum $V_{IN} = 6$ V, D = 0.769, $\Delta i_L = 0.316$ A, and so $i_{L\_peak} = 3.01 + 0.316 / 2 = 3.17$ A. Therefore, the inductor should have a saturation current of at least 3.8 A (20% higher than i_{L_peak}).

Minimum input current occurs at maximum V_{IN} and nominal V_{OUT}.

$$i_{IN\_min} = V_{OUT\_nom} \times i_{OUT} / (V_{IN\_max} \times \eta)$$

Substitute $V_{OUT\_nom} = 23.25$ V, $V_{IN\_max} = 18$ V, and $\eta = 0.9$ to get $i_{IN\_min} = 0.865$ A.

At maximum $V_{IN} = 18$ V, D = 0.239, $\Delta i_L = 0.294$ A, and so $i_{L\_valley} = 0.865 - 0.294 / 2 = 0.718$ A. Therefore, the converter operates in CCM throughout the input voltage range.

Step 5: Verify that there is sufficient slope compensation for the inductor chosen. The A80601 generates a variable internal Slope Comp according to f_{SW} and V_{IN}.

- If V_{IN} is between 9 V and 15 V:
  $SC = 3 \times f_{SW} \times V_{IN} / 12$
- If $V_{IN} < 9$ V:
  $SC = 3 \times f_{SW} \times 9 / 12$
- If $V_{IN} > 15$ V:
  $SC = 3 \times f_{SW} \times 15 / 12$

where f_{SW} is in MHz and SC is in A/µs.

For example, at $f_{SW} = 2.15$ MHz and $V_{IN} = 6$ V, SC = 4.84 A/µs

The falling slope of inductor current is given as:

$$di_L/dt = -\Delta i_L / t_{OFF} = -\Delta i_L \times f_{SW} / (1 - D)$$

Based on equations from previous section, at $V_{IN} = 6$ V and $V_{OUT(OVP)} = 25.6$ V, D = 0.769 and $\Delta i_L = 0.316$ A. Therefore $|di_L/dt| = 2.94$ A/µs, which is slower than the internal slope. That means there is sufficient slope compensation.

In case the negative slope of inductor current is faster than the internal slope comp, a higher inductance value must be used.

Step 6: Select External Boost Switch MOSFET.

Refer to Appendix B for more details on how to select the external boost MOSFET. For this example, the MOSFET picked is SVD5867NL with the following key parameters:

- Breakdown voltage $V_{(BD)DSS} = 60$ V min
- On-resistance $R_{DS(on)} = 50$ mΩ max at $V_{GS} = 4.5$ V
- Total Gate Charge $Q_G = 10$ nC for $V_{GS} = 0$ to 6.5 V

Step 7: Select boost switch current sense resistor from Equation 5:

$$R_{CS} = V_{CS(LIM1)} / i_{CS(LIM1)}$$

From previous section, $i_{L\_peak} = 3.17$ A at min V_{IN} and max V_{OUT}. Set the cycle-by-cycle SW current limit at least 20% higher, which means ~3.8 A. Therefore:

$$R_{CS} = 210\ mV / 3.8\ A = 55\ m\Omega$$

Pick a standard resistor value of 47 mΩ. This gives cycle-by-cycle current limit of $i_{CS(LIM1)} = 4.5$ A.

Step 8: Choose the input disconnect switch components.

Set the input disconnect switch current limit at least 20% above the SW cycle-by-cycle current limit:

$$i_{SENSE} = 4.5\ A \times 1.2 = 5.4\ A$$

$$R_{SC} = V_{SENSETRIP} / i_{SENSE} = 18.1\ m\Omega$$

where $V_{SENSETRIP} = 98$ mV.

Pick the closest lower resistance value, which is 18 mΩ.

$$R_{ADJ} = [V_{SENSETRIP} - (R_{SC} \times i_{SENSE})] / i_{ADJ} = 40\ \Omega$$

where $i_{ADJ} = 20$ µA.

Select the input disconnect switch P-MOSFET based on its drain-source breakdown voltage and on-resistance.

The SQJ459EP can be used in this case. It has $V_{DS} = -60$ V and $R_{DS(ON)} = 24$ mΩ at $V_{GS} = -4.5$ V.

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Step 9: Select the switching diode.

A Schottky barrier diode (SBD) is typically selected based on its voltage and current ratings:

- The reverse voltage rating must be higher than the maximum voltage stress, which is equal to the OVP threshold in this case.
- The average forward current rating must be higher than the total LED current. The peak current rating of the diode must exceed the secondary current limit, $I_{CS(LIM2)}$, which is $1.4 \times I_{CS(LIM1)}$.

Another critical parameter is the diode's reverse leakage current at hot. This is especially important when using PWM dimming. During PWM off time, the boost converter is not switching, so voltage at output capacitor decays due to leakage current. This increases output ripple voltage, which may generate audible noise from ceramic capacitors.

Make sure to verify the diode's reverse current at hot (such as 125°C) and at the nominal V_{OUT}. As a general guideline, look for a diode with leakage of 100 µA or less. If necessary, consider using a diode with higher voltage rating (such as 100 V instead of 50 V). Doing so can significantly reduce the leakage current at nominal V_{OUT}.

For this design example, a 100 V, 3 A Schottky diode SS3H10 is selected. It has a very low i_R = 50 µA at T_J = 125°C and V_R = 30 V.

Step 10: Selection of output capacitors.

The use of multilayer ceramic capacitor (MLCC) is recommended. MLCC has extremely low ESR, which is necessary to reduce output switching ripple for boost converter. In addition, the total output capacitance needs to be sufficient to reduce output droop during PWM dimming operation.

The biggest contributing factors for total output capacitance are PWM off-time and leakage current (i_{LK}). This current is mainly due to the reverse current of switching diode, plus a small/negligible leakage current into the OVP pin.

In this design example, the PWM dimming frequency is 200 Hz with minimum duty cycle of 0.01%. So the maximum PWM off-time is essentially t_{OFF} = 5 ms. A typical goal is to keep the output voltage variation at 250 mV or less to avoid audible noise.

$$\Delta V_{OUT} = t_{OFF} \times i_{LK} / C_{OUT}$$

Therefore:

$$C_{OUT} = t_{OFF} \times i_{LK} / \Delta V_{OUT}$$

Substitute t_{OFF} = 5 ms, i_{LK} = 110 µA, and ΔV_{OUT} = 0.25 V to get C_{OUT} = 2.2 µF.

A major problem with multilayer ceramic capacitor (MLCC) is that its actual capacitance drops with respect to DC bias. For example, the capacitance of a 4.7 µF, 50 V, 0805 MLCC may be derated by 80% when it is biased at 25 V. That means its real capacity is less than 1 µF in actual application.

An MLCC of larger physical size and higher voltage rating typically suffers less derating problem. For example, a 4.7 µF, 50 V, 1210 MLCC may retain 3.3 µF of capacitance at 25 V. This is shown in the table below:

Part Number	Package	Rated Capacitance at 0 V (µF)	Derating at 25 V	Actual Capacitance at 25 V (µF)
GRM21BC71H475KE11	0805	4.7	–80%	0.94
GRM31CR71H475MA12	1206	4.7	–45%	2.59
GRM32ER71H475KA88	1210	4.7	–30%	3.29

Step 11: Selection of input capacitor.

A combination of MLCC and electrolytic capacitor is recommended. The MLCC provides low ESR to reduce input switching ripple. The electrolytic capacitor provides larger capacitance to stabilize input voltage during PWM dimming operation.

A good rule of thumb is to set the input voltage ripple ΔV_{IN} to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows.

$$C_{IN} = \Delta i_L / (8 \times f_{SW} \times \Delta V_{IN})$$

Substitute Δi_L = 0.316 A at V_{IN} = 6 V (from step 4d), ΔV_{IN} = 0.06 V, and f_{SW} = 2.15 MHz to get C_{IN} = 0.306 µF. Due to the DC bias derating, the actual MLCC selected should be rated 1 µF or higher. For this design, a 2.2 µF capacitor is used.

A much larger input capacitance is required to provide the inrush current during PWM dimming operation. The exact requirement depends on many external factors, such as length of power cables and response time of the power supply. As a first-order estimate: assume the power supply takes 25 µs to response, and the input capacitor must keep the V_{IN} dip under 0.2 V while input current ramps up from zero to full load. The following is needed:

$$C_{IN} = i_{IN} \times t_{PS} / (8 \times \Delta V_{IN})$$

Substitute i_{IN} = 3.01 A at V_{IN} = 6 V (from step 4d), ΔV_{IN} = 0.2 V and t_{PS} = 25 µs to get C_{IN} = 47 µF. Use an electrolytic capacitor of 47 µF in parallel with the MLCC.

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Step 12: Selection of Compensation Components.

For most applications, the compensation network shown in Figure 48 is sufficient for stable circuit performance.

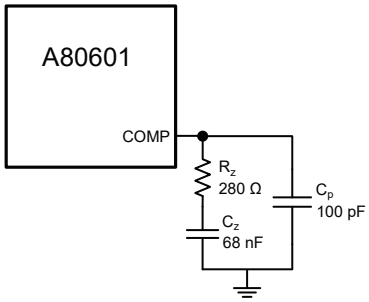

Figure 48: Compensation Network Schematic

This application will use the following compensation values: R_z = 280 Ω, C_z = 68 nF, C_p = 100 pF.

For applications where a higher voltage control loop crossover frequency is desired, R_z can be increased. To increase phase margin at the crossover frequency, C_z can be increased, but exceeding 470 nF is not recommended. Control loop stability should be evaluated in any application to ensure proper performance.

The following schematic diagram shows calculated component values from the design example. The other components that are not discussed in this design example are recommended for proper circuit performance.

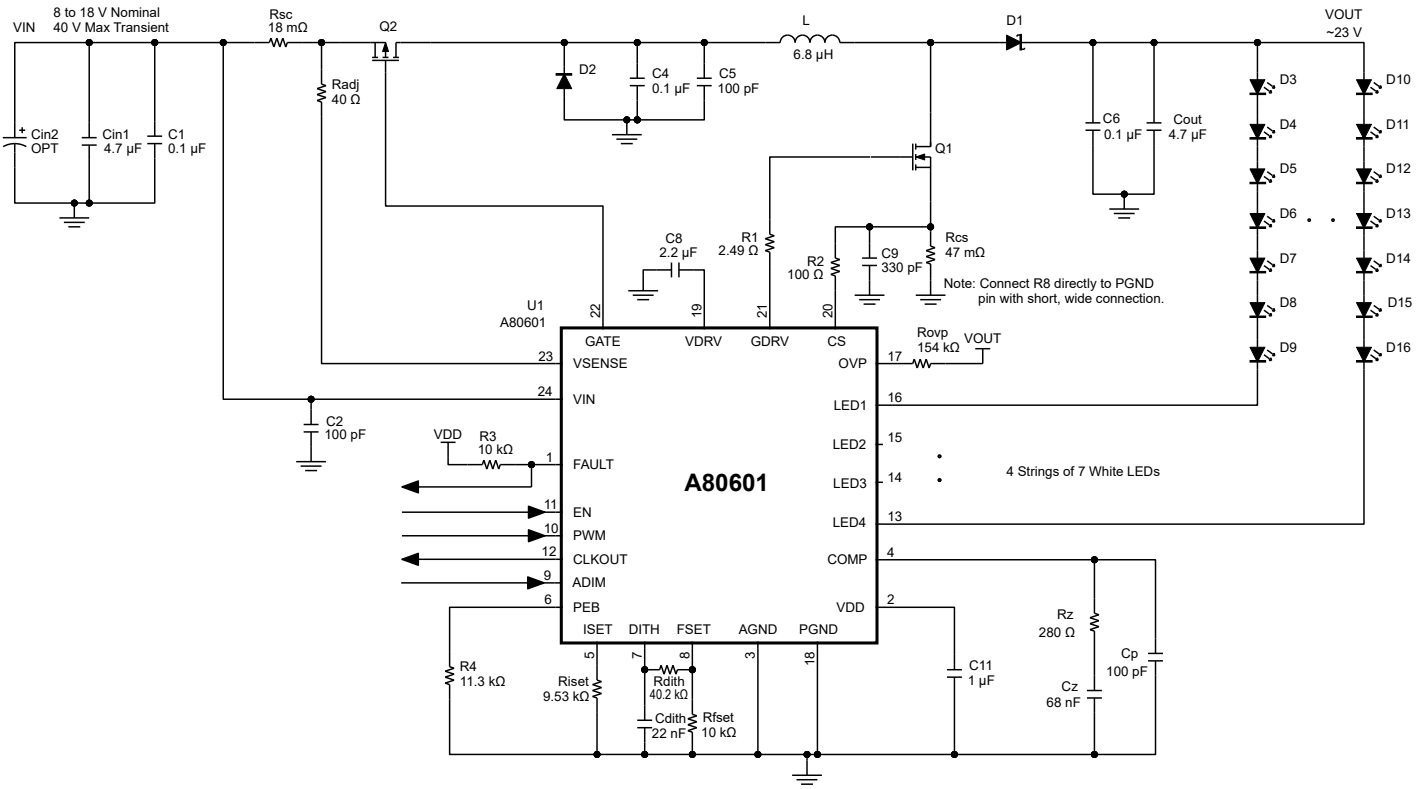

Figure 49: Boost Design Example Schematic

V_{IN} = 8 to 18 V (nominal), 18 to 40 V (transient)
V_{OUT} = 23 V, I_{LED} = 150 mA per string, 4 strings

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Table 7: Boost Design Example Bill of Materials

Designator	Quantity	Value	Description	Footprint	Comment
Cin1, Cout	2	4.7 µF	CAP CER, 50 V, X7R	1210	
Cin2	1	47 µF	POLARIZED CAP (RADIAL)	Cap Radial 8 mm surface mount	Panasonic EEE-TG1H470UP
C1, C4, C6	3	0.1 µF	CAP CER, 50 V, X7R	0603	
C2, C5, Cp	3	100 pF	CAP CER, 50V, COG/NPO	0603	
C8	1	2.2 µF	CAP CER, 16 V, X7R	0805	
C9	1	330 pF	CAP CER, 25 V, COG/NPO	0603	
C11	1	1 µF	CAP CER, 16 V, X7R	0603	
Cdith	1	22 nF	CAP CER, 25 V, X7R	0603	
Cz	1	68 nF	CAP CER, 10 V, X7R	0603	
D1	1		DIODE SCHOTTKY, 100 V, 3 A	DO-214AB	Vishay SS3H10-E3/9AT
D2	1		DIODE GENERAL PURPOSE, 100 V, 300 mA	SOD123	Diodes Incorporated 1N4148W-7
D3-D31	28		LED, WHITE, 3.2 V FORWARD VOLTAGE DROP		Total of 28 for 4 strings of 7 LEDs
L	1	6.8 µH	Inductor, 6 A, 27 mΩ		Coilcraft XEL5050-682
Q1	1		MOSFET N-CHANNEL, 60 V, 18 A	DPAK	ON Semiconductor SVD5867NLT4G
Q2	1		MOSFET P-CHANNEL, 60 V, 52 A	PowerPAK SO-8L	Vishay Siliconix SQJ459EP-T1_GE3
R1	1	2.49 Ω	RES, 1%	0603	
R2	1	100 Ω	RES, 1%	0603	
R3, Rfset	2	10 kΩ	RES, 1%	0603	
R4	1	11.3 kΩ	RES, 1%	0603	
Radj	1	40 Ω	RES, 1%	0603	
Rcs	1	47 mΩ	RES, 1%	1210	
Rdith	1	40.2 kΩ	RES, 1%	0603	
Riset	1	9.53 kΩ	RES, 1%	0603	
Rovp	1	154 kΩ	RES, 1%	0603	
Rsc	1	18 mΩ	RES, 1%	1206	
Rz	1	280 Ω	RES, 1%	0603	
U1	1		Allegro MicroSystems A80601	ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank	High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

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APPENDIX B: REFERENCE DESIGNS

SEPIC Configuration

A SEPIC architecture can be employed to allow the converter to regulate with the input voltage below, equal to or above the output voltage. While a coupled inductor is not necessary for this design to function, a coupled inductor will generally reduce the overall solution size and component count and may reduce the solution cost.

Figure 50 shows the A80601 in a SEPIC configuration driving four strings of four white LEDs. Each string has a forward voltage drop of about 14 V, and the current in each string is regulated to 200 mA. The SEPIC converter switching frequency is set to 400 kHz. This design can be employed as-is or can be modified to accommodate different circuit requirements as needed.

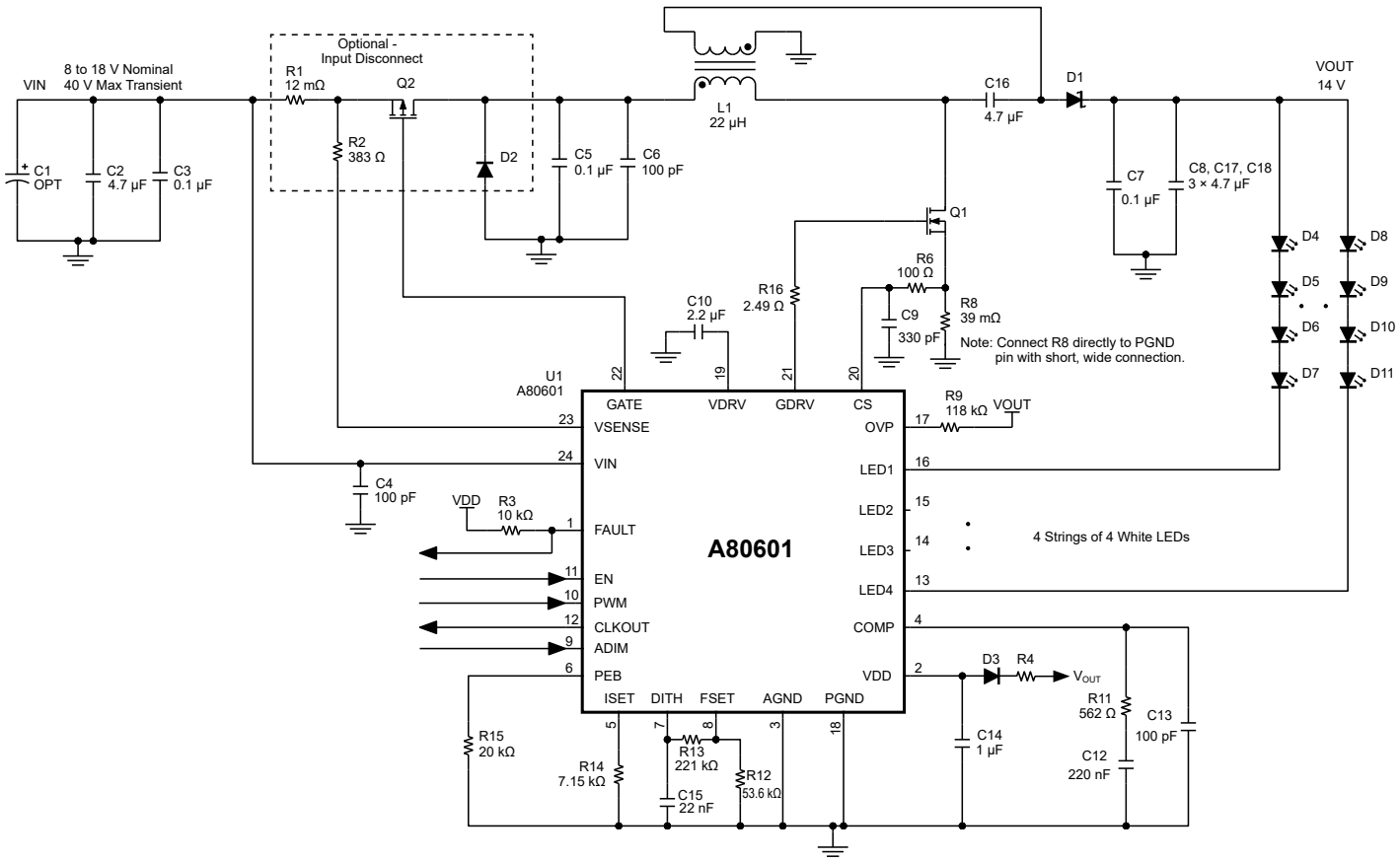

Figure 50: SEPIC configuration. Allows operation with V_{IN} both above and below V_{OUT}.

V_{IN} = 8 to 18 V (nominal), 4.5 to 8 V / 18 to 40 V (transient)
V_{OUT} = 14 V, I_{LED} = 200 mA per string, 4 strings

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Table 8: SEPIC Configuration Bill of Materials

Designator	Quantity	Value	Description	Footprint	Comment
C1	0 (OPT)	47 µF	POLARIZED CAP (RADIAL)	Cap Radial 8 mm surface mount	Panasonic EEE-TG1H470UP
C2, C8, C16, C17, C18	5	4.7 µF	CAP CER, 50 V, X7R	1210	
C3, C5, C7	3	0.1 µF	CAP CER, 50 V, X7R	0603	
C4, C6, C13	3	100 pF	CAP CER, 50 V, COG/NPO	0603	
C9	1	330 pF	CAP CER, 25 V, COG/NPO	0603	
C10	1	2.2 µF	CAP CER, 16 V, X7R	0805	
C12	1	220 nF	CAP CER, 10 V, X7R	0603	
C14	1	1 µF	CAP CER, 16 V, X7R	0603	
C15	1	22 nF	CAP CER, 25 V, X7R	0603	
D1	1		DIODE SCHOTTKY, 100 V, 3 A	DO-214AB	Vishay SS3H10-E3/9AT
D2, D3	2		DIODE GENERAL PURPOSE, 100 V, 300 mA	SOD123	Diodes Incorporated 1N4148W-7
D4, D5, D6, D7, D8, D9, D10, D11	16		LED, WHITE, 3.5 V FORWARD VOLTAGE DROP		Total of 16 for 4 strings of 4 LEDs
L1	1	22 µH	COUPLED INDUCTOR FOR SEPIC CONVERTER APPLICATIONS	Coupled-Inductor 2	Wurth 7448990220
Q1	1		MOSFET N-CHANNEL, 60 V, 18 A	DPAK	ON Semiconductor SVD5867NLT4G
Q2	1		MOSFET P-CHANNEL, 60 V, 52 A	PowerPAK SO-8L	Vishay Siliconix SQJ459EP-T1_GE3
R1	1	12 mΩ	RES, 1%	1206	
R2	1	383 Ω	RES, 1%	0603	
R3	1	10 kΩ	RES, 1%	0603	
R4	1	1 kΩ	RES, 1%	0603	
R6	1	100 Ω	RES, 1%	0603	
R8	1	39 mΩ	RES, 1%	1210	
R9	1	118 kΩ	RES, 1%	0603	
R11	1	562 Ω	RES, 1%	0603	
R12	1	53.6 kΩ	RES, 1%	0603	
R13	1	221 kΩ	RES, 1%	0603	
R14	1	7.15 kΩ	RES, 1%	0603	
R15	1	20 kΩ	RES, 1%	0603	
R16	1	2.49 Ω	RES, 1%	0603	
U1	1		Allegro MicroSystems A80601	ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank	High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

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Cascode-Protected LED Pins Design

The A80601's LEDx pins have an absolute maximum voltage rating of 40 V. For applications where V_{OUT} exceeds 40 V, it is important to protect the LEDx pins in the event that part or all of an LED string is shorted. Figure 51 shows a circuit that protects the LEDx pins by using cascode transistors to disconnect LEDx from VOUT in this event. A voltage rail, V_{GCAS}, must be provided externally or generated from an available voltage such as V_{OUT}. One simple way to derive V_{GCAS} from V_{OUT} is by use of a resistor and Zener diode as shown in Figure 51.

For proper LEDx pin protection, V_{GCAS} must be sufficiently large to ensure that upon an LED short event, the corresponding LEDx pin exceeds its LED String Partial-Short Detect Threshold, V_{LEDSD}. Also, V_{GCAS} must not exceed the maximum gate-to-source rating of the transistor. Minimum V_{GCAS} can be calculated as follows:

$$V_{GCAS(min)} = V_{GP} + V_{LEDSD(max)}$$

where

$V_{GCAS(min)}$ is the minimum suitable gate voltage,

V_{GP} is the cascode transistor's plateau voltage (see gate threshold voltage versus total gate charge curve in the transistor's datasheet), and

$V_{LEDSD(max)}$ is the maximum LED String Partial-Short Detect threshold ($V_{LEDSD(max)}$ = 6.1 V).

Figure 51 shows the A80601 driving four strings of 12 white LEDs. Each string has a forward voltage drop of about 42 V, and the current in each string is regulated to 150 mA. Each LED string has a cascode transistor that will protect the respective LEDx pin from overvoltage in the event of an LED string short. Output overvoltage protection of the boost converter is set to 45.5 V, and the switching frequency is 2 MHz.

The cascode transistors can be any small-signal N-channel MOSFETs rated for the maximum output voltage and LED current per channel. As an example: consider T2N7002BK in SOT23 package. This device has a 60 V breakdown rating and 400 mA continuous current rating.

This design can be employed as-is or can be modified to accommodate different circuit requirements as needed. Note that the maximum number of LEDs is limited by the minimum input voltage and the minimum boost power switch gate driver off-time ($t_{SW(OFF)}$). Reducing the switching frequency of the converter will allow operation with a lower input voltage for a given number of LEDs.

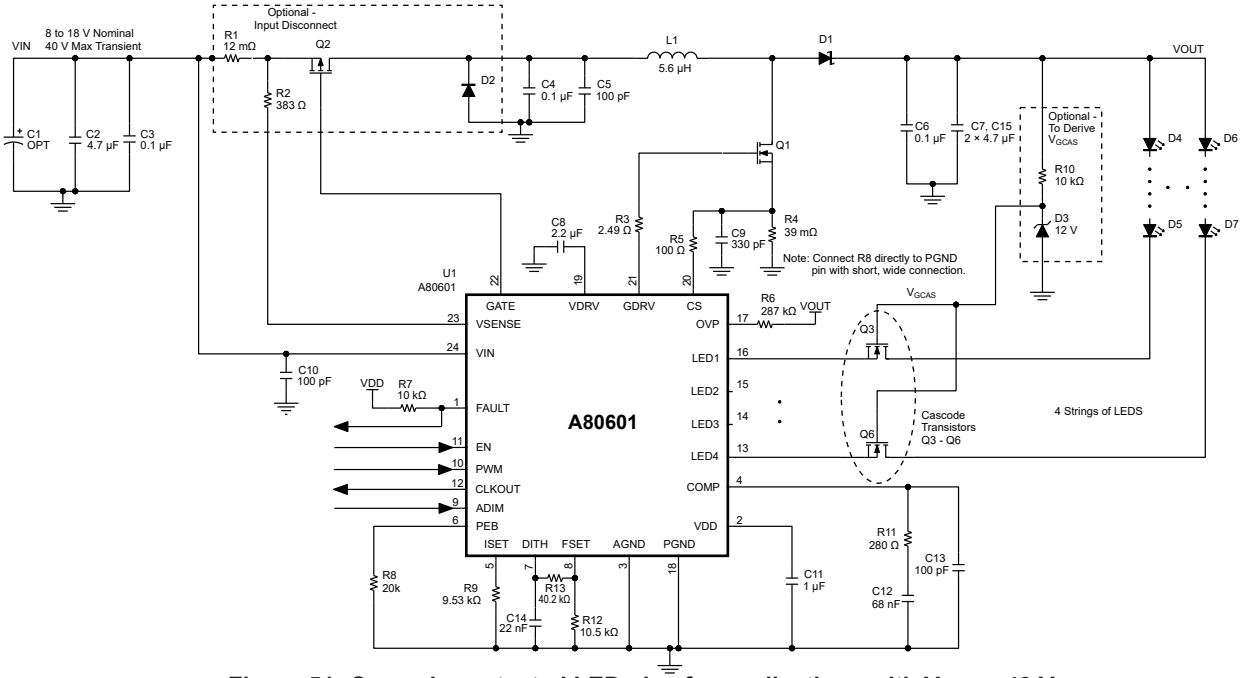

Figure 51: Cascode-protected LED pins for applications with V_{OUT} > 40 V.

V_{IN} = 8 to 18 V (nominal), 18 to 40 V (transient)
V_{OUT} = 42 V, I_{LED} = 150 mA per string, 4 strings

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Table 9: Cascode-Protected LED Pins Design Bill of Materials

Designator	Quantity	Value	Description	Footprint	Comment
C1	0 (OPT)	47 µF	POLARIZED CAP (RADIAL)	Cap Radial 8 mm surface mount	Panasonic EEE-TG1H470UP
C2, C7, C15	3	4.7 µF	CAP CER, 50 V, X7R	1210	
C3, C4, C6	3	0.1 µF	CAP CER, 50 V, X7R	0603	
C5, C10, C13	3	100 pF	CAP CER, 50 V, COG/NPO	0603	
C8	1	2.2 µF	CAP CER, 16 V, X7R	0805	
C9	1	330 pF	CAP CER, 25 V, COG/NPO	0603	
C11	1	1 µF	CAP CER, 16 V, X7R	0603	
C12	1	68 nF	CAP CER, 10 V, X7R	0603	
C14	1	22 nF	CAP CER, 25 V, X7R	0603	
D1	1		DIODE SCHOTTKY, 100 V, 3 A	DO-214AB	Vishay SS3H10-E3/9AT
D2	1		DIODE GENERAL PURPOSE, 100 V, 300 mA	SOD123	Diodes Incorporated 1N4148W-7
D3	1		DIODE ZENER, 12 V, 300 MW	SOD323	ON Semiconductor SZMM3Z12VT1G
D4, D5, D6, D7 ...	48		LED, WHITE, 3.5 V FORWARD VOLTAGE DROP		Total of 48 for 4 strings of 12 LEDs
L1	1	5.6 µH	INDUCTOR, 5.5 A, 23 mΩ		Coilcraft XEL5050-562ME
Q1	1		MOSFET N-CHANNEL, 60 V, 18 A	DPAK	ON Semiconductor SVD5867NLT4G
Q2	1		MOSFET P-CHANNEL, 60 V, 52 A	PowerPAK SO-8L	Vishay Siliconix SQJ459EP-T1_GE3
Q3 - Q6	4		MOSFET N-CHANNEL, 60 V, 400 mA	SOT23	Toshiba T2N7002BK.LM
R1	1	12 mΩ	RES, 1%	1206	
R2	1	383 Ω	RES, 1%	0603	
R3	1	2.49 Ω	RES, 1%	0603	
R4	1	39 mΩ	RES, 1%	1210	
R5	1	100 Ω	RES, 1%	0603	
R6	1	287 kΩ	RES, 1%	0603	
R7, R10	2	10 kΩ	RES, 1%	0603	
R8	1	20 kΩ	RES, 1%	0603	
R9	1	9.53 kΩ	RES, 1%	0603	
R11	1	280 Ω	RES, 1%	0603	
R12	1	10.5 kΩ	RES, 1%	0603	
R13	1	40.2 kΩ	RES, 1%	0603	
U1	1		Allegro MicroSystems A80601	ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank	High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

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Master/Slave Design

For applications where more than four strings of LEDs are desired, two A80601-1s can be configured in a master/slave configuration, as in Figure 52. Master/slave operation requires the asymmetrical COMP and bidirectional Fault pin, which are only available with the A80601-1 (not A80601). This application allows up to four strings of LEDs at 100 mA per string, and the boost converter switching frequency is set to 400 kHz. This circuit can be used as-is or modified to meet application specific requirements.

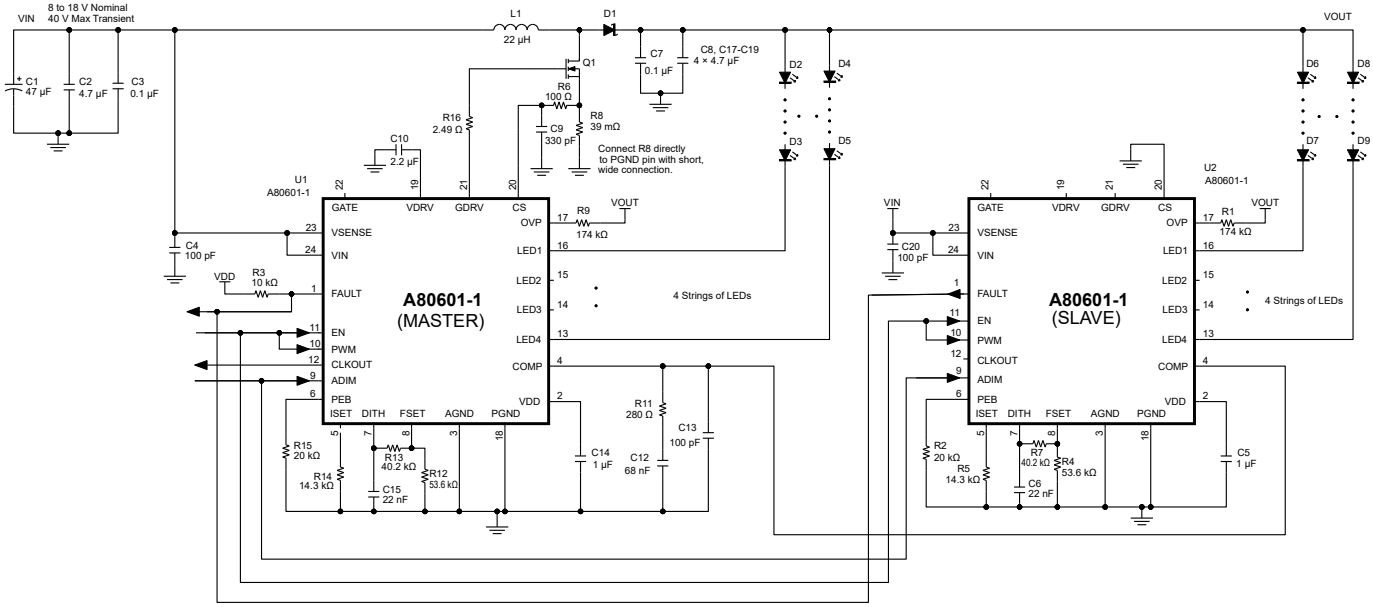

Figure 52: Two A80601-1s connected in master-slave configuration to drive 8 strings of LEDs.

V_{IN} = 8 to 18 V (nominal), 18 to 40 V (transient)
V_{OUT} = 25 V, I_{LED} = 100 mA per string, 8 strings

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Table 10: Master-Slave Design Bill of Materials

Designator	Quantity	Value	Description	Footprint	Comment
C1	1	47 µF	POLARIZED CAP (RADIAL)	Cap Radial 8mm surface mount	Panasonic EEE-TG1H470UP
C2, C8, C17-C19	5	4.7 µF	CAP CER, 50 V, X7R	1210	
C3, C7	2	0.1 µF	CAP CER, 50 V, X7R	0603	
C4, C13, C20	3	100 pF	CAP CER, 50 V, COG/NPO	0603	
C5, C14	2	1 µF	CAP CER, 16 V, X7R	0603	
C6, C15	2	22 nF	CAP CER, 25 V, X7R	0603	
C9	1	330 pF	CAP CER, 25 V, COG/NPO	0603	
C10	1	2.2 µF	CAP CER, 16 V, X7R	0805	
C12	1	68 nF	CAP CER, 10 V, X7R	0603	
D1	1		DIODE SCHOTTKY, 100 V, 3 A	DO-214AB	Vishay SS3H10-E3/9AT
D1, D2, D3, D4, D5, D6, D7, D8, D9	80		LED, WHITE, 3.5 V FORWARD VOLTAGE DROP		Total of 80 for 8 strings of 10 LEDs
Q1	1		MOSFET N-CHANNEL, 60 V, 18 A	DPAK	ON Semiconductor SVD5867NLT4G
L1	1	22 µH	INDUCTOR, 9 A, 37 mΩ		Bourns Inc. SRP1265A-220M
R1, R9	2	174 kΩ		0603	
R2, R15	2	20 kΩ		0603	
R3	1	10 kΩ		0603	
R4, R12	2	53.6 kΩ		0603	
R5, R14	2	14.3 kΩ		0603	
R6	1	100 Ω		0603	
R7, R13	2	40.2 kΩ		0603	
R8	1	39 mΩ		1210	
R11	1	280 Ω		0603	
R16	1	2.49 Ω		0603	
U1, U2	2		Allegro MicroSystems A80601-1	ES, 24-Pin, 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank	High Power LED Driver with Pre-Emptive Boost for Ultra-High Dimming Ratio and Low Output Ripple

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APPENDIX C: EXTERNAL MOSFET SELECTION GUIDE

The A80601 drives an external MOSFET for the boost stage. This solution provides maximum flexibility in delivering a wide range of output voltage and current for different LED panels, compared to controllers with built-in boost switches. On the other hand, care must be taken in selection of external MOSFET, to ensure optimal tradeoff between component size, efficiency, and cost. Primary parameters to consider include the following.

BREAKDOWN VOLTAGE

Pick the device with "Drain to Source Breakdown Voltage" at least 20% higher than the maximum possible SW voltage.

- For boost configuration, $V_{SW} = V_{OUT} + V_F$; where V_F = boost diode forward drop.
  The A80601 has a maximum V_{OUT} of 40 V. Therefore, the MOSFET should be rated 50 V or higher.
- For SEPIC configuration, $V_{SW} = V_{IN} + V_{OUT} + V_F$.
  Note that V_{IN} can be as high as 40 V during load-dump conditions. The breakdown voltage needs to be increased accordingly.

GATE THRESHOLD VOLTAGE

The device must be fully enhanced by the time V_{GS} = 5 V. Note that this is not the same as "Gate to Source Threshold Voltage" in most MOSFET datasheets, which is typically specified at very small current such as 250 µA. A more reliable way is to consult the "Gate Charge Characteristics" chart of the device, and make sure that the 'plateau' occurs well before V_{GS} reaches 5 V. See example from datasheet of one potential candidate:

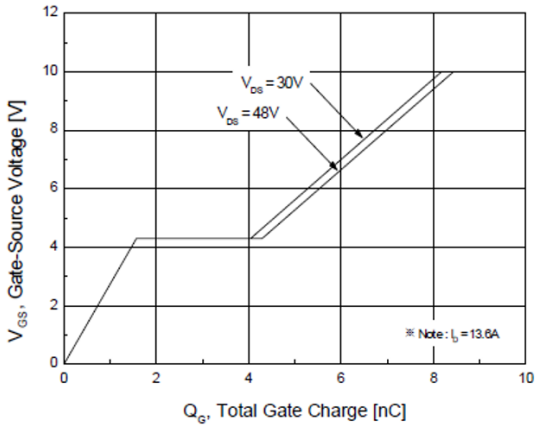

Figure 53: Gate Charge vs. Gate-Source Voltage for an example MOSFET. Note plateau at V_{GS} = 4.2 V approximately.

ON-RESISTANCE

A device with lower R_{DSON} will directly reduce the conduction loss of the boost converter. This is especially important when the output power is high and input supply voltage is low. Note that most datasheets typically highlight this parameter at V_{GS} = 10 V and T_J = 25°C. It is important to examine how R_{DSON} varies with gate voltage and temperature, as shown in the following charts:

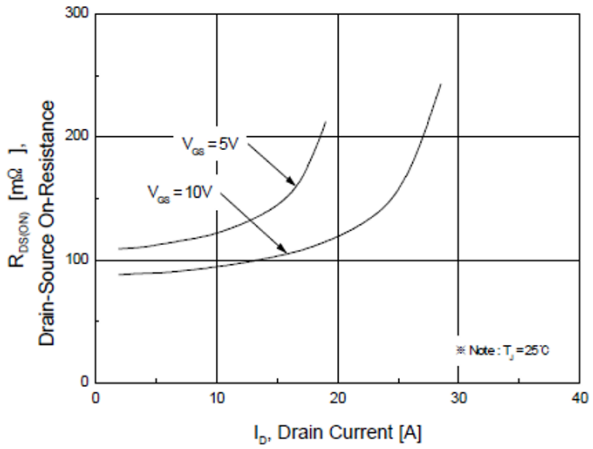

Figure 54: Chart showing On-Resistance varies with Drain Current and Gate Voltage.

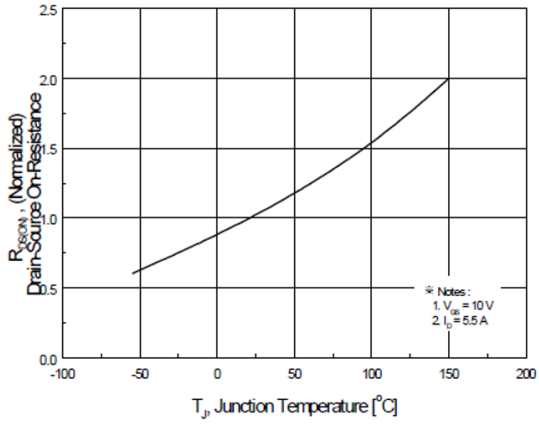

Figure 55: Nominalized On-Resistance vs. Junction Temperature at V_{GS} = 10 V. Note that resistance increases by 100% when temperature rises from 25°C to 150°C.

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THERMAL RATING

The thermal resistance ($R_{\theta JA}$) is primarily determined by the device's physical size. If the thermal resistance of the device is too high, or if there is insufficient heat dissipation on the PCB, the device may enter thermal run-away situation and burn itself out. For most medium-power (10-30 W) applications, a DPAK device is generally sufficient. For high-power (>50 W) applications, a D^2PAK device may be required. Depending on power loss, an additional heat sink can be mounted to improve the heat dissipation from the PCB.

GATE CHARGE

As mentioned earlier, lower R_{DSON} is desired to reduce conduction loss. But devices with lower R_{DSON} typically also have higher gate charge (Q_G), which can lead to higher switching loss. This is especially important when switching at high frequency (such as 2 MHz) and with high output voltage. Higher gate charge also results in higher gate driver current and hence higher power loss for the controller IC.

The A80601 uses an LDO to supply the driver voltage (V_{DRV}), which has a current limit of 25 mA minimum. Average gate driver current is:

$$i_{VDRV} = f_{SW} \times Q_G$$

If the MOSFET selected has Q_G = 27 nC, for example, then the highest switching frequency is limited to 925 kHz. See the following chart for relation between maximum switching frequency and MOSFET gate charge:

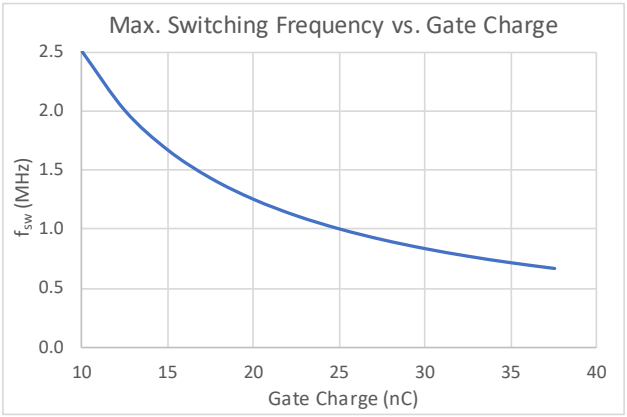

Figure 56: Maximum Switching Frequency vs. Gate Charge (to keep average V_{DRV} current under 25 mA).

On the other hand, selecting a device with very low Q_G may cause excessive voltage spikes at SW node due to high dV/dt. In this case, a snubber circuit can be added to dampen the ringing. The switching speed can be slowed down by adding a series gate resistance (such as 1-5 ohm) between the driver and the device. The downside of doing this is higher switching losses.

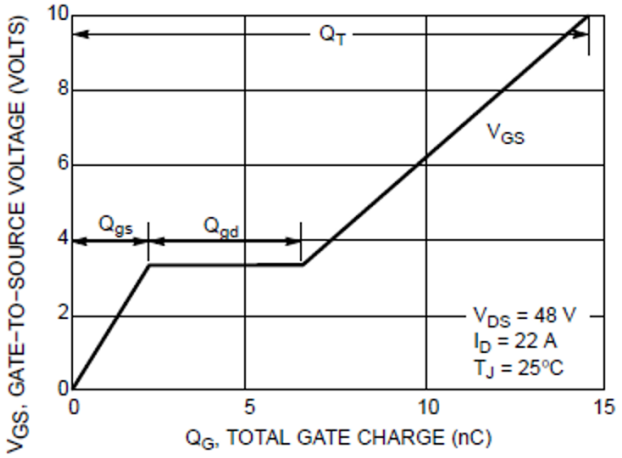

Figure 57: Gate Charge vs. Gate-Source Voltage chart for a suitable MOSFET (NVD5867NL). Note that its plateau is at ~3.5 V, and its total gate charge is about 10 nC as V_{GS} ramps up from 0 to 6.5 V.

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Revision History

Number	Date	Description
–	March 4, 2019	Initial release
1	March 6, 2020	Added design example appendix; minor editorial updates
2	March 18, 2021	Updated Features and Benefits, Description, simplified block diagram (page 1-2), Functional Block Diagram (page 4); updated APWM Duty Cycle Range (page 6); added Minimum PWM Off-Time characteristic (page 8); updated Functional Description (pages 9, 13, 15-17), Appendix A (pages 33-37); added Appendix B (pages 38-43); updated Appendix C (pages 44-45).
3	July 6, 2021	Updated Table of Contents (page 3); added Effects of Adding CS Pin RC Filter subsection (page 27)
4	April 26, 2022	Corrected SEPIC circuit, adding D3 and R4 from VDD to VOUT (pages 38-39)
5	April 28, 2023	Updated package drawing (page 32)

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