



**THE DATASHEET OF
NCV459MNWTBG**



NCV459

4 A Single Load Switch for Low Voltage Rail

The NCV459 is a power load switch with very low Ron NMOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a best in class current consumption optimization with NMOS structure, leakage currents are drastically decreased. Offering optimized leakages isolation on the ICs connected on the battery.

Output discharge path is proposed to eliminate residual voltages on the external components connected on output pin.

Proposed in wide input voltage range from 0.75 V to 5.5 V, and a very small DFNW8 3x3 mm, 0.65 pitch package.

Features

- 0.75 V – 5.5 V Operating Range
- 23 mΩ N–MOSFET
- Vbias Rail Input
- DC Current up to 4 A
- Output Auto–Discharge Option
- Active High EN Pin
- DFNW8, 3 x 3 mm, 0.65 pitch

Typical Applications

- ADAS System
- Camera Module
- Power Management



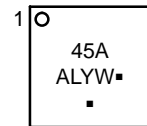
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM



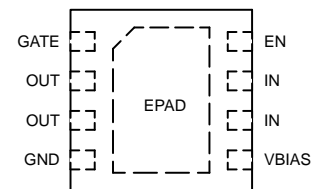
**DFNW8
CASE 507AB**



- 45A = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb–Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

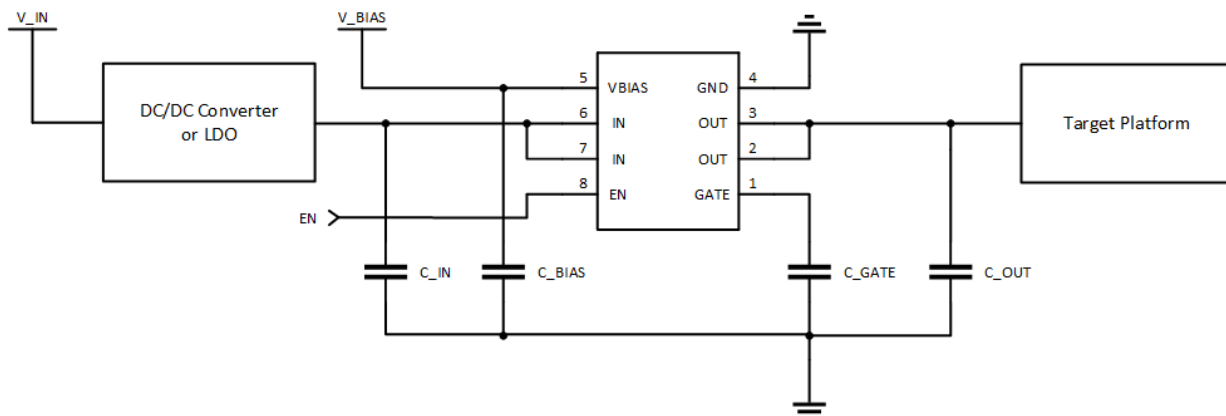


Figure 1. Typical Application Schematic

NCV459

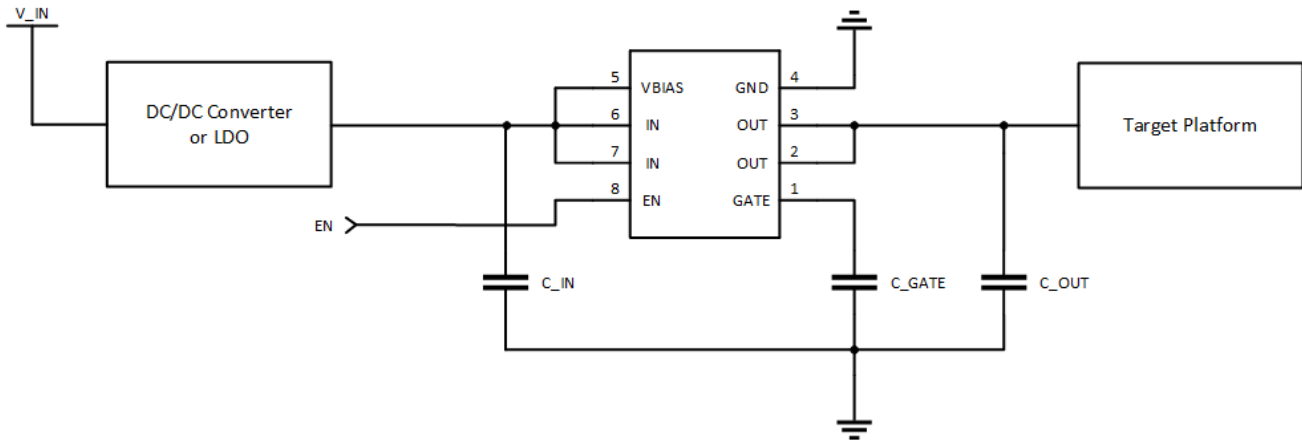


Figure 2. Application Schematic with Vbias Connected to IN

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
GATE	1	INPUT	OUT pin slew rate control (t_{rise}).
OUT	2, 3	POWER	Load-switch output pin.
GND	4	POWER	Ground connection.
VBIAS	5	POWER	External supply voltage input.
IN	6, 7	POWER	Load-switch input pin.
EN	8	INPUT	Enable input, logic high turns on power switch.
EPAD	9	POWER	Exposed pad, connect to ground potential.

NCV459

BLOCK DIAGRAMS

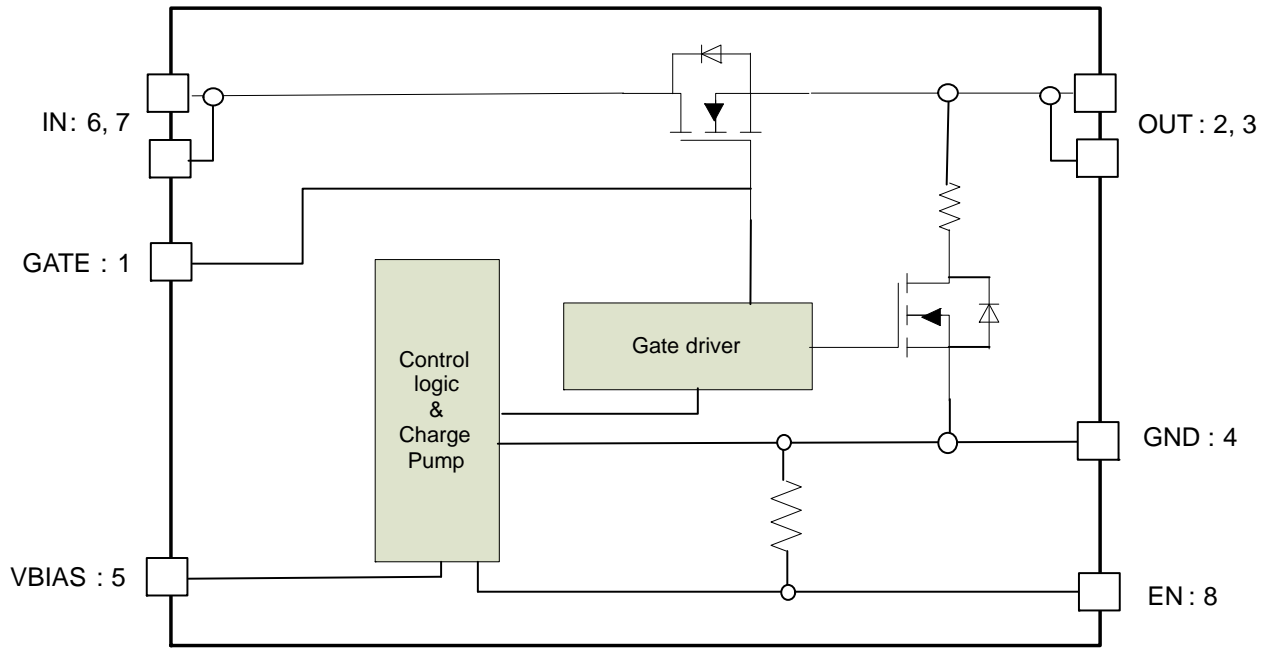


Figure 3. NCV459 Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, VBIAS, GATE Pins: (Note 1)	$V_{EN}, V_{IN}, V_{OUT}, V_{BIAS}, V_{GATE}$	-0.3 to +6.5	V
From IN to OUT Pins: Input/Output (Note 1)	V_{IN}, V_{OUT}	0 to + 6.5	V
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	2000	V
Maximum Junction Temperature	T_J	-40 to + 125	°C
Storage Temperature Range	T_{STG}	-40 to + 150	°C
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22-A108.
2. This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) ±2.0 kV per JEDEC standard:
JESD22-A114 for all pins.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply		0.75		5.5	V
V_{EN}	Enable Voltage		0		5.5	V
V_{BIAS}	Bias voltage ($V_{BIAS} \geq$ best of V_{IN}, V_{OUT})		1.2		5.5	V
T_A	Ambient Temperature Range		-40	25	+105	°C
C_{IN}	Decoupling input capacitor		100			nF
C_{OUT}	Decoupling output capacitor		100			nF
$R_{\theta JA}$	Thermal Resistance Junction to Air	DFNW8 (Note 4)		106		°C/W
I_{OUT}	DC current			4	4.5	A
	AC current 1 ms @ 217 Hz				5	A
	AC current 100 μs spike				15	A
P_D	Power Dissipation Rating (Note 5)			0.18		W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Value based on 1s0p board with copper 650 mm² (or 1 in²) of 1 oz thickness and FR4 PCB substrate
5. The maximum power dissipation (PD) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

NCV459

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J between -40°C to $+125^{\circ}\text{C}$ for V_{IN} between 0.75 V and 5.5 V, and V_{BIAS} between 1.2 V and 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
POWER SWITCH							
$R_{DS(on)}$	Static drain-source on-state resistance for each rail	$V_{IN} = V_{BIAS} = 5.5\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		23	60	m Ω
			$T_J = 125^{\circ}\text{C}$			80	
		$V_{IN} = V_{BIAS} = 3.3\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		23	60	
			$T_J = 125^{\circ}\text{C}$			80	
		$V_{IN} = V_{BIAS} = 1.8\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		23	60	
			$T_J = 125^{\circ}\text{C}$			80	
		$V_{IN} = V_{BIAS} = 1.5\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		23	60	
			$T_J = 125^{\circ}\text{C}$			80	
		$V_{IN} = V_{BIAS} = 1.2\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		24	60	
			$T_J = 125^{\circ}\text{C}$			80	
		$V_{IN} = 1.0\text{ V}$ $V_{BIAS} = 1.2\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		24	60	
			$T_J = 125^{\circ}\text{C}$			80	
		$V_{IN} = 0.8\text{ V}$ $V_{BIAS} = 1.2\text{ V}$	$I_{OUT} = 200\text{ mA}$, $T_A = 25^{\circ}\text{C}$		24	60	
			$T_J = 125^{\circ}\text{C}$			80	
R_{DIS}	Output discharge path	EN = low		230	300	Ω	

TIMINGS (Note 6)

T_R	Output rise time From 10% to 90% of V_{OUT}	$V_{IN} = 5\text{ V}$ $C_{LOAD} = 1\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$	No cap on GATE pin		0.26		ms	
			Gate capacitor = 1 nF		1.5			
			Gate capacitor = 10 nF		15			
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}		Without Cgate		10		μs	
			With 1 nF on Gate		60		μs	
T_F	Fall Time. From 90% to 10% of V_{OUT}				50		μs	
T_{dis}	Disable time				From EN to 90% Vout	75		μs
T_R	Output rise time From 10% to 90% of V_{OUT}		$V_{IN} = 3.3\text{ V}$ $C_{LOAD} = 1\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$	No cap on GATE pin		0.25	0.5	ms
				Gate capacitor = 1 nF		1		
				Gate capacitor = 10 nF		10		
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}			Without Cgate		20	50	μs
				With 1 nF on Gate		114		μs
T_F	Output fall time From 90% to 10% of V_{OUT}					60	120	μs
T_R	Output rise time From 10% to 90% of V_{OUT}			$V_{IN} = 1.8\text{ V}$ $C_{LOAD} = 1\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$	No cap on GATE pin		0.12	
		Gate capacitor = 1 nF				0.6		
		Gate capacitor = 10 nF				5.5		
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}	Without Cgate				15		μs
		With 1 nF on Gate				85		μs
T_F	Output fall time From 90% to 10% of V_{OUT}					35		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

NCV459

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J between -40°C to $+125^{\circ}\text{C}$ for V_{IN} between 0.75 V and 5.5 V, and V_{BIAS} between 1.2 V and 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
--------	-----------	------------	-----	-----	-----	------

TIMINGS (Note 6)

T_R	Output rise time From 10% to 90% of V_{OUT}	$V_{IN} = 1\text{ V}$ $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 25\ \Omega$	No cap on GATE pin		0.01	ms
			Gate capacitor = 1 nF		1	
			Gate capacitor = 10 nF		13	
T_{en}	Enable time From En V_{ih} to 10% of V_{OUT}	$V_{IN} = 1\text{ V}$ $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 25\ \Omega$	Without Cgate		10	μs
			With 1 nF on Gate		0.4	ms
T_F	Output fall time			20		μs

Logic

V_{IH}	High-level input voltage		0.9			V
V_{IL}	Low-level input voltage				0.4	V
R_{EN}	Pull down resistor		3		7	$\text{M}\Omega$

QUIESCENT CURRENT

I_{VBIAS}	V_{BIAS} Quiescent current	$V_{BIAS} = 3.3\text{ V}$, EN = high		1.3	5	μA
I_{INQ}	IN Quiescent current	EN = high		0.01	0.3	μA
I_{STBIN}	Standby current IN	EN = low, IN standby current, $V_{IN} = 3.3\text{ V}$, with discharge path, $T_A = -40^{\circ}\text{C}$ to 85°C		0.01	0.5	μA
$I_{STDVbias}$	Standby current V_{BIAS}	$V_{BIAS} = 3.3\text{ V}$ EN = low, $T_A = -40^{\circ}\text{C}$ to 85°C		0.4	1.5	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

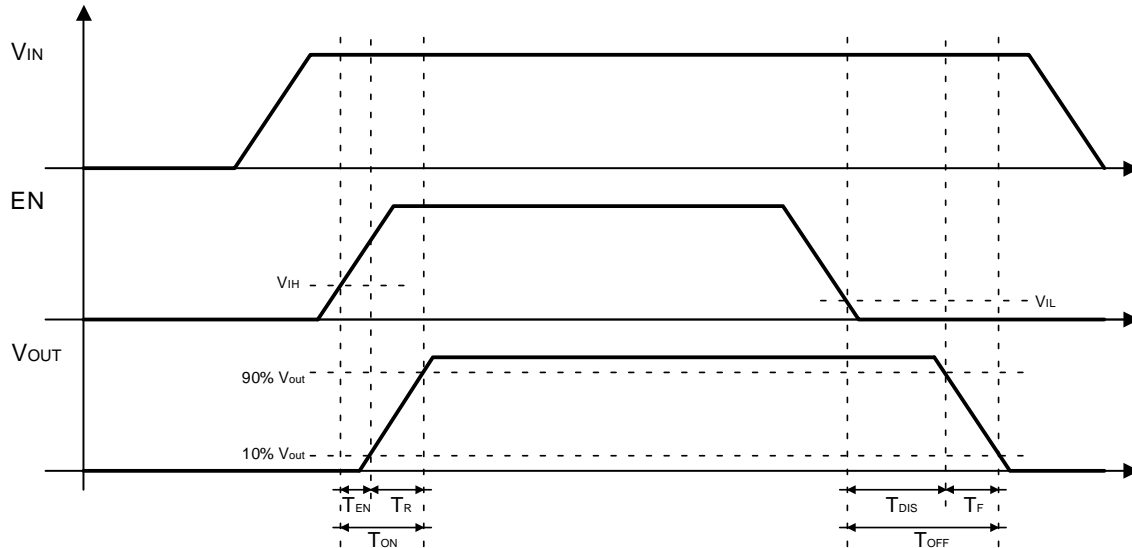


Figure 4. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

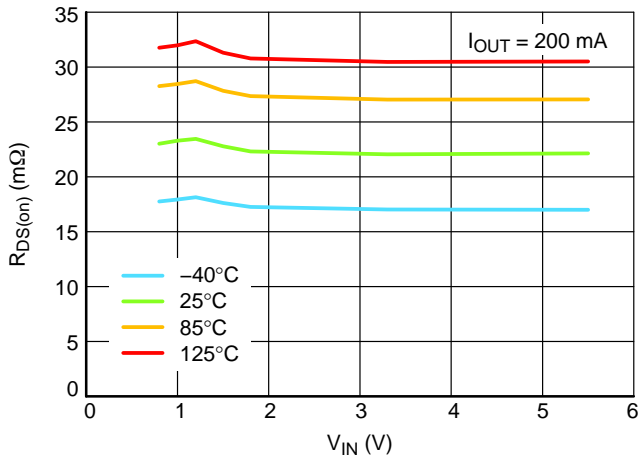


Figure 5. $R_{DS(on)}$ vs. V_{IN} , Multi Junction Temperature

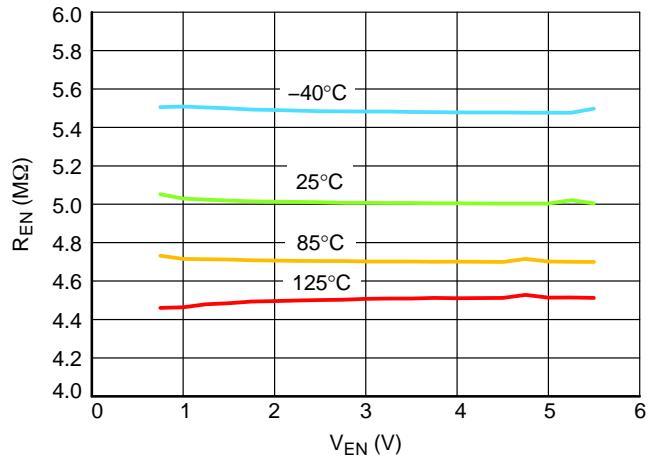


Figure 6. Pull Down Resistor vs. V_{EN} , Multi Junction Temperature

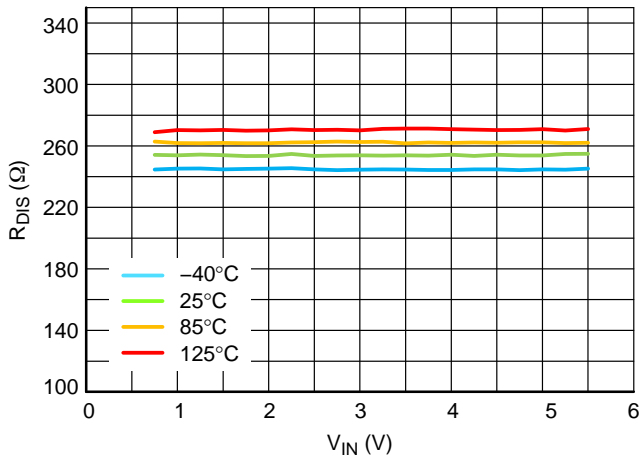


Figure 7. Output Discharge Resistor vs. V_{IN} , Multi Junction Temperature

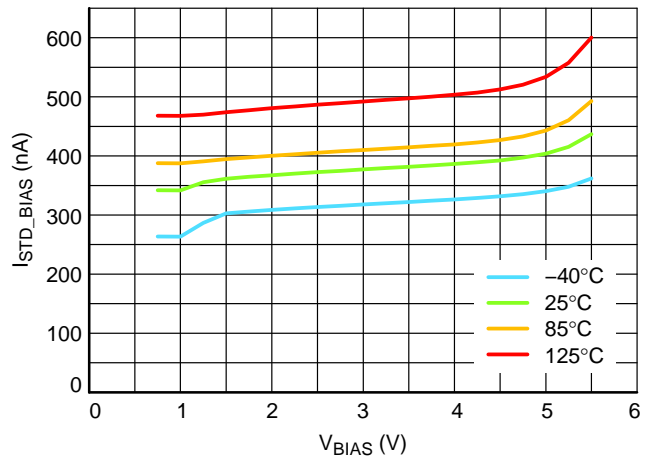


Figure 8. BIAS Standby Current vs. V_{BIAS} , Multi Junction Temperature

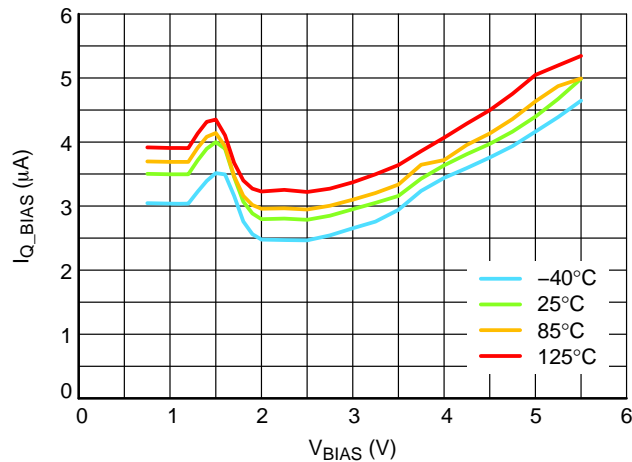


Figure 9. BIAS Quiescent Current vs. V_{BIAS} , Multi Junction Temperature

TYPICAL CHARACTERISTICS

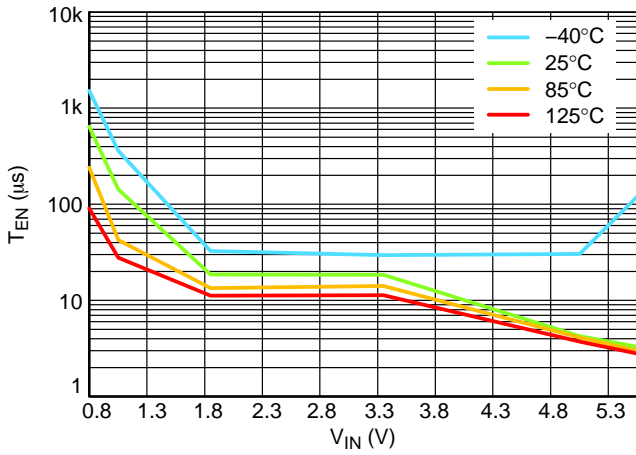


Figure 10. Enable Time vs. V_{IN} , Multi Junction Temperature (without Cgate)

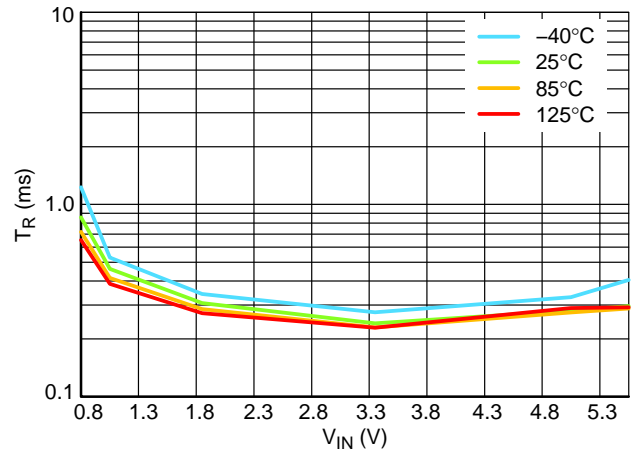


Figure 11. Rise Time vs. V_{IN} , Multi Junction Temperature (without Cgate)

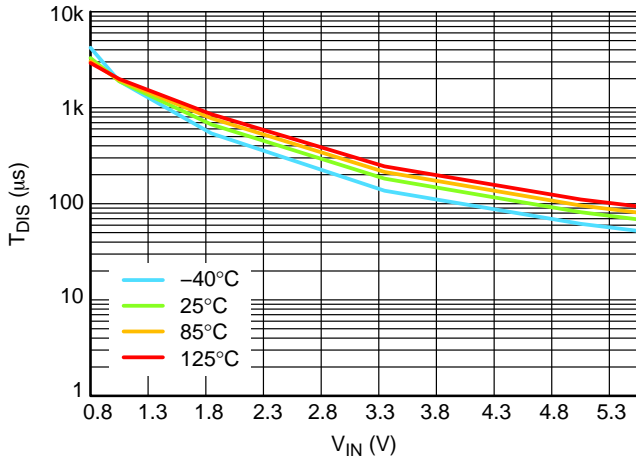


Figure 12. Disable Time vs. V_{IN} , Multi Junction Temperature, V_{BIAS} and V_{IN} Tied Together

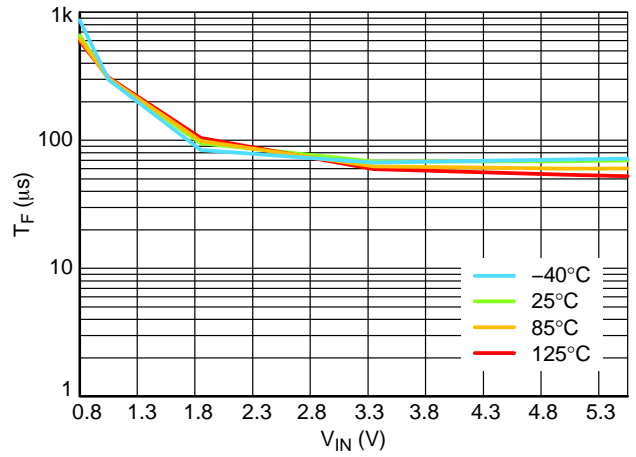


Figure 13. Fall Time vs. V_{IN} , Multi Junction Temperature, V_{BIAS} and V_{IN} Tied Together $R_{load} 25 \Omega$

FUNCTIONAL DESCRIPTION

Overview

The NCV459 are high side N channel MOSFET power distribution switch designed to isolate ICs connected on the LDO or DCDC supplies in order to save energy. The part can be used with a wide range of supply from 0.75 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing NMOS switch off.

The IN/OUT path is activated with a minimum of V_{BIAS} min, V_{in} min and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at R_{DIS} value.

Vbias Rail

The core of the IC is supplied thanks to Vbias supply rail (common +5 V, 3.3 V, 1.8 V, 1.2 V). Indeed, no current

consumption is used on IN pin, allowing to improve power saving of the rail that must be isolated by the power switch.

If Vbias rail is not available or used, Vbias pin and V_{in} pin can be connected together as close as possible the DUT. A minimum of 1.2 V is necessary to control the IC. It is recommended to connect external capacitor 10 μ F due to better EMC immunity.

Output rise time – Gate control

The NMOS is control with internal charge pump and driver. A minimum gate slew rate is internally set to avoid huge inrush current when EN is set from low to high. The default gate slew rate depends on V_{in} level. The higher V_{in} level, the longer rise time.

In addition, an external capacitor can be connected between Gate pin and GND in order to slow down the gate rising. See electrical table for more details.

Cin and Cout Capacitors

100 nF external capacitors must be connected as close as possible the DUT for noise immunity and better stability. In case of input hot plug (input voltage connected with fast slew rate – few μ s – it's strongly recommended to avoid big capacitor connected on the input. That allows to avoid input over voltage transients.

NCV459

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times (I_{OUT})^2 \quad (\text{eq. 1})$$

P_D	= Power dissipation (W)
$R_{DS(on)}$	= Power MOSFET on resistance (Ω)
I_{OUT}	= Output current (A)
$T_J = P_D \times R_{\theta JA} + T_A$	(eq. 2)
T_J	= Junction temperature ($^{\circ}\text{C}$)
$R_{\theta JA}$	= Package thermal resistance ($^{\circ}\text{C}/\text{W}$)
T_A	= Ambient temperature ($^{\circ}\text{C}$)

ORDERING INFORMATION

Device	Marking	Option	Package	Shipping†
NCV459NMWTBG	45A	Auto Discharge 230 Ω	DFNW8 3 x 3 mm (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

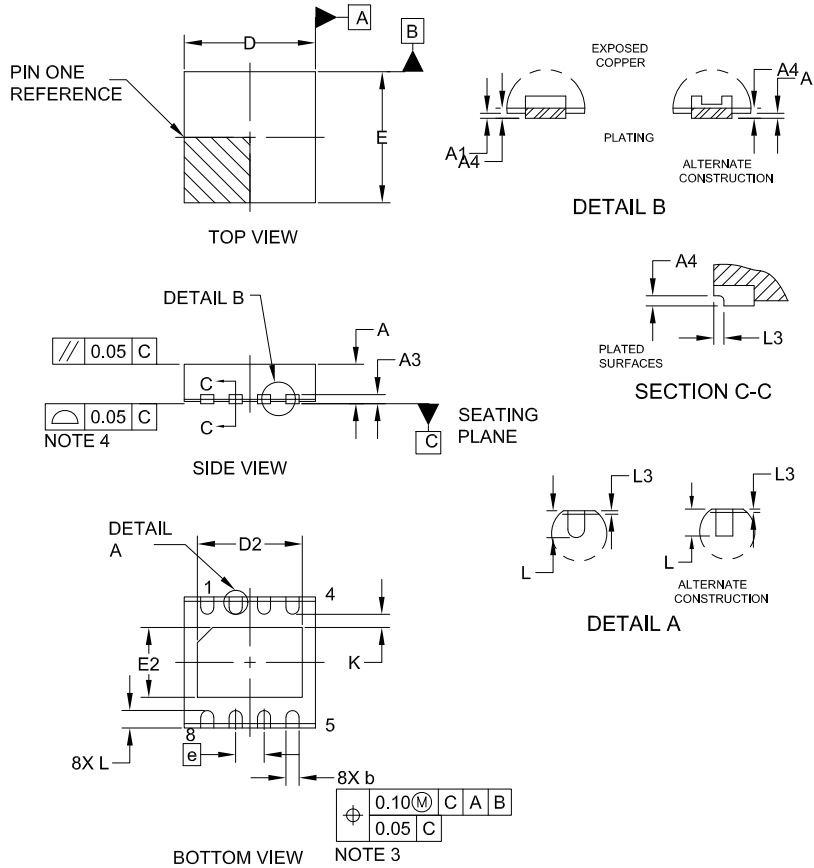
ON Semiconductor®



SCALE 2:1

DFNW8 3x3, 0.65P CASE 507AB ISSUE E

DATE 02 JUL 2021

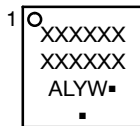


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	—	—	0.05
A3	0.20 REF		
A4	0.10	—	—
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
e	0.65 BSC		
K	0.30 REF		
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

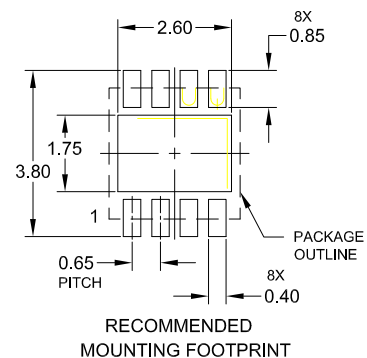
GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



DOCUMENT NUMBER:	98AON14978G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFNW8 3x3, 0.65P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:



Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View NCV459MNWTBG on WIN SOURCE](#)
-  [ON Semiconductor Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management