THE DATASHEET OF

NE5230NG

Operational Amplifier, Low Voltage

NCV5230

The NCV5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8 V or as high as 15 V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9 V supply voltages, the current required is only 110 μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 250 kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600 kHz while the supply current is increased to 600 μA. In this mode, the part will supply full power output beyond the audio range.

The NCV5230 also has a unique input stage that allows the common−mode input range to go above the positive and below the negative supply voltages by 250 mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally−compensated to reduce external component count.

The NCV5230 has a low input bias current of typically ±40 nA, and a large open−loop gain of 125 dB. These two specifications are beneficial when using the device in transducer applications. The large open−loop gain gives very accurate signal processing because of the large “excess” loop gain in a closed−loop system.

The output stage is a class AB type that can swing to within 100 mV of the supply voltages for the largest dynamic range that is needed in many applications. The NCV5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30 $nV/\sqrt{Hz}$ noise specification.

Features

- Works Down to 1.8 V Supply Voltages
- Adjustable Supply Current
- Low Noise
- Common−mode Includes Both Rails
- V_{OUT} Within 100 mV of Both Rails
- These are Pb−Free Devices

Applications

- Portable Precision Instruments
- Remote Transducer Amplifier
- Portable Audio Equipment
- Rail−to−Rail Comparators
- Half−wave Rectification without Diodes
- Remote Temperature Transducer with 4.0 to 20 mA Output Transmission

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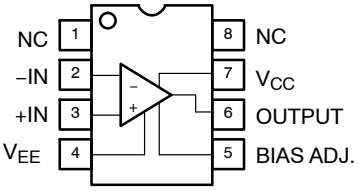
PIN CONNECTIONS

N, D Packages



(Top View)

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 15 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Single Supply Voltage	V_{CC}	18	V
Dual Supply Voltage	V_S	±9	V
Input Voltage (Note 1)	V_{IN}	±9 (18)	V
Differential Input Voltage (Note 1)		$\pm V_S$	V
Common−Mode Voltage (Positive)	V_{CM}	V_{CC} + 0.5	V
Common−Mode Voltage (Negative)	V_{CM}	V_{EE} − 0.5	V
Power Dissipation (Note 2)	P_D	500	mW
Thermal Resistance, Junction−to−Ambient D Package	$R_{\theta JA}$	182	°C/W
Operating Junction Temperature (Note 2)	T_J	150	°C
Operating Temperature Range	T_A	−40 to 125	°C
80 Output Short−Circuit Duration to Either Power Supply Pin (Notes 2 and 3)		Indefinite	s
Storage Temperature	T_{stg}	−65 to 150	°C
Lead Soldering Temperature (10 sec max)	T_{sld}	230	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Can exceed the supply voltages when $V_S \leq \pm 7.5$ V (15 V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
   Derate above 25°C at the following rates:
   D package at 5.5 mW/°C.
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Value	Unit
Single Supply Voltage	1.8 to 15	V
Dual Supply Voltage	±0.9 to ±7.5	V
Common−Mode Voltage (Positive)	V_{CC} + 0.25	V
Common−Mode Voltage (Negative)	V_{EE} − 0.25	V
Temperature	−40 to +125	°C

DC AND AC ELECTRICAL CHARACTERISTIC Unless otherwise specified, ±0.9V ≤ Vs ≤ ±7.5 V or equivalent single supply, R_L = 10 kΩ, full input common−mode range, over full operating temperature range.

Characteristic		Symbol	Test Conditions		Bias	Min	Typ	Max	Unit
NCV5230									
Offset Voltage		V_{OS}	T_A = 25°C		Any		0.4	3.0	mV
			T_A = T_{low} to T_{high}		Any		3.0	4.0	
Drift		V_{OS}			Any		2.0	5.0	μV/°C
Offset Current		I_{OS}	T_A = 25°C		High		3.0	50	nA
					Low		3.0	30	
			T_A = T_{low} to T_{high}		High			100	
					Low			60	
Drift		I_{OS}			High		0.5	1.4	nA/°C
					Low		0.3	1.4	
Bias Current		I_B	T_A = 25°C		High		40	150	nA
					Low		20	60	
			T_A = T_{low} to T_{high}		High			300	
					Low			300	
Drift		I_B			High		2.0	4.0	nA/°C
					Low		2.0	4.0	
Supply Current		I_S	V_S = ±0.9 V	T_A = 25°C	Low		110	160	μA
					High		600	750	
				T_A = T_{low} to T_{high}	Low			275	
					High			850	
			V_S = ±7.5 V	T_A = 25°C	Low		320	550	μA
					High		1100	1600	
				T_A = T_{low} to T_{high}	Low			600	
					High			1700	
Common−Mode Input Range		V_{CM}	V_{OS} ≤ 6 mV, T_A = 25°C		Any	V^- − 0.25		V^+ + 0.25	V
			V_{OS} ≤ 20 mV, T_A = T_{low} to T_{high}		Any	V^-		V^+	
Common−Mode Rejection Ratio		CMRR	V_S = ±7.5 V	R_S = 10 kΩ; V_{CM} = ±7.5 V; T_A = 25°C	Any	85	95		dB
				R_S = 10 kΩ; V_{CM} = ±7.5 V; T_A = T_{low} to T_{high}	Any	80			
Power Supply Rejection Ratio		PSRR	T_A = 25°C		High	90	105		dB
					Low	85	95		
			T_A = T_{low} to T_{high}		High	75			
					Low	80			
Load Current	Source	I_L	V_S = ±0.9 V; T_A = 25°C		High	4.0	6		mA
	Sink		V_S = ±0.9 V; T_A = 25°C		High	5.0	7		
	Source		V_S = ±7.5 V; T_A = 25°C		High		16		
	Sink		V_S = ±7.5 V; T_A = 25°C		High		32		
	Source		V_S = ±0.9 V; T_A = T_{low} to T_{high}		Any	1.0	5		
	Sink		V_S = ±0.9 V; T_A = T_{low} to T_{high}		Any	2.0	6		
	Source		V_S = ±7.5 V; T_A = T_{low} to T_{high}		Any	4.0	10		
	Sink		V_S = ±7.5 V; T_A = T_{low} to T_{high}		Any	5.0	15		

For NCV5230 devices, T_{low} = −40°C and T_{high} = +125°C.

DC AND AC ELECTRICAL CHARACTERISTIC Unless otherwise specified, ±0.9V ≤ Vs ≤ ±7.5 V or equivalent single supply, R_L = 10 kΩ, full input common−mode range, over full operating temperature range.

Characteristic	Symbol	Test Conditions		Bias	Min	Typ	Max	Unit
NCV5230								
Large−Signal Open−Loop Gain	A_{VOL}	V_S = ±7.5 V	R_L = 10 kΩ; T_A = 25°C	High	120	2000		V/mV
				Low	60	750		
			T_A = T_{low} to T_{high}	High	100			
				Low	50			
Output Voltage Swing	V_{OUT}	V_S = ±0.9 V	T_A = 25°C +SW	Any	750	800		mV
			T_A = 25°C −SW	Any	750	800		
			T_A = T_{low} to T_{high}; +SW	Any	700			
			T_A = T_{low} to T_{high}; −SW	Any	700			
		V_S = ±7.5 V	T_A = 25°C +SW	Any	7.30	7.35		V
			T_A = 25°C −SW	Any	−7.32	−7.35		
			T_A = T_{low} to T_{high}; +SW	Any	7.25	7.30		
			T_A = T_{low} to T_{high}; −SW	Any	−7.30	−7.35		
Slew Rate	SR	T_A = 25°C		High		0.25		V/μs
				Low		0.09		V/μs
Inverting Unity Gain Bandwidth	BW	C_L = 100 pF; T_A = 25°C		High		0.6		MHz
				Low		0.25		MHz
Phase Margin	θ_M	C_L = 100 pF; T_A = 25°C		Any		70		°
Settling Time	t_S	C_L = 100 pF, 0.1%		High		2.0		μs
				Low		5.0		μs
Input Noise	V_{INN}	R_S = 0 Ω; f = 1.0 kHz		High		30		nV/$\sqrt{Hz}$
				Low		60		nV/$\sqrt{Hz}$
Total Harmonic Distortion	THD	V_S = ±7.5 V A_V = 1; V_{IN} = 500 mV; f = 1.0 kHz		High		0.003		%
		V_S = ±0.9 V A_V = 1, V_{IN} = 500 mV; f = 1.0 kHz		High		0.002		%

For NCV5230 devices, T_{low} = −40°C and T_{high} = +125°C.

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NCV5230 has a common−mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250 mV without increasing the input offset voltage by more than 6.0 mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail−to−rail input common−mode range, two emitter−coupled differential pairs are placed in parallel so that the common−mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter−coupler transistors are configured to form the basic input stage cell. Common−mode input signal voltages in the range from 0.8 V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common−mode input signal voltages in the range of V_{EE} to 0.8 V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail−to−rail capability. As the common−mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common−mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non−conducting. When the common−mode input voltage passes below the reference voltage, V_{B1} − 0.8 V at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120 mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common−mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross−coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3 mV and a change in the input offset voltage of less than 0.1 mV.

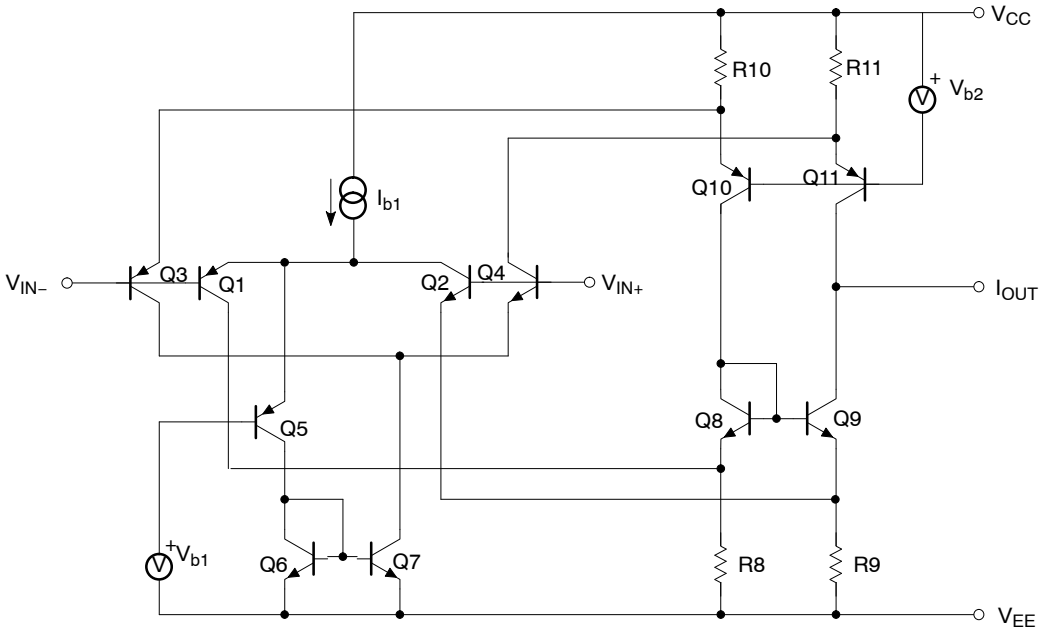


Figure 1. Input Stage

Output Stage

Processing output voltage swings that nominally reach to less than 100 mV of either supply voltage can only be achieved by a pair of complementary common−emitter connected transistors. Normally, such a configuration causes complex feed−forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NCV5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2 and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10 mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10 mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base−emitter diodes of the output transistors Q1 and Q3. The base−emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base−emitter diode of Q7 and R7. The summed voltage across the base−emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} - I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in−phase driving signals on the bases of Q5 and Q2. This is very important for simple high−frequency compensation. The output transistors can be high−frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general−purpose op amp of this type must have enough open−loop gain for applications when the output is driving a low resistance load. The NCV5230 accomplishes this by inserting an intermediate common−emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles − one at the output of each common−emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole−splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole−splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally−compensated op amp with a phase margin of 70°.

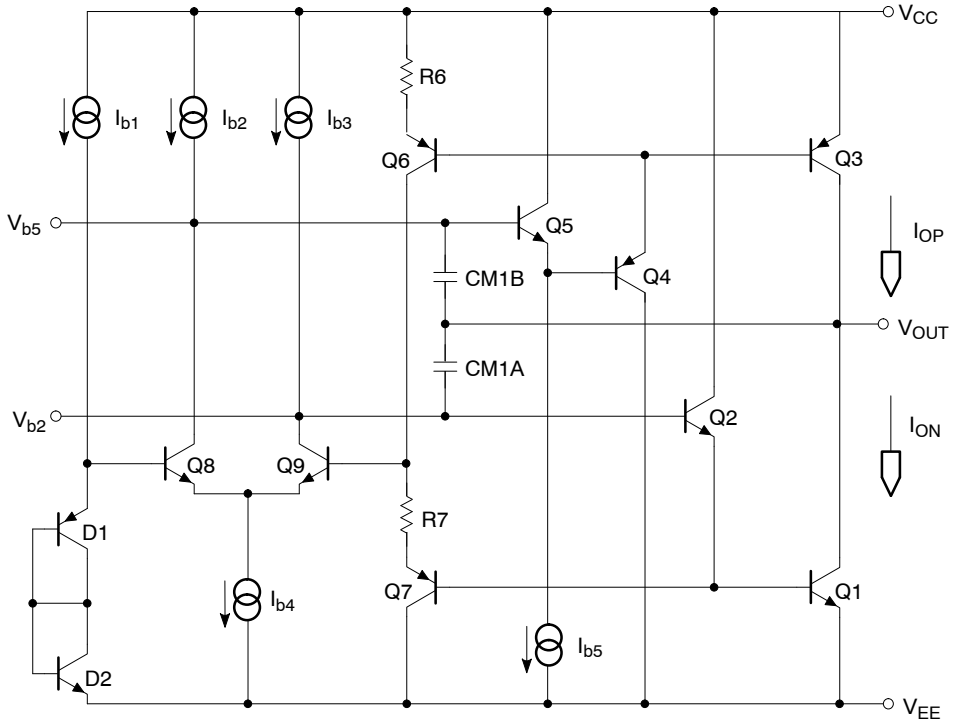


Figure 2. Output Stage

THERMAL CONSIDERATIONS

When using the NCV5230, the internal power dissipation capabilities of each package should be considered. ON Semiconductor does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_j = T_{amb} + (P_D \times \theta_{JA}) \quad \text{(eq. 1)}$$

Where

T_{amb} = Ambient Temperature
T_j = Die Temperature
P_D = Power Dissipation
= (I_{CC} x V_{CC})
θ_{JA} = Package Thermal Resistance
= 270°C/W for SO−8 in PC Board Mounting

See the packaging section for information regarding other methods of mounting.

θ_{JA} − 100°C/W for the plastic DIP.

The maximum supply voltage for the part is 15 V and the typical supply current is 1.1 mA (1.6 mA max). For operation at supply voltages other than the maximum, see the data sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100 μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower Mean Time Between Failures (MTBF). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NCV5230 is a very user−friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current−control pin depends on the trade−offs which can be made in the designer's application. The graphs in Figures 3 and 4 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100 μA to 600 μA for a supply voltage of 1.8 V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1.0 Ω to 100 kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain−bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5.0 μs at low bias to 2.0 μs at high bias. The supply current control can also be utilized for wave−shaping applications such as for pulse or triangular waveforms. The gain−bandwidth can be varied from between 250 kHz at low bias to 600 kHz at high bias current. The slew rate range is 0.08 V/μs at low bias and 0.25 V/μs at high bias.

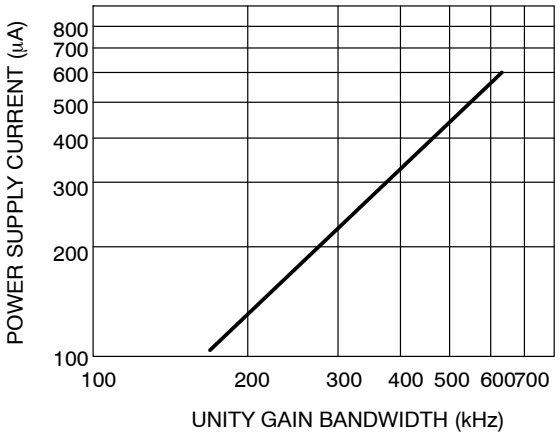


Figure 3. Unity Gain Bandwidth vs. Power Supply Current for V_{CC} = ±0.9 V

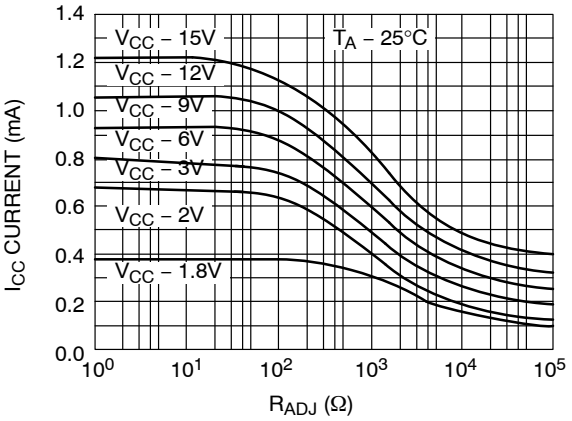


Figure 4. I_{CC} Current vs. Bias Current Adjusting Resistor for Several Supply Voltages

The full output power bandwidth range for V_{CC} equals 2.0 V, is above 40 kHz for the maximum bias current setting and greater than 10 kHz at the minimum bias current setting.

If extremely low signal distortion (<0.05%) is required at low supply voltages, exclude the common−mode crossover point (V_{B1}) from the common−mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common−mode range of the amplifier. This leads to another helpful and unique property of the NCV5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common−mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non−inverting voltage−follower configuration. This is shown in Figure 5 where the input sine wave allows an undistorted output sine wave which will swing less than 100 mV of either supply voltage. Many competitive parts will show severe clipping caused by input common−mode limitations. The NCV5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

There are not as many considerations when designing with the NCV5230 as with other devices. Since the NCV5230 is internally−compensated and has a unity gain−bandwidth of 600 kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NCV5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low−pass RC network as close to the supply pins as possible to eliminate 60 Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NCV5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

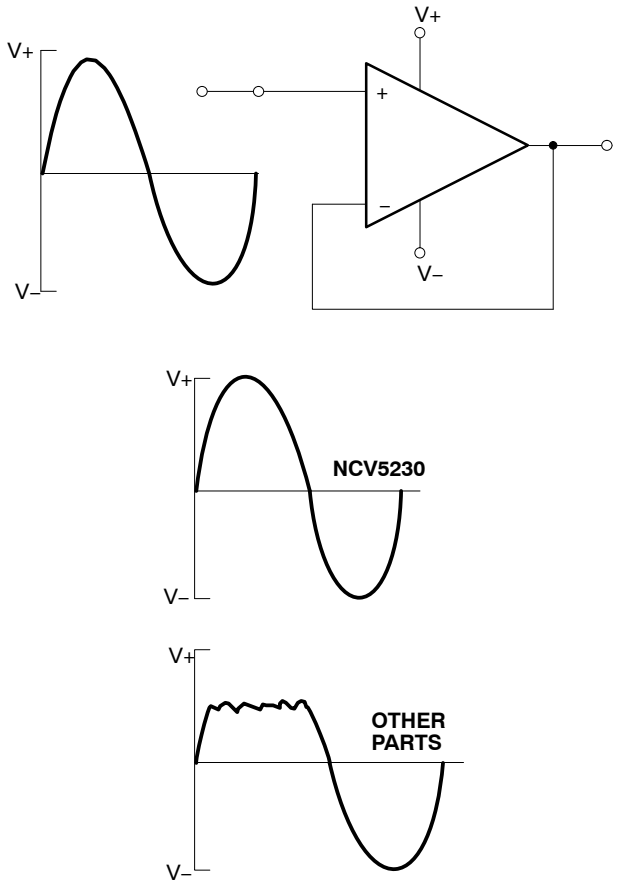


Figure 5. In a non−inverting voltage−follower configuration, the NCV5230 will give full rail−to−rail swing. Other low voltage amplifiers will not because they are limited by their input common−mode range and output swing capability.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4.0 to 20 mA information which is used in many control−type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NCV5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuits for this are shown in Figures 6 and 7. Here, the part is configured as a voltage−to−current, or transconductance amplifier. This is a novel circuit that takes advantage of the NCV5230's large open−loop gain. In AC applications, the load current will decrease as the open−loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NCV5230 must also be considered in this application.

The NCV5230 circuit shown in Figure 6 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non−inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage−follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current−follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = \frac{V_{IN}}{R_C} \qquad \text{(eq. 2)}$$

and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NCV5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NCV5230 is as follows:

$$R_{Lmax} = \frac{[V_{remote\ supply} - V_{CC\ min} - V_{IN\ max}]}{I_L} \qquad \text{(eq. 3)}$$

Where $V_{CC\ min}$ is the worst−case power supply voltage (approximately 1.8 V) that will still keep the part operational. As an example, when using a 15 V remote power supply, a current sensing resistor of 1.0 Ω, and an input voltage (V_{IN}) of 20 mV, the output current (I_L) is 20 mA. Furthermore, a load resistance of zero to approximately 650 Ω can be inserted in the loop without any change in current when the bias current−control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NCV5230 because it will operate down to 1.8 V. With a 15 V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20 mA output into the 650 Ω load.

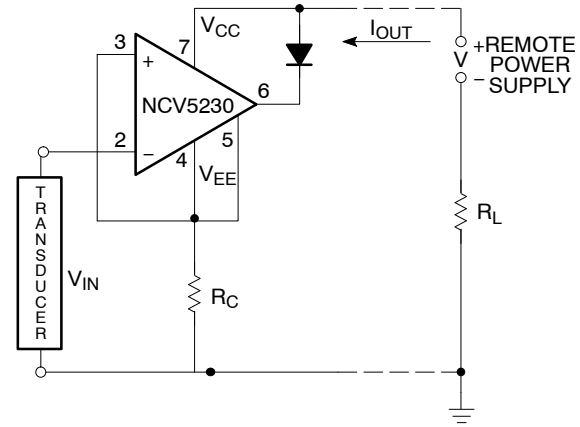


Figure 6. The NCV5230 as a Remote Transducer Transconductance Amp with 4.0 − 20 mA Current Transmission Output Capability

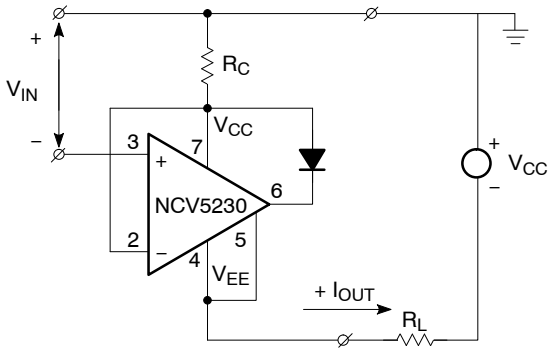


Figure 7. The Same Type of Circuit as Figure 6, but for Sourcing Current to the Load

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650 Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NCV5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NCV5230 transconductance configuration.

The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4.0 to 20 mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 7 can be used with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NCV5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (Figure 8). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NCV5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.

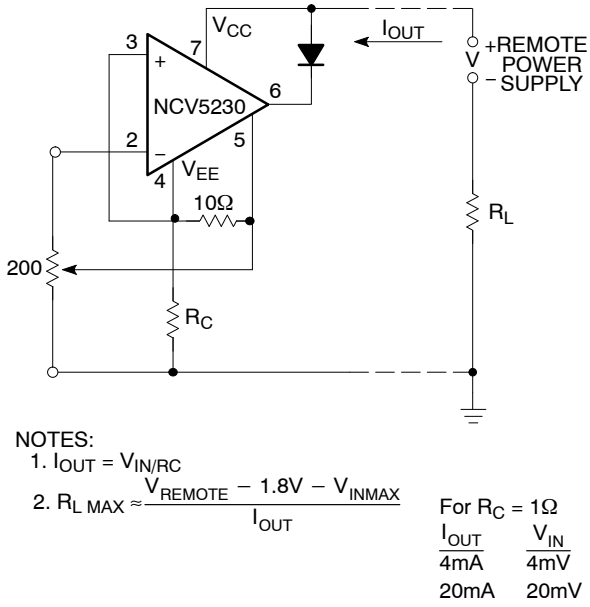


Figure 8. NCV5230 remote temperature transducer utilizing 4.0 – 20 mA current transmission. This application shows the use of the accessibility of the PTAT cell in the device to make the part, itself, a transducer.

HALF−WAVE RECTIFIER WITH RAIL−TO−GROUND OUTPUT SWING

Since the NCV5230 input common−mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half−wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive− or negative−going outputs, depending on the way the bias is arranged. In Figure 9, the circuit is biased to ground, while circuit (Figure 10) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NCV5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of “hard” saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NCV5230 into “saturation” and obtain half−wave rectification with good recovery. The simplicity of biasing and the rail−to−ground half−sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one−half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half−wave that can have a peak equal to the total supply voltage. The photographs in Figure 11 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NCV5230 can achieve in this configuration.

Half−Wave Rectifier With Positive−Going Output Swings

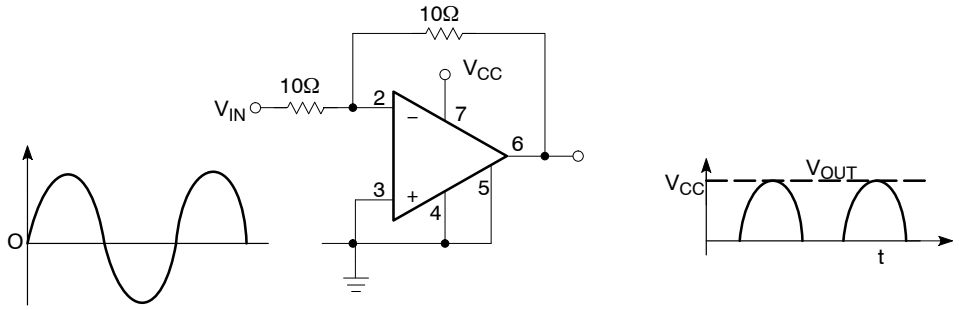


Figure 9. Rail−to−Ground Output Swing Referenced to Ground

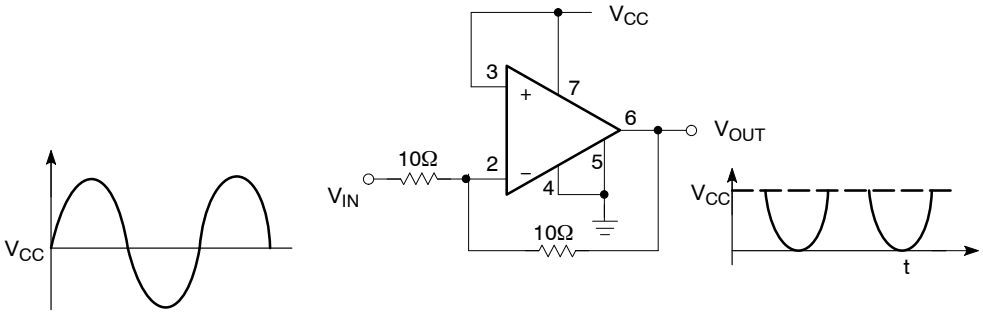
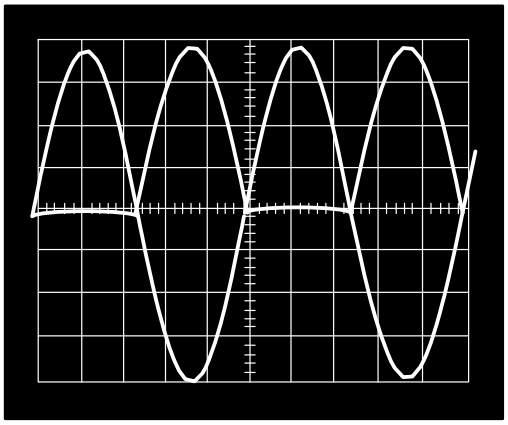
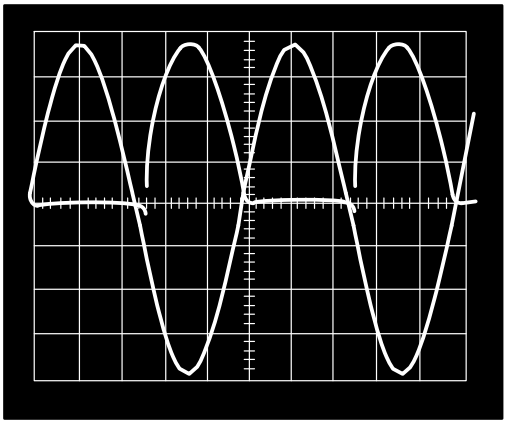


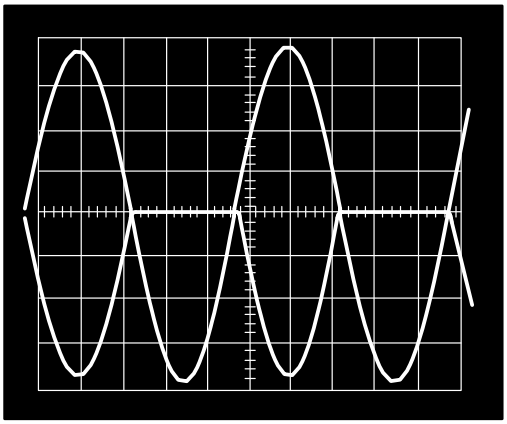
Figure 10. Negative−Going Output Referenced to V_{CC}



500 mV/Div 200μS /Div
Biased to Ground



500 mV/Div 20 μS/Div
Biased to Ground



500 mV/Div 20 μS/Div
Biased to Positive Rail

Figure 11. Performance Waveforms for the Circuits in Figures 9 and 10.
Good response is shown at 1.0 and 10 kHz for both circuits under full swing with a 2.0 V supply.

By adding another NCV5230 in an inverting summer configuration at the output of the half−wave rectifier, a full−wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 12. The summing network combines the input signal at the half−wave and adds it to double the half−wave's output, resulting in the full−wave. The output waveform can be referenced to the supply or ground, depending on the half−wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full−wave output for meters or chart recorders that need DC levels.

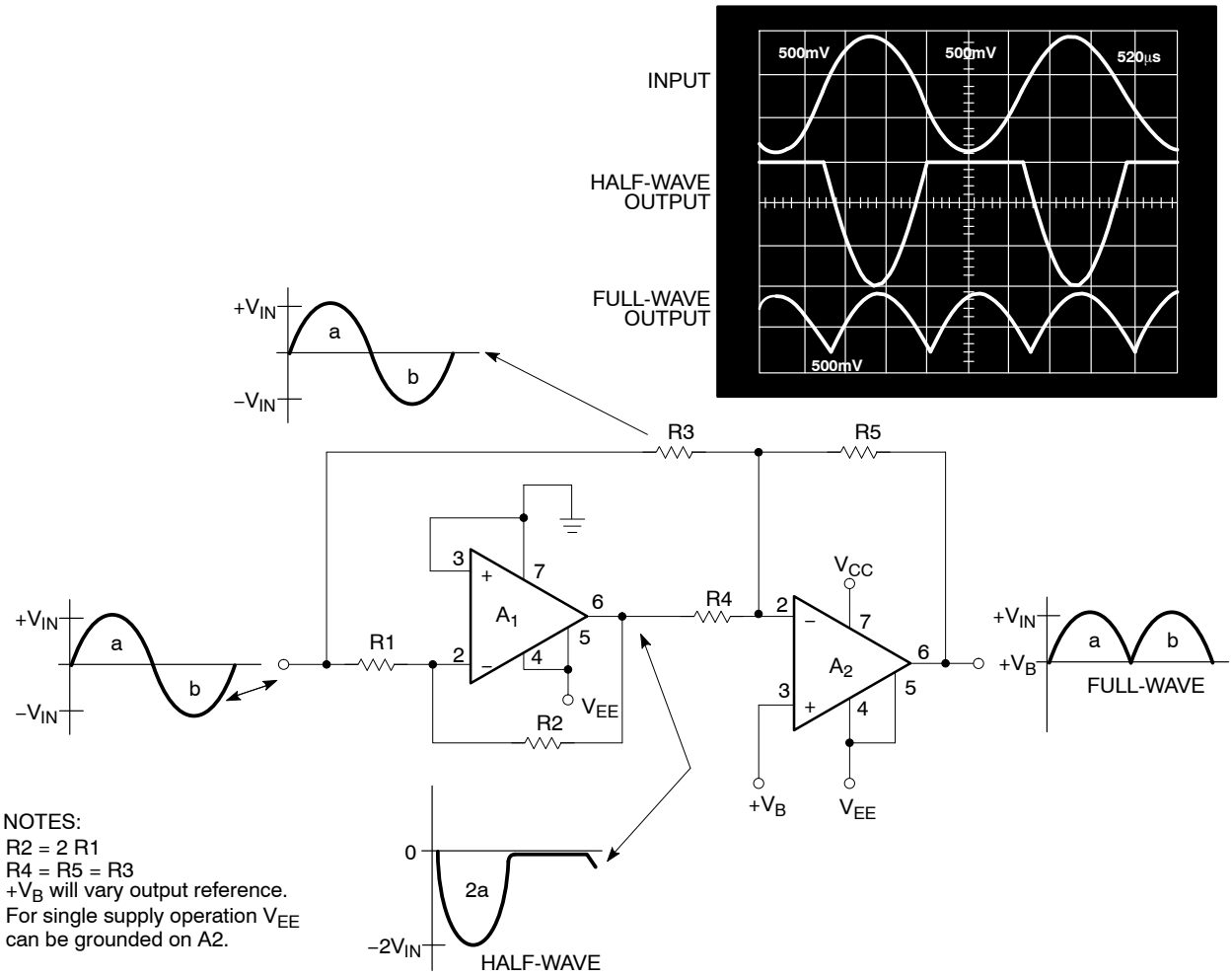


Figure 12. Adding an Inverting Summer to the Input and Output of the Half−Wave will Result in Full−Wave

CONCLUSION

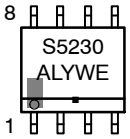
The NCV5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NCV5230's special input and output stages.

The NCV5230 has a combination of novel specifications which allows the designer to implement it easily into existing low−supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs where S/N ratios are important. The wide full−power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open−loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105 dB.

REFERENCES

1. Johan H. Huijsing, *Multi−stage Amplifier with Capacitive Nesting for Frequency Compensation*, U.S. Patent Application Serial No. 602.234, filed April 19, 1984.
2. Bob Blauschild, *Differential Amplifier with Rail−to−Rail Capability*, U.S. Patent Application Serial No. 525.181, filed August 23, 1983.
3. *Operational Amplifiers − Characteristics and Applications*, Robert G. Irvine, Prentice−Hall, Inc., Englewood Cliffs, NJ 07632, 1981.
4. *Transducer Interface Handbook − A Guide to Analog Signal Conditioning*, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

MARKING DIAGRAMS



SOIC−8
D SUFFIX
CASE 751

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Description	Temperature Range	Shipping†
NCV5230DR2G	8−Pin Plastic Small Outline (SO−8) Package (Pb−Free)	−40°C to +125°C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

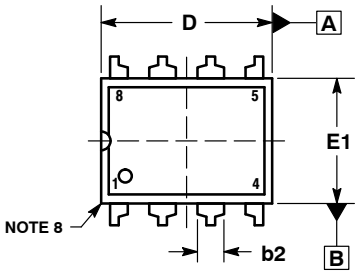
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

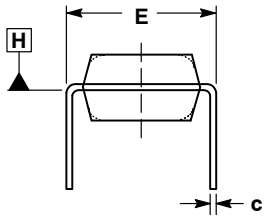
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

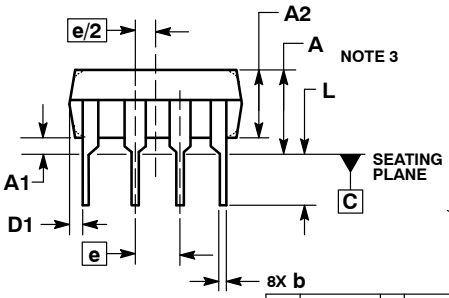
DATE 22 APR 2015



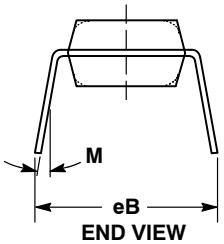
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



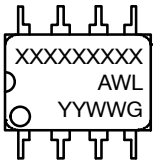
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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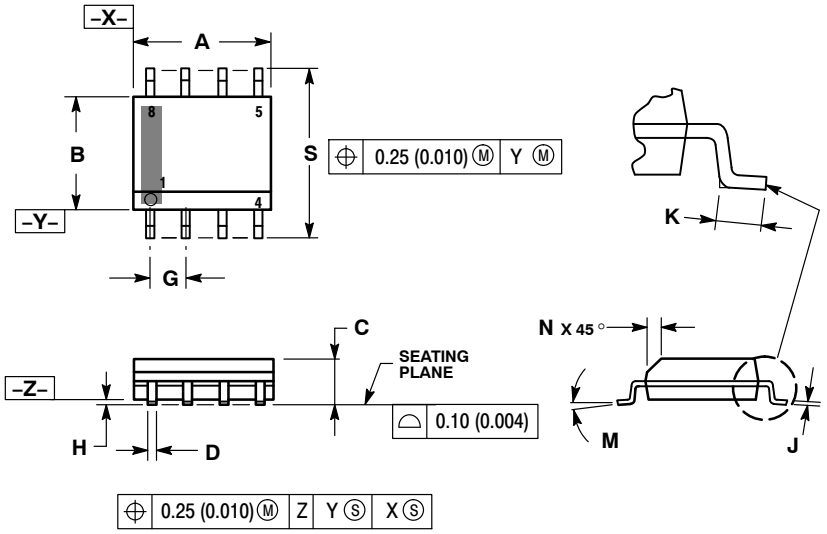
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

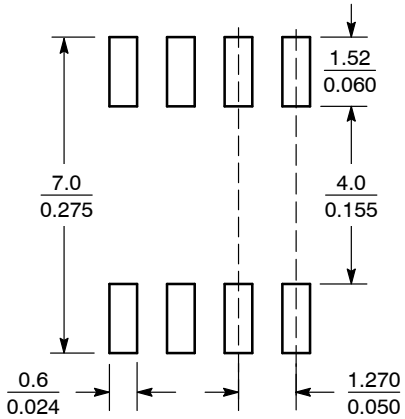
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

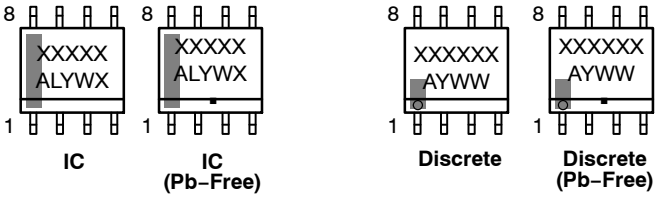
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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- Excess Inventory Management