



**THE DATASHEET OF
CM2009-00QR**



CM2009

VGA Port Companion Circuit

Product Description

The CM2009 connects between a video graphics controller embedded in a PC, graphics adapter card or set top box and the VGA or DVI-I port connector. The CM2009 incorporates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the video, DDC and SYNC lines is implemented with low-capacitance current steering diodes.

All ESD diodes are designed to safely handle the high current spikes specified by IEC-61000-4-2 Level 4 (± 8 kV contact discharge if C_{BYP} is present, ± 4 kV if not). The ESD protection for the DDC signal pins are designed to prevent “back current” when the device is powered down while connected to a monitor that is powered up.

Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs to provide design flexibility in multi-supply-voltage environments.

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the video controller IC (SYNC1, SYNC2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and V_{CC_SYNC} , which is typically 5 V. Additionally, each driver has a series termination resistor (R_T) connected to the SYNC_OUT pin, eliminating the external termination resistors typically required for the HSYNC and VSYNC lines of the video cable. There are three versions with different values of R_T to allow termination at typically 65Ω (CM2009-00) or 15Ω (CM2009-02).

The 15Ω (CM2009-02) version will typically require two external resistors which can be chosen to exactly match the characteristic impedance of the SYNC lines of the video cable.

Two N-channel MOSFETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. The gate terminals for these MOSFETs (V_{CC_DDC}) should be connected to the supply rail (typically 3.3 V) that supplies power to the transceivers of the DDC controller.

Features

- Includes ESD Protection, Level-Shifting, Buffering and Sync Impedance Matching
- 7 Channels of ESD Protection for all VGA Port Connector Pins Meeting IEC-61000-4-2 Level 4 ESD Requirements (± 8 kV Contact Discharge)
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines (4 pF Maximum)
- 5 V Drivers for HSYNC and VSYNC Lines
- Integrated Impedance Matching Resistors on Sync Lines
- Bi-directional Level Shifting N-Channel FETs Provided for DDC_CLK & DDC_DATA Channels
- Backdrive Protection on DDC Lines
- Compact 16-Lead QSOP Package
- These Devices are Pb-Free and are RoHS Compliant

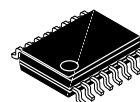
Applications

- VGA and DVI-I Ports in:
 - ◆ Desktop and Notebook PCs
 - ◆ Graphics Cards
 - ◆ Set Top Boxes



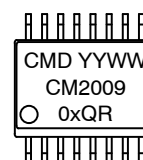
ON Semiconductor®

<http://onsemi.com>



QSOP16
QR SUFFIX
CASE 492

MARKING DIAGRAM



CM2009 0xQR = Specific Device Code
YY = Year
WW = Work Week

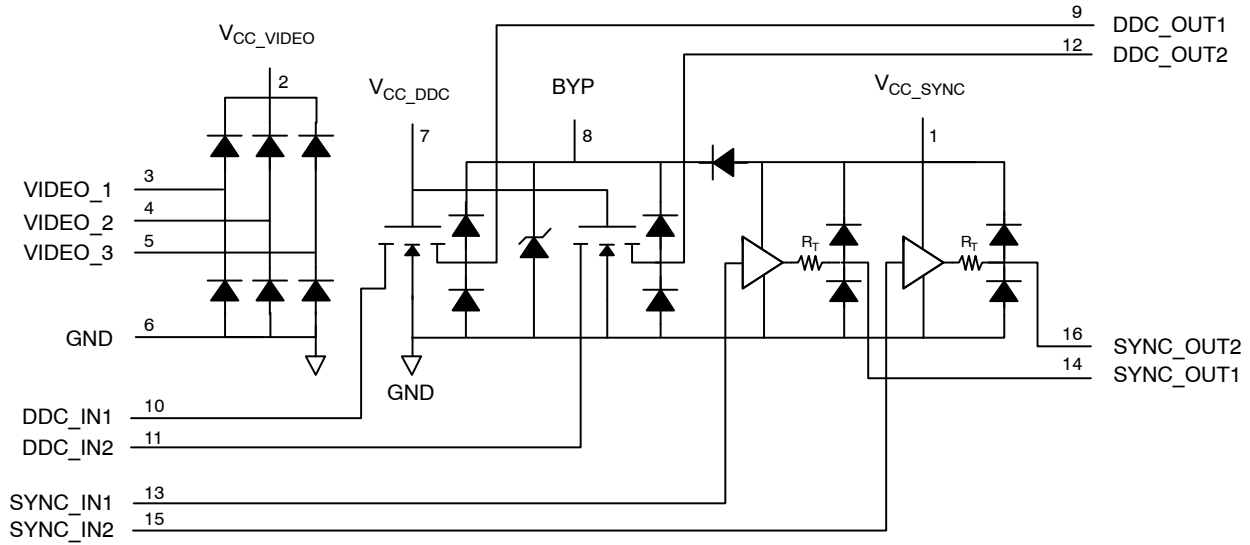
ORDERING INFORMATION

Device	Package	Shipping†
CM2009-00QR	QSOP-16 (Pb-Free)	2500/Tape & Reel
CM2009-02QR	QSOP-16 (Pb-Free)	2500/Tape & Reel

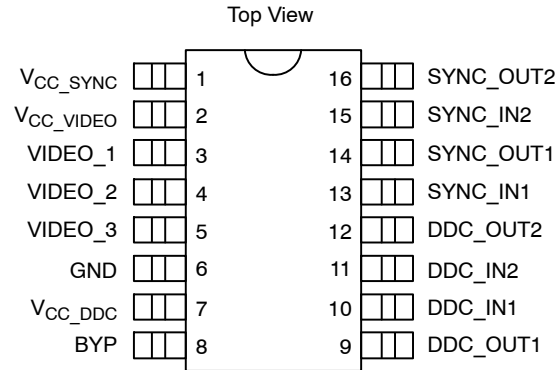
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM2009

SIMPLIFIED ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAM



16 Pin QSOP

Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
1	V _{CC_SYNC}	This is an isolated supply input for the SYNC_1 and SYNC_2 level shifters and their associated ESD protection circuits.
2	V _{CC_VIDEO}	This is a supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits.
3	VIDEO_1	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
4	VIDEO_2	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
5	VIDEO_3	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
6	GND	Ground reference supply pin.
7	V _{CC_DDC}	This is an isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates.
8	BYP	This input is used to connect an external 0.2 μF bypass capacitor to the DDC circuits, resulting in an increased ESD withstand voltage rating for these circuits (±8 kV with vs. ±4 kV without).
9	DDC_OUT1	DDC signal output. Connects to the video connector side of one of the sync lines.
10	DDC_IN1	DDC signal input. Connects to the VGA controller side of one of the sync lines.

CM2009

Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
11	DDC_IN2	DDC signal input. Connects to the VGA controller side of one of the sync lines.
12	DDC_OUT2	DDC signal output. Connects to the video connector side of one of the sync lines.
13	SYNC_IN1	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
14	SYNC_OUT1	Sync signal buffer output. Connects to the video connector side of one of the sync lines.
15	SYNC_IN2	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
16	SYNC_OUT2	Sync signal buffer output. Connects to the video connector side of one of the sync lines.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{CC_VIDEO} , V_{CC_DDC} and V_{CC_SYNC} Supply Voltage Inputs	[GND - 0.5] to +6.0	V
ESD Diode Forward Current (one diode conducting at a time)	10	mA
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 DDC_IN1, DDC_IN2 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2	[GND - 0.5] to [$V_{CC_VIDEO} + 0.5$] [GND - 0.5] to 6.0 [GND - 0.5] to 6.0 [GND - 0.5] to [$V_{CC_SYNC} + 0.5$]	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C
Package Power Rating ($T_A = 25^\circ\text{C}$)	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

CM2009

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{CC_VIDEO}	V _{CC_VIDEO} Supply Current	V _{CC_VIDEO} = 5.0 V; VIDEO inputs at V _{CC_VIDEO} or GND			10	μA
I _{CC_DDC}	V _{CC_DDC} Supply Current	V _{CC_DDC} = 5.0 V			10	μA
I _{CC_SYNC}	V _{CC_SYNC} Supply Current	V _{CC_SYNC} = 5 V; SYNC inputs at GND or V _{CC_SYNC} ; SYNC outputs unloaded			50	μA
		V _{CC_SYNC} = 5 V; SYNC inputs at 3.0 V; SYNC outputs unloaded			2.0	mA
V _F	ESD Diode Forward Voltage	I _F = 10 mA			1.0	V
V _{IH}	Logic High Input Voltage	V _{CC_SYNC} = 5.0 V; (Note 2)	2.0			V
V _{IL}	Logic Low Input Voltage	V _{CC_SYNC} = 5.0 V; (Note 2)			0.6	V
V _{OH}	Logic High Output Voltage	I _{OH} = 0 mA, V _{CC_SYNC} = 5.0 V; (Note 2)	4.85			V
V _{OL}	Logic Low Output Voltage	I _{OL} = 0 mA, V _{CC_SYNC} = 5.0 V; (Note 2)			0.15	V
R _{OUT}	SYNC Driver Output Resistance (CM2009-00 only)	V _{CC_SYNC} = 5.0 V; SYNC Inputs at GND or 3.0 V		65		Ω
R _{OUT}	SYNC Driver Output Resistance (CM2009-02 only)	V _{CC_SYNC} = 5.0 V; SYNC Inputs at GND or 3.0 V; (Note 2)		15		Ω
V _{OH-02}	Logic High Output Voltage (CM2009-02 only)	I _{OH} = 24 mA; V _{CC_SYNC} = 5.0 V; (Note 2)	2.0			V
V _{OL-02}	Logic Low Output Voltage (CM2009-02 only)	I _{OL} = 24 mA; V _{CC_SYNC} = 5.0 V; (Note 2)			0.8	V
I _{IN}	Input Current VIDEO Inputs	V _{CC_VIDEO} = 5.0 V; V _{IN} = V _{CC_VIDEO} or GND			±1	μA
	SYNC_IN1, SYNC_IN2 Inputs	V _{CC_SYNC} = 5.0 V; V _{IN} = V _{CC_SYNC} or GND			±1	μA
I _{OFF}	Level Shifting N-MOSFET "OFF" State Leakage Current	(V _{CC_DDC} - V _{DDC_IN}) ≤ 0.4 V; V _{DDC_OUT} = V _{CC_DDC}			10	μA
		(V _{CC_DDC} - V _{DDC_OUT}) ≤ 0.4 V; V _{DDC_IN} = V _{CC_DDC}			10	μA
V _{ON}	Voltage Drop Across Level-shifting N-MOSFET when "ON"	V _{CC_DDC} = 2.5 V; V _S = GND; I _{DS} = 3 mA;			0.18	V
C _{IN_VID}	VIDEO Input Capacitance	V _{CC_VIDEO} = 5.0 V; V _{IN} = 2.5 V; f = 1 MHz; (Note 4)			4	pF
		V _{CC_VIDEO} = 2.5 V; V _{IN} = 1.25 V; f = 1 MHz; (Note 4)			4.5	pF
t _{PLH}	SYNC Driver L => H Propagation Delay	C _L = 50 pF; V _{CC} = 5.0 V; Input t _R and t _F ≤ 5 ns			12	ns
t _{PHL}	SYNC Driver H => L Propagation Delay	C _L = 50 pF; V _{CC} = 5.0 V; Input t _R and t _F ≤ 5 ns			12	ns
t _R , t _F	SYNC Driver Output Rise & Fall Times	C _L = 50 pF; V _{CC} = 5.0 V; Input t _R and t _F ≤ 5 ns		4		ns
V _{ESD}	ESD Withstand Voltage	V _{CC_VIDEO} = V _{CC_SYNC} = 5 V; (Notes 3, 4 & ?)	±8			kV

- All parameters specified over standard operating conditions unless otherwise noted.
- These parameters apply only to the SYNC drivers. Note that R_{OUT} = R_T + R_{BUFFER}.
- Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method. BYP, V_{CC_VIDEO} and V_{CC_SYNC} must be bypassed to GND via a low impedance ground plane with a 0.2 μF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulses can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard ±2 kV Human Body Model (MIL-STD-883, Method 3015). The bypass capacitor at the BYP pin may optionally be omitted, in which case the max. ESD withstand voltage for the DDC_OUT1 and DDC_OUT2 pins is reduced to ±4 kV.
- The SYNC_OUT pins on the CM2009-02 are guaranteed for 2 kV HBM ESD protection.

APPLICATION INFORMATION

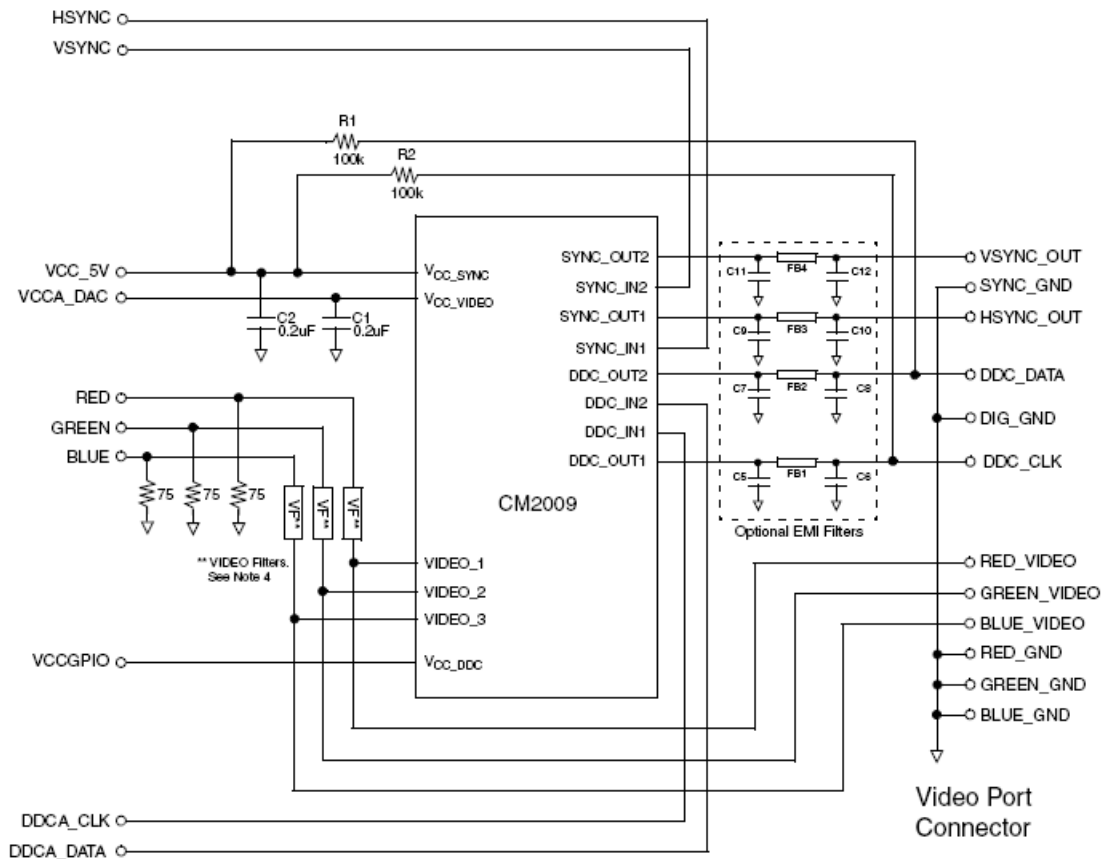


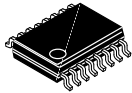
Figure 1. Typical Application Connection Diagram

NOTES:

1. The CM2009 should be placed as close to the VGA or DVI-I connector as possible.
2. The ESD protection channels VIDEO_1, VIDEO_2, VIDEO_3 may be used interchangeably between the R, G, B signals.
3. If differential video signal routing is used, the RED, BLUE, and GREEN signal lines should be terminated with external 37.5 Ω resistors.
4. “VF” are external video filters for the RGB signals.
5. Supply bypass capacitors C1 and C2 must be placed immediately adjacent to the corresponding Vcc pins. Connections to the Vcc pins and ground plane must be made with minimal length copper traces (preferably less than 5 mm) for best ESD protection.
6. The bypass capacitor for the BYP pin has been omitted in this diagram. This results in a reduction in the maximum ESD withstand voltage at the DDC_OUT pins from ± 8 kV to ± 4 kV. If 8 kV ESD protection is required, a 0.2 μ F ceramic bypass capacitor should be connected between BYP and ground.
7. The SYNC buffers may be used interchangeably between HSYNC and VSYNC.
8. The EMI filters at the SYNC_OUT and DDC_OUT pins (C5 to C12, and Ferrite Beads FB1 to FB4) are for reference only. The component values and filter configuration may be changed to suit the application.
9. The DDC level shifters DDC_IN, DDC_OUT, may be used interchangeably between DDCA_CLK and DDCA_DATA.
10. R1, R2 are optional. They may be used, if required, to pull the DDC_CLK and DDC_DATA lines to VCC_5V when no monitor is connected to the VGA connector. If used, it should be noted that “back current” may flow between the DDC pins and VCC_5V via these resistors when VCC_5V is powered down.
11. For optimal ESD performance with the CM2009-02, an additional clamp device (such as the CMD PACDN042) should be placed on HSYNC/VSYNC lines between the external matching resistor and the VGA connector.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

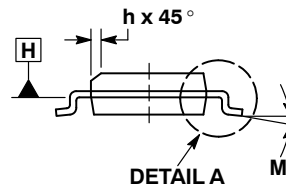
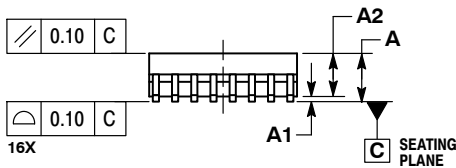
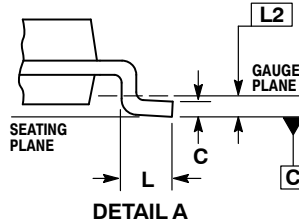
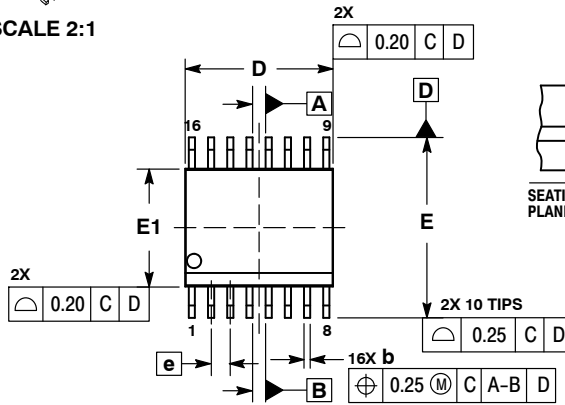
ON Semiconductor®



SCALE 2:1

QSOP16 CASE 492-01 ISSUE A

DATE 23 MAR 2011

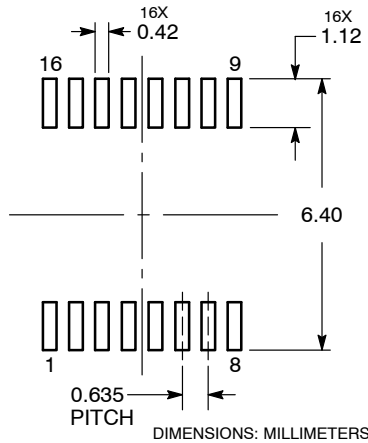


NOTES:

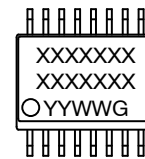
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	----	1.24	----
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.193 BSC		4.89 BSC	
E	0.237 BSC		6.00 BSC	
E1	0.154 BSC		3.90 BSC	
e	0.025 BSC		0.635 BSC	
h	0.009	0.020	0.22	0.50
L	0.016	0.050	0.40	1.27
L2	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

DOCUMENT NUMBER:	98AON04472D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	QSOP16	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View CM2009-00QR](#) on WIN SOURCE

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management