THE DATASHEET OF

2EDL23I06PJXUMA1

2EDL23x06PJ family

600 V Half Bridge Gate Driver with OCP and Integrated Bootstrap Diode

Features

- Infineon thin-film-SOI-technology
- Fully operational to +600 V
- Integrated Ultra-fast, low $R_{DS(ON)}$ Bootstrap Diode
- Floating channel designed for bootstrap operation
- Output source/sink current capability +1.8 A/-2.5 A
- Tolerant to negative transient voltage up to -100 V (Pulse width is up 300 ns) given by SOI-technology
- Interlock, Enable, Fault, and over current protection
- 10 ns typ., 60 ns max. propagation delay matching
- dV/dt immune ±50 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V and 15 V input logic compatible
- RoHS compliant

Product summary

V_{OFFSET}	= 620 V max.
$I_{O+/-}$ (typ.)	= 1.8 A/2.5 A
V_{OUT}	= 10 V - 17.5 V
Delay Matching	= 60 ns max.
t_f/t_r (typ. C_L=4.9 nF)	= 37 ns/48 ns

Package

DSO-14

Potential applications

- Motor drives, general purpose inverters
- Refrigeration compressors, home appliance
- Half-bridge and full-bridge converters in offline AC-DC power supplies for telecom and lighting

Product validation

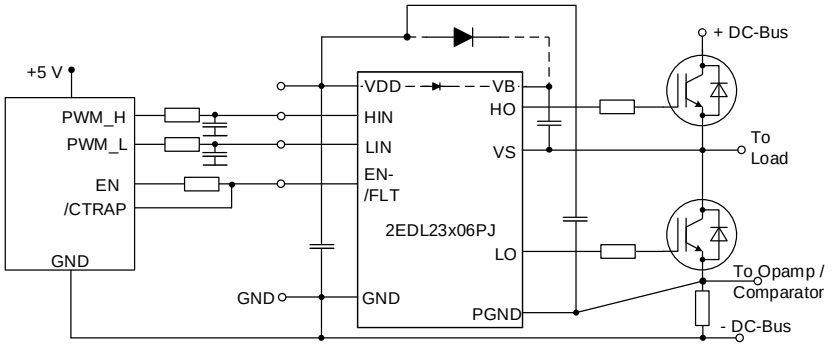
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2EDL family contains devices, which control power devices like MOS-transistors or IGBTs with a maximum blocking voltage of +600 V in half bridge configurations. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions.

The two independent driver outputs are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic which are optimised either for IGBT or MOSFET.

Those parts, which are designed for IGBT have asymmetric undervoltage lockout levels, which support strongly the integrated ultra-fast bootstrap diode. Additionally, the offline gate clamping function provides an inherent protection of the transistors for parasitic turn-on by floating gate conditions, when the IC is not supplied via VDD.



Refer to lead assignments for correct pin configuration. This diagram show electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 Typical application diagram

Ordering information

Sales Name	Special function	output current	Target transistor	typ. Level Shift UVLO thresholds	Bootstrap diode	Package	Evaluation board
2EDL23I06PJ	Deadtime, Interlock, Enable, Fault, Over Current Protection	2.3 A	IGBT	12.5 V / 11.6 V	Yes	DSO-14	EVAL-2EDL23I06PJ
2EDL23N06PJ		2.3 A	MOSFET	9.1 V / 8.3 V	Yes	DSO-14	EVAL-2EDL23N06PJ

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1 Block diagram

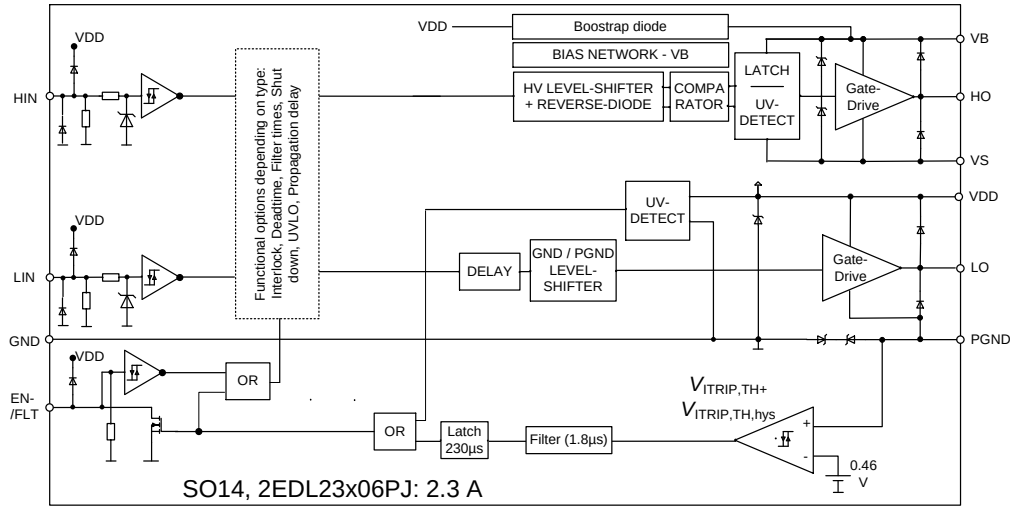


Figure 2 Functional block diagram

2 Lead definitions

Table 1 2EDL23 family lead definitions

Pin no.	Name	Function
1	VDD	Low-side and logic supply voltage
2	HIN	Logic input for high-side gate driver output (HO), in phase. Schmitt trigger inputs with hysteresis and pull down
3	LIN	Logic input for low-side gate driver output (LO), in phase. Schmitt trigger inputs with hysteresis and pull down
4	EN-/FLT	Enable input and Fault indication output
5	GND	Logic ground
6	PGND	Low-side gate drive return
7	LO	Low-side driver output
8,9,13,14	nc	Not connected
10	VS	High voltage floating supply return
11	HO	High-side driver output
12	VB	High-side gate drive floating supply

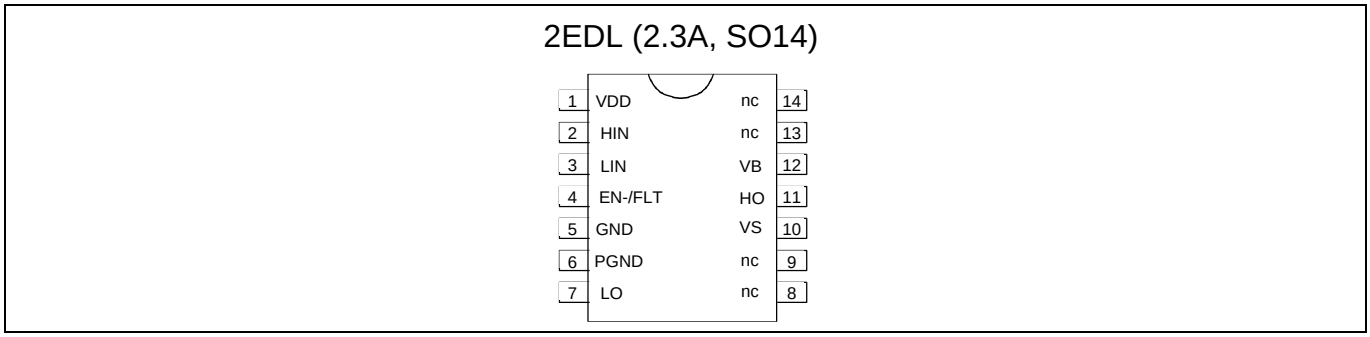


Figure 3 2EDL23 family lead assignments (top view)

3 Functional description

3.1 Low Side and High Side Control Pins (LIN, HIN)

3.1.1 Input voltage range

All input pins have the capability to process input voltages up to the supply voltage of the IC. The inputs are therefore internally clamped to VDD and GND by diodes. An internal pull-down resistor is high ohmic, so that it can keep the IC in a safe state in case of PCB crack.

3.1.2 Switching levels

The Schmitt trigger input threshold is such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. The input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4 and Figure 5. Please note, that the switching levels of the input structures remain constant even though they can accept amplitudes up to the IC supply level.

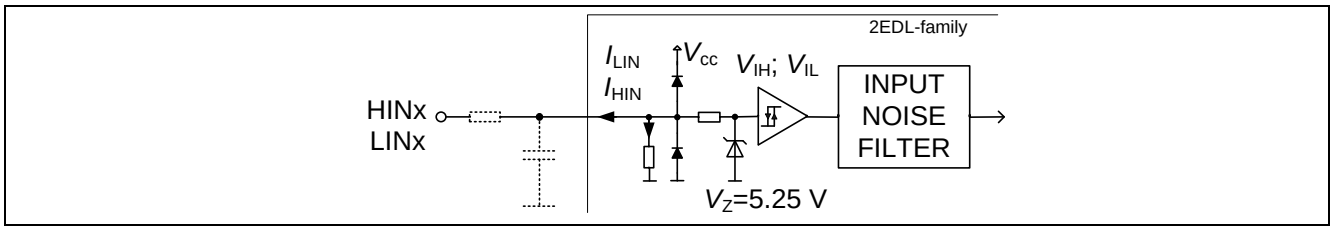


Figure 4 Input pin structure

3.1.3 Input filter time

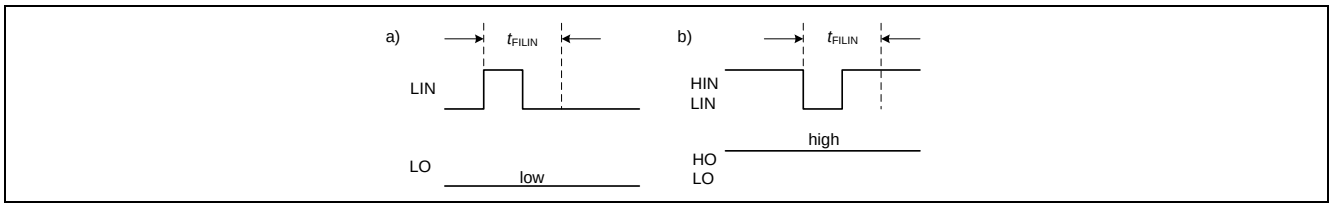


Figure 5 Input filter timing diagram

Short pulses are suppressed by means of an input filter. The MOSFET version (2EDL23N06PJ) has an input filter time of t_{FILIN} = 100 ns typ. for high side and 150 ns typ. for low side. The IGBT version (2EDL23I06PJ) has filter times of 190 ns typ.

3.2 VDD, GND and PGND (Low Side Supply)

VDD is the low side supply and it provides power to both the input logic and the low side output power stage. The input logic is referenced to GND ground as well as the under-voltage detection circuit. Output power stage is referenced to PGND ground. PGND ground is floating respect to GND ground with an absolute maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The undervoltage lockout circuit enables the device to operate at power on when a typical supply voltage higher than V_{DDUV+} is present. Please see section 3.5 “Undervoltage lockout”” for further information.

A filter time of typ. 1.5 µs[1] helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

3.3 VB and VS (High Side Supplies)

VB to VS is the high side supply voltage. The high side circuit can float with respect to GND following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VDD. A filter time of typ. 1.3 µs helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than V_{DDUV+} is present. Please see section 3.5 “Undervoltage lockout” for further information. Details on bootstrap supply section and transient immunity can be found in application note EiceDRIVER™ 2EDL family: Technical description.

3.4 LO and HO (Low and High Side Outputs)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive for IGBT and MOSFET devices. Low side output is state triggered by the respective inputs, while high side output is edge triggered by the respective inputs. In particular, after an undervoltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the high side output. In contrast, the low side outputs switch to the state of their respective inputs after an undervoltage condition of the VDD supply.

The output current specification I_{O+} and I_{O-} is defined in a way, which considers the power transistors miller voltage.This helps to design the gate drive better in terms of the application needs. Nevertheless, the devices are also characterised for the value of the pulse short circuit value I_{Opk+} and I_{Opk-}.

3.5 Undervoltage lockout (UVLO)

Two different UVLO options are required for IGBT and MOSFET. The types 2EDL23I06PJ are designed to drive IGBT. There are higher levels of undervoltage lockout for the low side UVLO than for the high side. This supports an improved start up of the IC, when bootstrapping is used. The thresholds for the low side are typically V_{DDUV+} = 12.5 V (positive going) and V_{DDUV-} = 11.6 V (negative going). The thresholds for the high side are typically V_{BSUV+} = 11.6 V (positive going) and V_{BSUV-} = 10.7 V (negative going).

The types 2EDL23N06PJ are designed to drive power MOSFET. A similar distinction for the high side and low side UVLO threshold as for IGBT is not realised here. The IC shuts down all the gate drivers power outputs, when the supply voltage is below typ. V_{DDUV-} = 8.3 V (min. / max. = 7.5 V / 9 V). The turn-on threshold is typ. V_{DDUV+} = 9.1 V (min. / max. = 8.3 V / 9.9 V)

3.6 Bootstrap diode (BSD)

An ultra fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when charging the bootstrap capacitor initially.

[1] Not subject of production test, verified by characterisation

3.7 Deadtime and interlock function

The IC provides a hardware fixed deadtime. The deadtime is different for the MOSFET type (2EDL23N06PJ) and for the IGBT type (2EDL23I06PJ). The deadtimes are particularly typ. 380 ns for IGBT and typ. 75 ns for MOSFET. An additional interlock function prevents the two outputs from being activated simultaneously.

3.8 EN-/FLT (fault indication and enable function)

The types 2EDL23x06PJ provide a pin, which can either be used to shut down the IC or to read out a failure status of the IC. The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. An integrated pull down resistor shuts down the IC in case of a floating input. The internal structure of the pin is given in Figure 6. The switching levels of the Schmitt-Trigger are here $V_{EN,TH+}$ = 2.1 V and $V_{EN,TH-}$ = 0.9 V. The typical propagation delay time is t_{EN} = 550 ns. The input is clamped by diodes to VDD and GND. The input voltage range is the same as the input control pins with a max. of 20 V.

The /FAULT function is an active low open-drain output indicating the status of the gate driver (see Figure 6). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VDD supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VDD pin description for more details). The fault signal is activate as long as UVLO is given during power up.
- Overcurrent detection (ITRIP): The fault condition is latched until the overcurrent trigger condition is finished and additional typ. 230 µs are elapsed.

The interface to the microcontroller can be realised by using an open collector / drain configured output pin for enabling the driver IC and a GPIO pin for monitoring the /FAULT. The external pull-up resistor will pull-up the voltage to +5V, when the IC is set for operation.

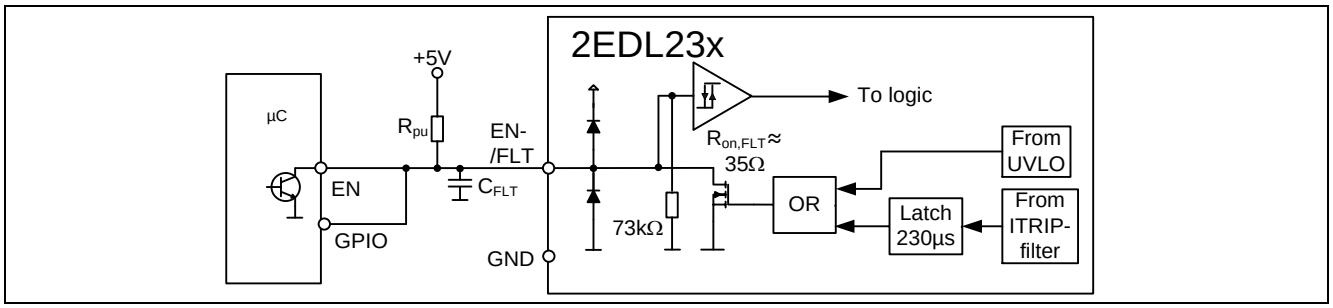


Figure 6 EN-/FLT pin structures and interface to microcontroller (µC)

3.9 Power ground / over current protection

A power ground (PGND) connects directly the emitter or source of the low side transistor with the gate drive IC. No other components, such as shunts, etc., are between this connection and the emitter or source. This enables the routing of smallest gate circuit loops and therefore smallest gate inductances.

A potential shunt resistor is between the power ground (PGND) connection and the gound connection (GND), which leads to a voltage drop between these two pins.

The voltage drop between PGND and GND can be seen sensed by means of a comparator with a threshold of $V_{th,ITRIP}$ = 0.46 V. If the voltage drop is larger than $V_{th,ITRIP}$, then the output of the comparator is triggered and the /FLT output is activated. Simultaneously, the IC shuts down both gate outputs for the period of the fault indication, which is 230 µs.

Several influences, such as reverse recovery currents, parasitic inductances and other noise sources, make the need of a signal filter necessary. The filter has a time constant of typically 1.8 µs to ensure good noise quality.

3.10 Tolerant to negative transient voltage on VS pin (-VS)

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical three phase inverter circuit is shown in Figure 7; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 8 and 9) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

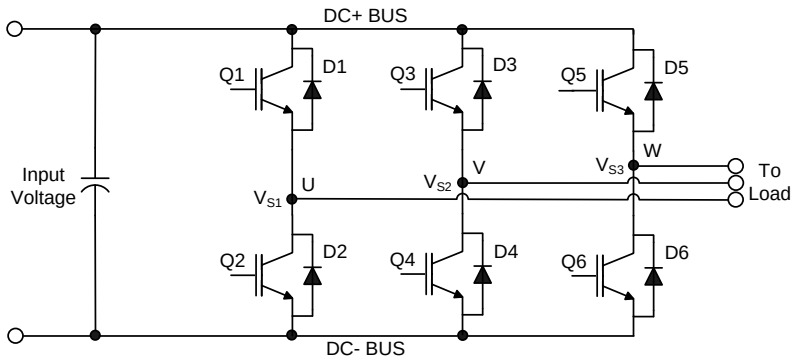


Figure 7 Three phase inverter

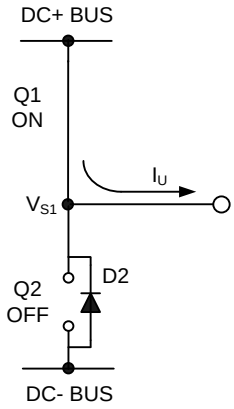


Figure 8 Q1 conducting

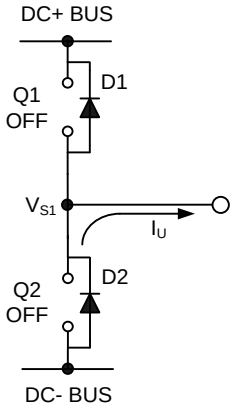


Figure 9 D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 10 and 11), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

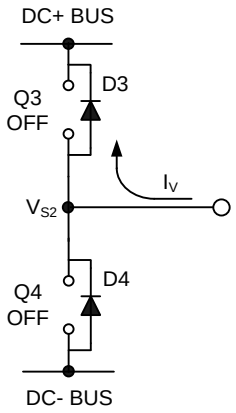


Figure 10 D3 conducting

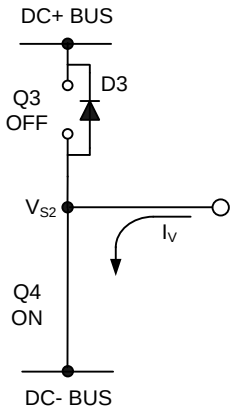


Figure 11 Q4 conducting

However, in a real inverter circuit the V_S voltage swing does not stop at the level of the negative DC bus but instead swings below the level of the negative DC bus. This undershoot voltage is called “negative transient voltage”.

The circuit shown in Figure 12 depicts one leg of the three phase inverter; Figures 13 and 14 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the VS pin).

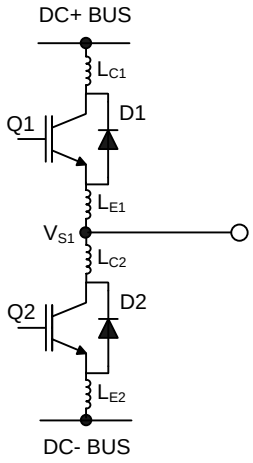


Figure 12 Parasitic Elements

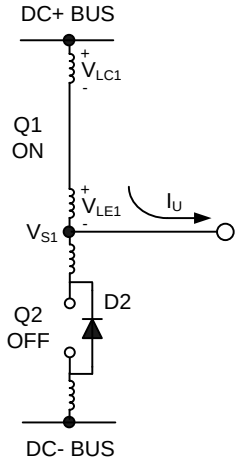


Figure 13 VS positive

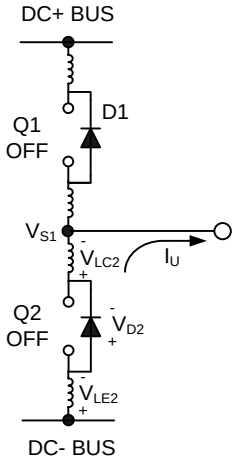


Figure 14 VS negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon’s HVICs have been designed for the robustness required in many of today’s demanding applications. An indication of the 2EDL23 family’s robustness can be seen in Figure 15, where the 2EDL23 Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative voltage spikes. A negative transient voltage falling in the grey area

(outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative VS transients fall inside the SOA.

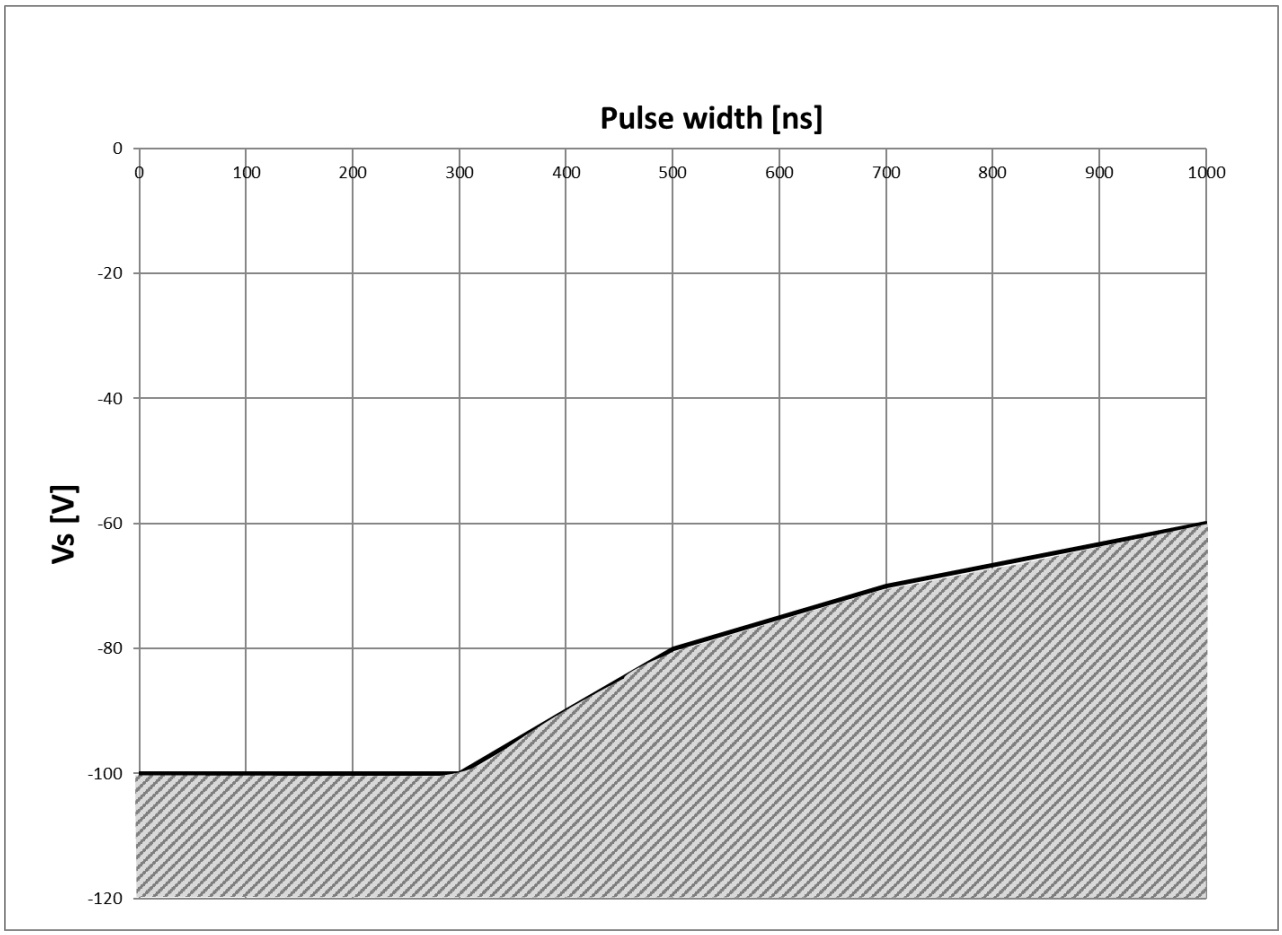


Figure 15 Negative transient voltage SOA on VS pin for 2EDL23 family @ VBS=15 V

Even though the 2EDL23 family has been shown to be able to handle these large negative transient voltage conditions, it is highly recommended that the circuit designer always limit the negative transient voltage on VS pin as much as possible by careful PCB layout and component use.

4 Electrical parameters

4.1 Absolute maximum ratings

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a=25°C).

Table 2 Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
High side offset voltage[1]	V_S	V_{DD}-V_{BS}-6	600	V
High side offset voltage (t_p<300ns)[1]		V_{DD} -V_{BS} – 100	–	
High side offset voltage [1]	V_B	V_{DD} – 6	620	
High side offset voltage (t_p<300ns)[1]		V_{DD} – 100	–	
High side floating supply voltage (V_B vs. V_S) (internally clamped)	V_{BS}	-1	20	
High side output voltage (V_{HO} vs. V_S)	V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)	V_{DD}	-1	20	
Low side supply voltage (V_{DD} vs. V_{PGND})	V_{DDPGND}	-0.5	25	
Gate driver ground	V_{PGND}	-5.7	5.7	
Low side output voltage (V_{LO} vs. V_{PGND})	V_{LO}	-0.5	V_{PGND} + 0.5	
Input voltage LIN,HIN, EN	V_{IN}	-0.5	V_{DD} + 0.5	
FAULT output voltage	V_{FLT}	-0.5	V_{DD} + 0.5	
Power dissipation (to package)[2]	P_D	–	0.9	W
Thermal resistance (junction to ambient, see section 6)	$R_{th(j-a)}$	–	134	K/W
Junction temperature[3]	T_J	–	150	°C
Storage temperature	T_S	- 40	150	
offset voltage slew rate[4]	dV_S/dt	–	50	V/ns

[1] In case V_{DD} > V_B there is an additional power dissipation in the internal bootstrap diode between pins VDD and VB in case of activated bootstrap diode. Insensitivity of bridge output to negative transient voltage up to –100V is not subject to production test – verified by design / characterization.

[2] Consistent power dissipation of all outputs. All parameters are inside operating range.

[3] Qualification stress tests cover a max. junction temperature of 150°C for 1000 h.

[4] Not subject of production test, verified by characterisation.

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a=25°C).

Table 3 Required Operation Conditions

Parameter	Symbol	Min.	Max.	Unit
High side offset voltage[1]	V_B	7	620	V
Low side supply voltage (internally clamped, V_{DD} vs. V_{PGND})	V_{DDPGND}	10	25	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a=25°C)

Table 4 Operating range

Parameter		Symbol	Min.	Max.	Unit
High side floating supply offset voltage		V_S	V_{DD} - V_{BS} -1	 500	V
High side floating supply offset voltage (V_B vs. V_{DD}, statically)		V_{BDD}	-1.0	500	
High side floating supply voltage (V_B vs. V_S)[1]	IGBT-Types	V_{BS}	13	17.5	
	MOSFET-Types		10	17.5	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	0	V_{BS}	
Low side output voltage (V_{LO} vs. V_{PGND})		V_{LO}	0	V_{DD}	
Low side supply voltage	IGBT-Types	V_{DD}	13	17.5	
	MOSFET-Types		10	17.5	
Low side ground voltage		V_{PGND}	-2.5	2.5	
Logic input voltages LIN,HIN, EN[2]		V_{IN}	0	17.5	
FAULT output voltage		V_{FLT}	0	V_{DD}	
Pulse width for ON or OFF[3]	IGBT-Types	t_{IN}	0.8	–	µs
	MOSFET-Types		0.3	–	
Ambient temperature		T_a	-40	125	°C
Thermal coefficient (junction to top, see section 6)		$\Psi_{th(j\text{-}top)}$	– –	4.8 3.3	K/W

[1] Logic operational for V_B (V_B vs. V_{GND}) > 7.0 V.

[2] All input pins (HIN, LIN, EN) are internally clamped (see abs. maximum ratings).

[3] The input pulse may not be transmitted properly in case of input pulse width at LIN and HIN below 0.8µs (IGBT types) or 0.3 µs (MOSFET) respectively.

4.4 Static logic function table

VDD	VBS	ENABLE	FAULT	PGND	LO	HO
$<V_{DDUV-}$	X	X	0	X	0	0
15V	$<V_{BSUV-}$	3.3 V	High imp.	$< V_{th,ITRIP}$	LIN	0
15V	15V	3.3 V	0	$> V_{th,ITRIP}$	0	0
15V	15V	0 V	High imp.	X	0	0
15V	15V	3.3 V	High imp.	$< V_{th,ITRIP}$	LIN	HIN

All voltages with reference to GND

4.5 Static parameters

V_{DD} = V_{BS} = 15V and V_{GND} = V_{PGND} unless otherwise specified. (T_a=25°C).

Table 5 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage LIN, HIN, EN		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage LIN, HIN, EN		V_{IL}	0.7	0.9	1.1		
High level output voltage	LO HO	V_{OH}	– –	V_{DD} -0.32 V_B -0.32	V_{DD} -0.7 V_B -0.7		I_O = - 100 mA
Low level output voltage	LO HO	V_{OL}	– –	V_{PGND}+0.18 V_S+0.18	V_{PGND}+0.4 V_S +0.4		I_O = 100 mA
V_{DD} supply undervoltage positive going threshold	IGBT-types	V_{DDUV+}	11.8	12.5	13.2		
	MOSFET types		8.3	9.1	9.9		
V_{BS} supply undervoltage positive going threshold	IGBT-types	V_{BSUV+}	10.9	11.6	12.4		
	MOSFET types		8.3	9.1	9.9		
V_{DD} supply undervoltage negative going threshold	IGBT-types	V_{DDUV-}	10.9	11.6	12.4		
	MOSFET types		7.5	8.3	9		
V_{BS} supply undervoltage negative going threshold	IGBT-types	V_{BSUV-}	10	10.7	11.7		
	MOSFET types		7.5	8.3	9		
V_{DD} and V_{BS} supply UVLO hysteresis	IGBT-types	V_{DDUVH} V_{BSUVH}	0.5	0.9	–		
	MOSFET types		0.5	0.9	–		
ITRIP comparator threshold		$V_{th,ITRIP}$	0.4	0.46	0.53		V_{ITRIP} = V_{PGND} - V_{GND}
ITRIP comparator hysteresis		$V_{th,ITRIP\ hys}$	0.045	0.07	–		
High side leakage current betw. VS and GND		I_{LVS+}	–	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and GND		I_{LVS+}[1]	–	10	–		T_J = 125 °C, V_S = 600 V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	–	180	300		HO = low depending on current types

[1] Not subject of production test, verified by characterisation

Table 5 Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Quiescent current V_{BS} supply (VB only)	I_{QBS2}	–	180	300		HO = high depending on current types
Quiescent current VDD supply (VDD only)	I_{QDD1}	–	0.34	0.8	mA	V_{LIN} = float.
Quiescent current VDD supply (VDD only)	I_{QDD2}	–	0.32	0.8		V_{LIN} = 3.3 V, V_{HIN}=0
Quiescent current VDD supply (VDD only)	I_{QDD3}	–	0.32	0.8		V_{LIN}=0 , V_{HIN}=3.3 V
Input bias current	I_{LIN+}	15	35	60	µA	V_{LIN} = 3.3 V
Input bias current	I_{LIN-}	–	0	–		V_{LIN} = 0
Input bias current	I_{HIN+}	15	35	60		V_{HIN} = 3.3 V
Input bias current	I_{HIN-}	–	0	–		V_{HIN} = 0
Input bias current (EN=high)	I_{EN+}	–	45	100		V_{ENABLE} = 3.3 V
Mean output current for load capacity charging in range from 4.5 (30%) to 7.5V (50%)	I_{O+}	1.3	1.8	–	A	C_L = 61 nF
Peak output current turn on (single pulse)	I_{Opk+}[1]	–	2.3	–		R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 7.5V (50%) to 4.5V (30%)	I_{O-}	1.65	2.5	–		C_L = 61 nF
Peak output current turn off (single pulse)	I_{Opk-}[1]	–	2.8	–		R_L = 0 Ω, t_p <10 µs
Bootstrap diode forward voltage between VDD and VB	$V_{F,BSD}$	–	0.9	1.2	V	I_F = 0.3 mA
Bootstrap diode forward current between VDD and VB	$I_{F,BSD}$	45	82	–	mA	$V_{DD} - V_B$ = 4 V
Bootstrap diode resistance	R_{BSD}	15	27	40	Ω	V_{F1} = 4 V, V_{F2} = 5 V
EN-/FLT low on resistance of the pull down transistor	$R_{on,FLT}$	–	35	70		$V_{EN-/FLT}$ = 0.5 V

[1] Not subject of production test, verified by characterisation

4.6 Dynamic parameters

V_{DD} = V_{BS} = 15 V, V_S = V_{GND} = V_{PGND}, C_L = 180 pF unless otherwise specified. (T_a=25°C).

Table 6 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay	IGBT types	t_{on}	280	420	610	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
	MOSFET types		210	310	460		
Turn-off propagation delay	IGBT types	t_{off}	260	400	590		
	MOSFET types		200	300	440		
Turn-on rise time		t_r	–	48	80		$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 4.9 nF
Turn-off fall time		t_f	–	37	60		
Shutdown propagation delay ENABLE		t_{EN}	–	550	850		V_{EN}=0.5 V, V_{LO} / V_{HO} = 20%
Input filter time at LIN/HIN for turn on and off	IGBT types	t_{FILIN}	120	190	320		$V_{LIN/HIN}$ = 0 & 3.3 V
	MOSFET types HIN LIN		 50 100	 100 150	 170 250		
Input filter time EN		t_{FILEN}	200	400	–		
ITRIP filter time		$t_{FILITRIP}$	1.0	1.8	2.7	µs	V_{PGND} = 1 V, /FLT=0
Shut down propoagation delay PGND to any output		t_{ITRIP}	1.1	2.2	3.0		V_{PGND} = 1 V V_{LO} / V_{HO} = 3V
Propagation delay ITRIP to FAULT		t_{FLT}	1.0	2.1	2.9		V_{PGND} = 1 V, /FLT=0.5 V
Fault-clear time		t_{FLTCLR}	70	230	–		V_{PGND} = 0.1 V, /FLT=2.1 V
Dead time	IGBT types	DT	260	380	540	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
	MOSFET types		30	75	140		
Dead time matching abs(DT_LH – DT_HL) for single IC	IGBT types	MDT	–	10	80		ext. dead time 0ns
	MOSFET types			10	50		
Matching delay ON, abs(ton_HS - ton_LS)		MT_{ON}	–	10	60		external dead time > 500 ns
Matching delay OFF, abs(toff_HS-toff_LS)		MT_{OFF}	–	10	60		external dead time >500 ns
Output pulse width matching. PW_{in}-PW_{out}	IGBT types	PM	–	20	80		PW_{in} > 1 µs
	MOSFET types		–	20	70		

5 Timing diagrams

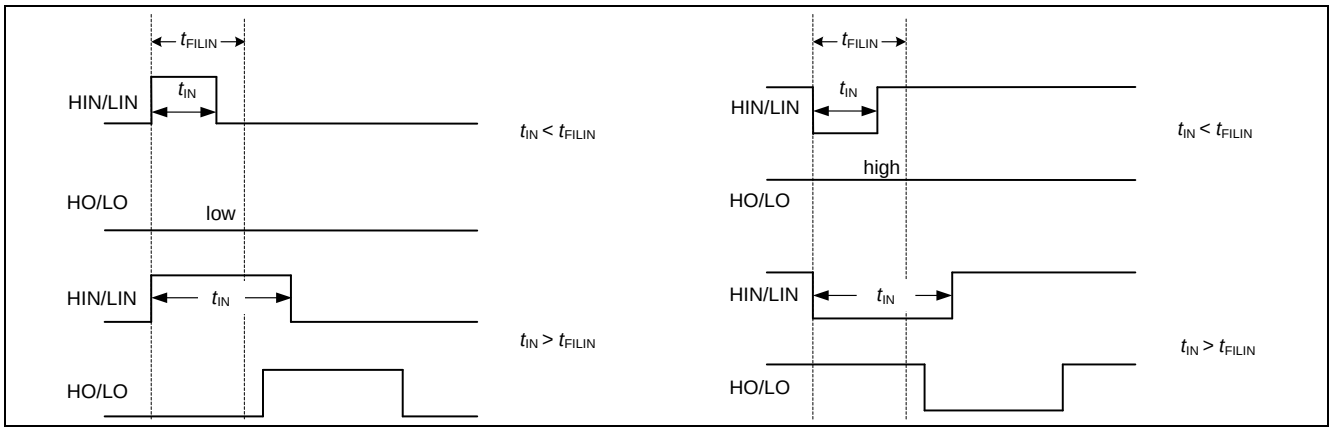


Figure 16 Timing of short pulse suppression

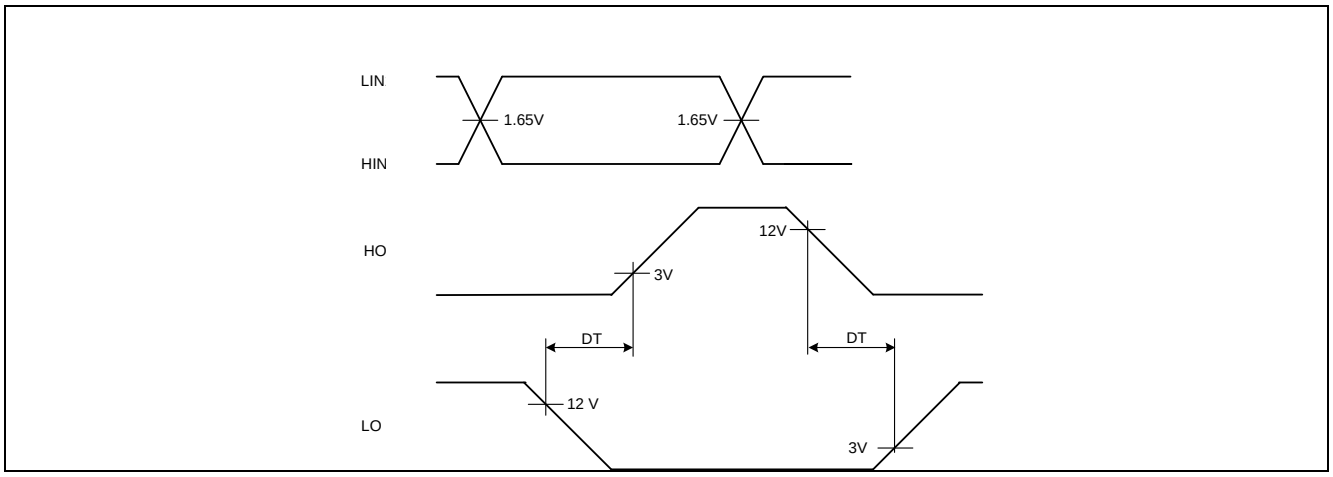


Figure 17 Timing of of internal deadtime

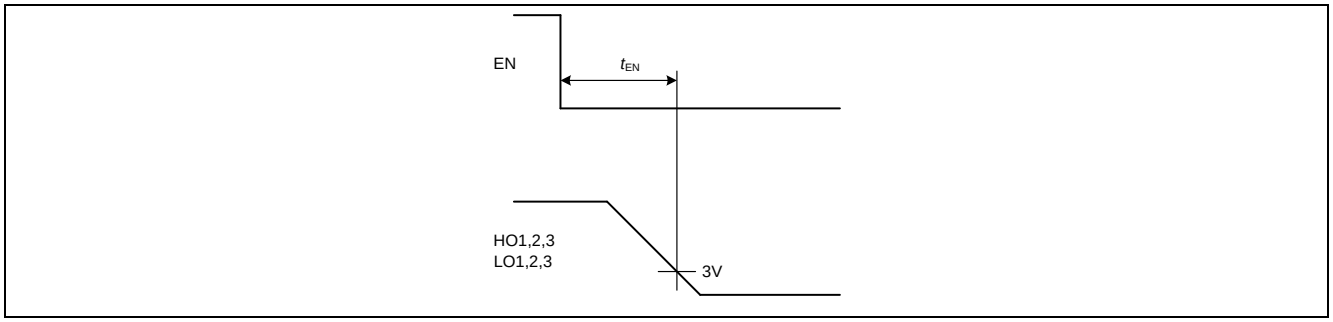


Figure 18 Timing of of internal deadtime

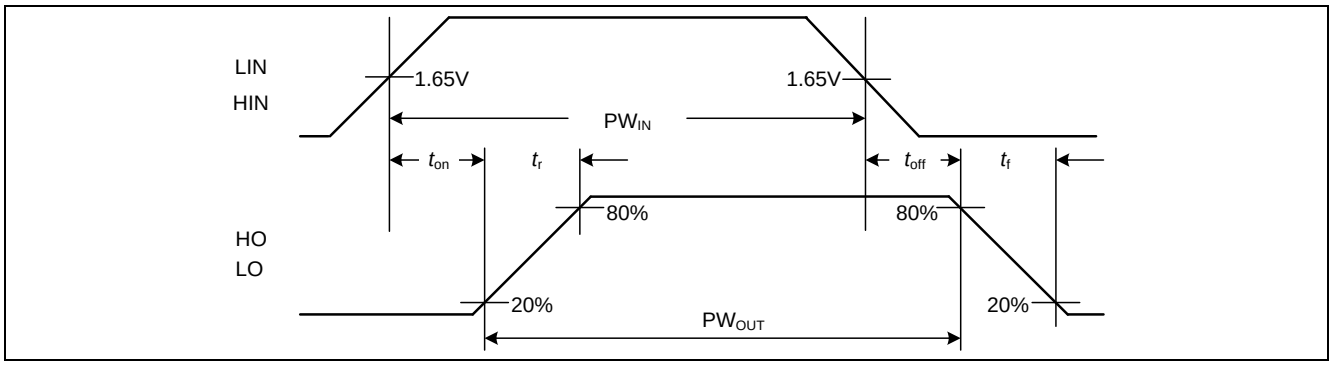


Figure 19 Input to output propagation delay times and switching times definition

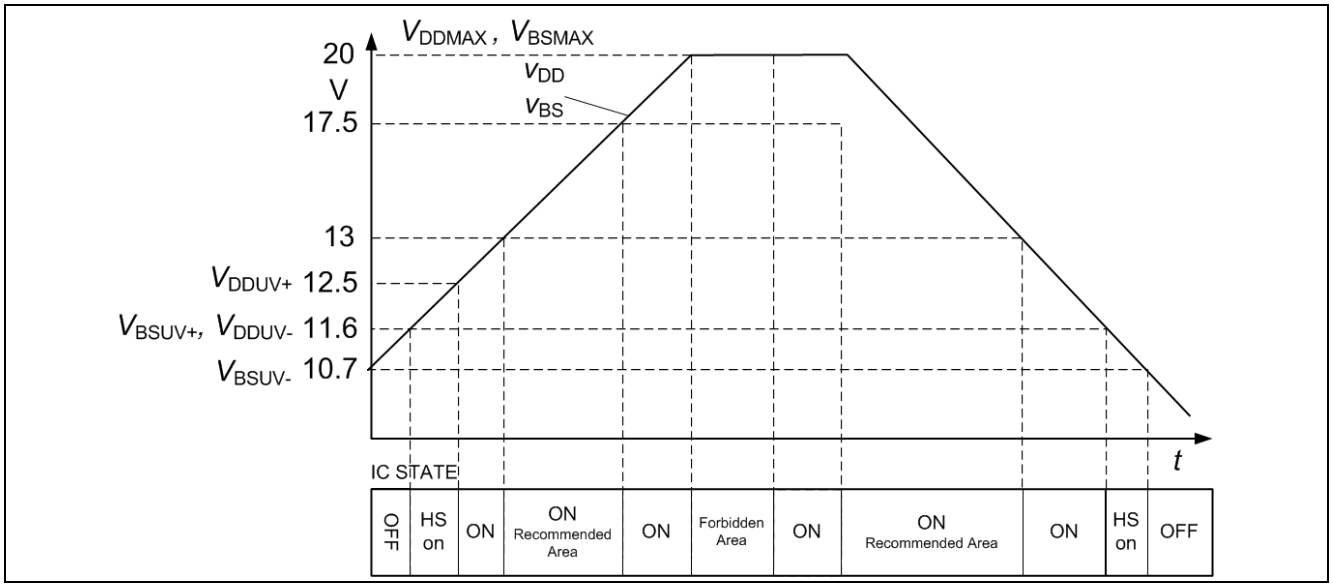


Figure 20 Operating areas (IGBT UVLO levels)

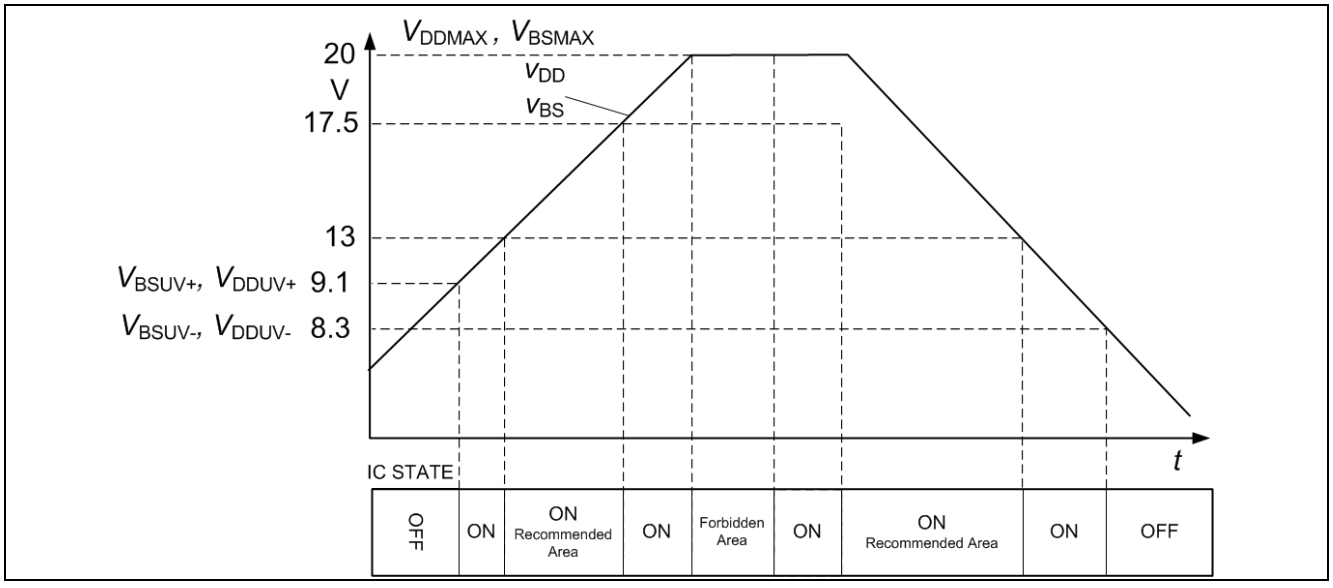


Figure 21 Operating areas (MOSFET UVLO levels)

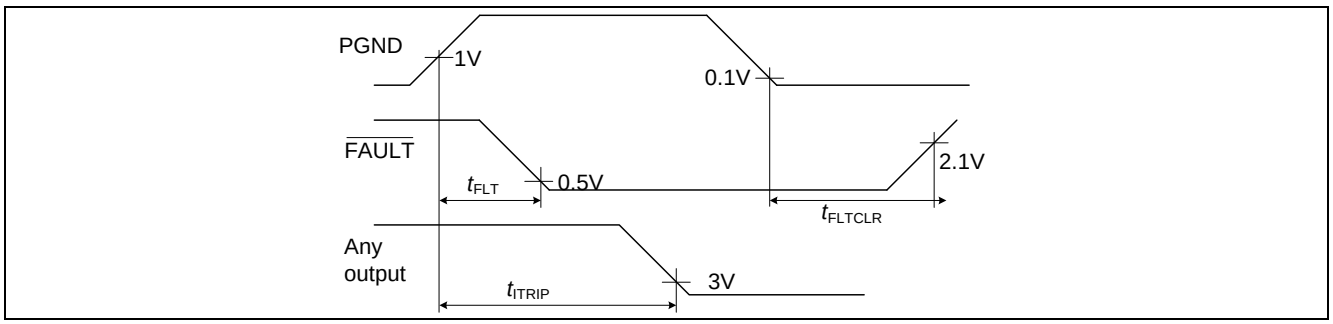


Figure 22 ITRIP-Timing

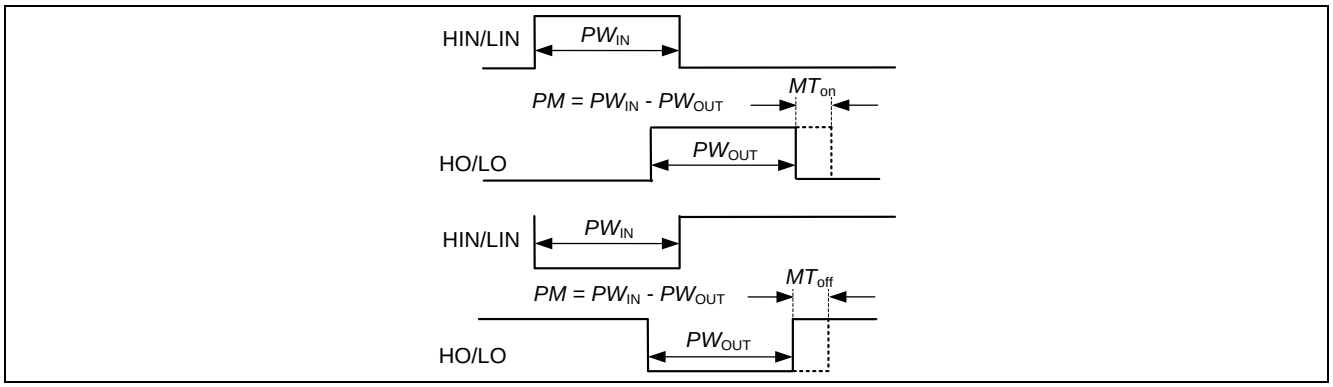


Figure 23 Output pulse width timing and matching delay timing diagram for positive logic

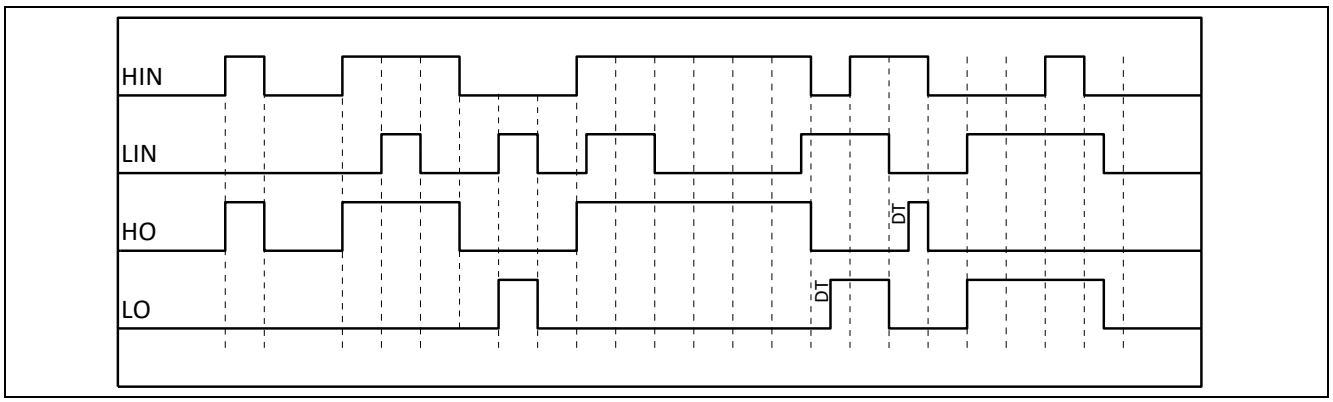
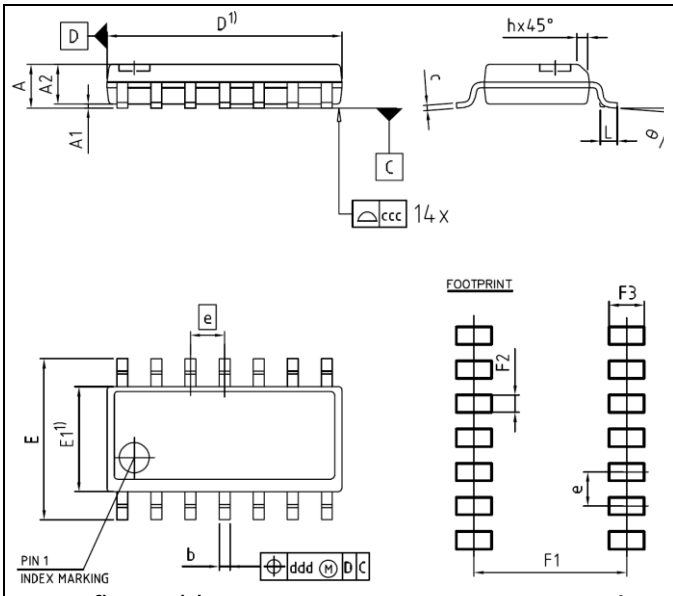


Figure 24 Deadtime and interlock

6 Package information



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	-	0.049	-
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
N	14		14	
L	0.39	0.89	0.015	0.035
h	0.25	0.50	0.010	0.020
Θ	0°	8°	0°	8°
ccc	0.10		0.004	
ddd	0.20		0.008	
F1	5.69		0.224	
F2	0.65		0.026	
F3	1.31		0.052	

Max. reflow solder temperature: 265°C acc. JEDEC
Max. wave solder temperature: 245°C acc. JEDEC

Figure 25 Package outline PG-DSO-14

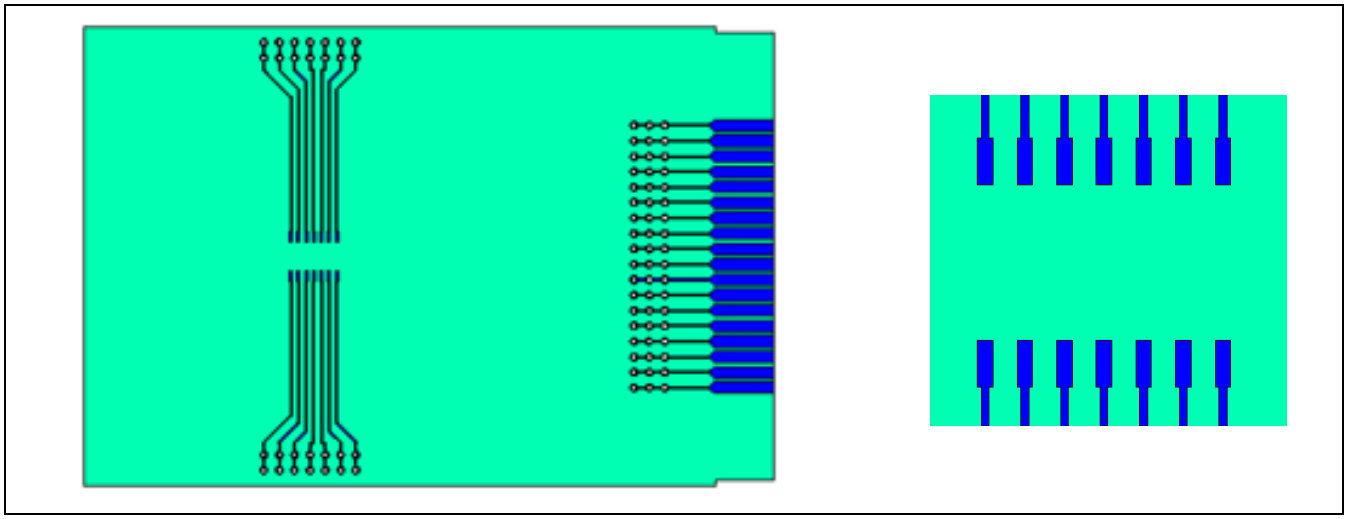


Figure 26 PCB reference layout (according to JEDEC 1s0P)
left: Reference layout
right: detail of footprint

The thermal coefficient is used to calculate the junction temperature, when the IC surface temperature is measured. The junction temperature is

$$T_j = \Psi_{th(j\text{-}top)} \cdot P_d + T_{top}$$

Table 7 Data of reference layout

Dimensions	Material	Metal (Copper)
76.2 × 114.3 × 1.5 mm³	FR4 (λ_{therm} = 0.3 W/mK)	70µm (λ_{therm} = 388 W/mK)

7 Qualification information[1]

Table 8 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-8/-14	MSL3[3], 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (> 1.0 kV) (per JESD22-C101)	
	Human body model	Class 2 (per JEDEC standard JESD22-A114)	
IC latch-up test		Class II Level A (per JESD78)	
RoHS compliant		Yes	

8 Related products

Table 9

Product	Description
Gate Driver ICs	
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, Fault reporting, and Enable for MOSFET or IGBT switches.
2EDL05I06 / 2EDL05N06	600 V, Half-bridge thin-film SOI level shift gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diode, 0.36/0.7 A source/sink current driver, 8pins/14pins package, for MOSFET or IGBT switches.
Power Switches	
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS™ CFD2 with integrated fast body diode in DPAK
IPN50R950CE	500 V CoolMOS™ CE Superjunction MOSFET in PG-SOT223 package
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
[3] Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

Revision history

Document version	Date of release	Description of changes
0.86	2014-05-15	Change term VCC in VDD
2.2	2016-06-01	Update maximum Ta from 95°C to 105°C in Table 3
2.3	2016-08-18	Updated disclaimer, trademarks. Upated parameter V_{HO}
2.4	2017-11-28	$\Psi_{th(j\text{-}top)}$ change to junction to top
2.5	2018-11-20	Updated ESD HBM information
2.6	2019-01-25	Updated Charpter 3.10 Tolerant to negative transient voltage on VS pin
2.7	2020-07-07	IC latch-up test per JESD78
2.8	2021-07-19	Modified ambient temperature max. rating in Table 4 on page 11
2.9	2022-05-12	Remove $I_{F,BSD}$ maximum spec

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