



**THE DATASHEET OF  
CM1213-08MR**



# CM1213

## 6 and 8-Channel Low Capacitance ESD Protection Arrays

### Product Description

The CM1213 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive ( $V_P$ ) or negative ( $V_N$ ) supply rail. A Zener diode is embedded between  $V_P$  and  $V_N$ , offering two advantages. First, it protects the  $V_{CC}$  rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213 will protect against ESD pulses up to  $\pm 8$  kV per the IEC 61000-4-2 standard.

These devices are particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire<sup>®</sup>, iLink<sup>™</sup>), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

### Features

- 6 or 8 Channels of ESD Protection  
Note: For 1, 2, and 4 Channel Devices, See the CM1213A Datasheet
- Provides ESD Protection to IEC61000-4-2 Level 4
  - $\pm 8$  kV Contact Discharge
- Low Channel Input Capacitance of 1.0 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Channel Input Capacitance Matching of 0.02 pF Typical is Ideal for Differential Signals
- Mutual Capacitance between Signal Pin and Adjacent Signal Pin -0.11 pF Typical
- Zener Diode Protects Supply Rail and Eliminates the Need for External By-pass Capacitors
- Each I/O Pin Can Withstand Over 1000 ESD Strikes\*
- Available in SOIC and MSOP
- These Devices are Pb-Free and are RoHS Compliant

### Applications

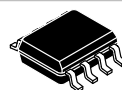
- USB2.0 Ports at 480 Mbps in Desktop PCs, Notebooks and Peripherals
- IEEE1394 Firewire<sup>®</sup> Ports at 400 Mbps / 800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-speed Data Line ESD Protection
- Handheld PCs/PDAs

\*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to  $\pm 8$  kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

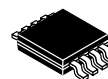


ON Semiconductor<sup>®</sup>

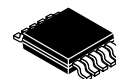
<http://onsemi.com>



SOIC-8  
SM SUFFIX  
CASE 751AC

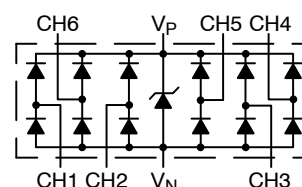


MSOP-8  
MR SUFFIX  
CASE 846AD

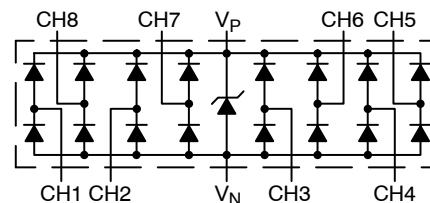


MSOP-10  
MR SUFFIX  
CASE 846AE

### BLOCK DIAGRAMS



CM1213-06SM  
CM1213-06MR



CM1213-08MR

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
CM1213-06SM	SOIC-8 (Pb-Free)	2500/Tape & Reel
CM1213-06MR	MSOP-8 (Pb-Free)	4000/Tape & Reel
CM1213-08MR	MSOP-10 (Pb-Free)	4000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

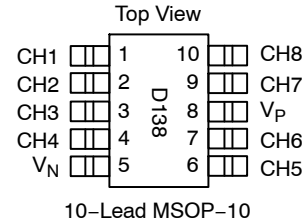
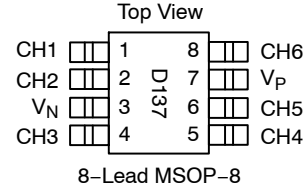
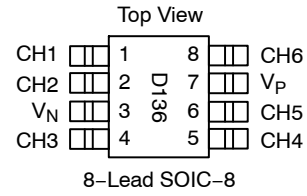
# CM1213

**Table 1. PIN DESCRIPTIONS**

6-Channel, 8-Lead MSOP-8/SOIC-8 Packages			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	V <sub>N</sub>	GND	Negative voltage supply rail
4	CH3	I/O	ESD Channel
5	CH4	I/O	ESD Channel
6	CH5	I/O	ESD Channel
7	V <sub>P</sub>	PWR	Positive voltage supply rail
8	CH6	I/O	ESD Channel

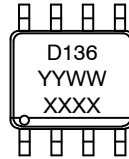
8-Channel, 10-Lead MSOP-10 Package			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V <sub>N</sub>	GND	Negative voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V <sub>P</sub>	PWR	Positive voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

## PACKAGE / PINOUT DIAGRAMS

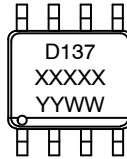


## GENERIC MARKING DIAGRAMS

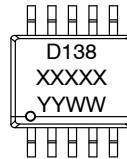
CM1213-06SM



CM1213-06MR



CM1213-08MR



XXXXX = Lot Number  
 YY = Year  
 WW = Work Week

# CM1213

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
Operating Supply Voltage ( $V_P - V_N$ )	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_N - 0.5)$ to $(V_P + 0.5)$	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C
Package Power Rating MSOP-8 Package (CM1213-06MR) MSOP-10 Package (CM1213-08MR) SOIC-8 Package (CM1213-06SM)	400 400 600	mW

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_P$	Operating Supply Voltage ( $V_P - V_N$ )			3.3	5.5	V
$I_P$	Operating Supply Current	$(V_P - V_N) = 3.3$ V			8.0	μA
$V_F$	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 8$ mA; $T_A = 25^\circ\text{C}$	0.60 0.60	0.80 0.80	0.95 0.95	V
$I_{LEAK}$	Channel Leakage Current	$T_A = 25^\circ\text{C}$ ; $V_P = 5$ V, $V_N = 0$ V		±0.1	±1.0	μA
$C_{IN}$	Channel Input Capacitance	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V		1.0	1.5	pF
$\Delta C_{IN}$	Channel Input Capacitance Matching	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V		0.02		pF
$C_{MUTUAL}$	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V		0.11		pF
$V_{ESD}$	ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard	$T_A = 25^\circ\text{C}$ (Notes 3 and 4)	±8			kV
$V_{CL}$	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$ , $I_{PP} = 1$ A, $t_P = 8/20$ μS (Note 4)		+8.8 -1.4		V
$R_{DYN}$	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1$ A, $t_P = 8/20$ μS Any I/O pin to Ground (Note 4)		0.7 0.4		Ω

1. All parameters specified at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.
2. Human Body Model per MIL-STD-883, Method 3015,  $C_{Discharge} = 100$  pF,  $R_{Discharge} = 1.5$  KΩ,  $V_P = 3.3$  V,  $V_N$  grounded.
3. Standard IEC 61000-4-2 with  $C_{Discharge} = 150$  pF,  $R_{Discharge} = 330$  Ω,  $V_P = 3.3$  V,  $V_N$  grounded.
4. These measurements performed with no external capacitor on  $V_P$  ( $V_P$  floating).

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

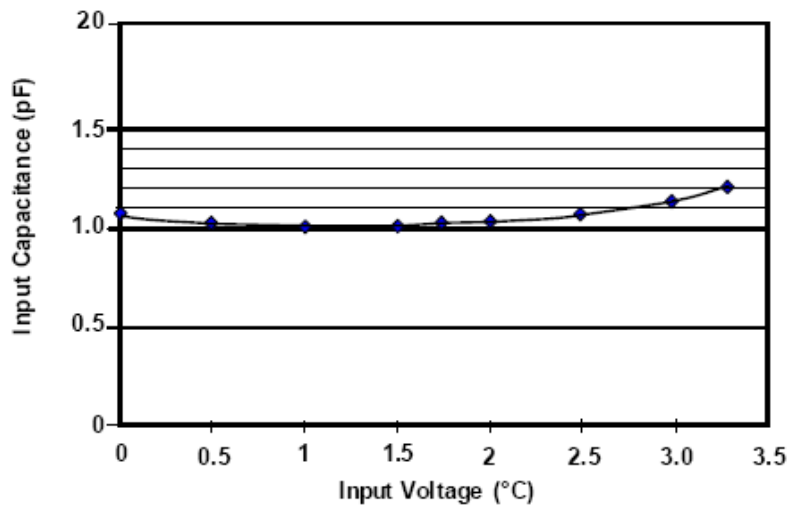


Figure 1. Typical Variation of  $C_{IN}$  vs.  $V_{IN}$   
 ( $f = 1 \text{ MHz}$ ,  $V_P = 3.3 \text{ V}$ ,  $V_N = 0 \text{ V}$ ,  $0.1 \mu\text{F}$  Chip Capacitor between  $V_P$  and  $V_N$ ,  $25^\circ\text{C}$ )

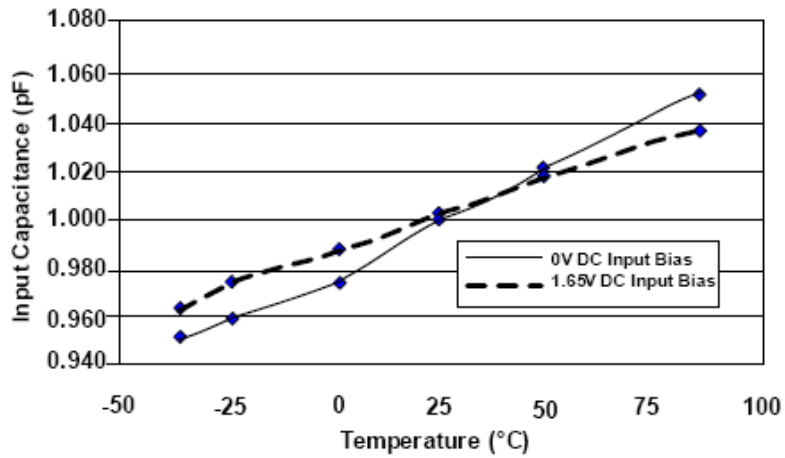


Figure 2. Typical Variation of  $C_{IN}$  vs. Temp  
 ( $f = 1 \text{ MHz}$ ,  $V_{IN} = 30 \text{ mV}$ ,  $V_P = 3.3 \text{ V}$ ,  $V_N = 0 \text{ V}$ ,  $0.1 \mu\text{F}$  Chip Capacitor between  $V_P$  and  $V_N$ )

# CM1213

## PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (Nominal Conditions unless Specified Otherwise, 50 Ohm Environment)

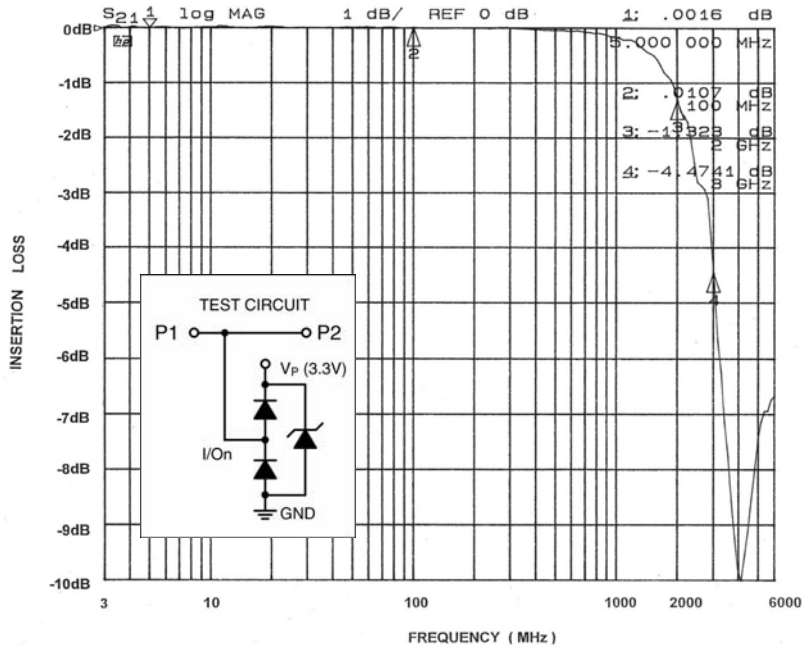


Figure 3. Insertion Loss (S21) vs. Frequency (0 V DC Bias,  $V_P=3.3$  V)

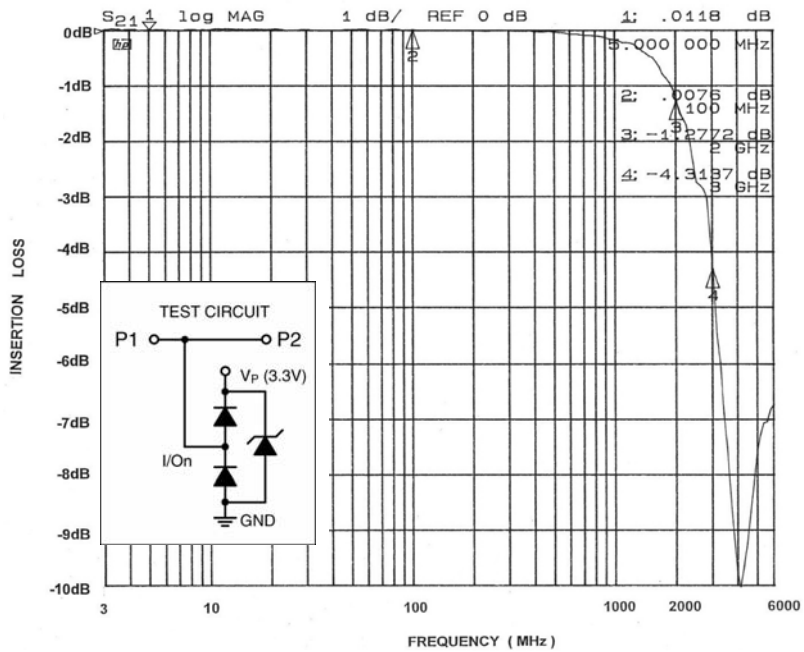


Figure 4. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias,  $V_P=3.3$  V)

APPLICATION INFORMATION

**Design Considerations**

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to power supply is represented by  $L_1$  and  $L_2$ . The voltage  $V_{CL}$  on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{\text{SUPPLY}} + L_1 \times d(I_{\text{ESD}}) / dt + L_2 \times d(I_{\text{ESD}}) / dt$$

where  $I_{\text{ESD}}$  is the ESD current pulse, and  $V_{\text{SUPPLY}}$  is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here  $d(I_{\text{ESD}})/dt$  can be approximated by  $\Delta I_{\text{ESD}}/\Delta t$ , or  $30/(1 \times 10^{-9})$ . So just 10 nH of series inductance ( $L_1$  and  $L_2$  combined) will lead to a 300 V increment in  $V_{CL}$ !

Similarly for negative ESD pulses, parasitic series inductance from the  $V_N$  pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213 has an integrated Zener diode between  $V_P$  and  $V_N$ . This greatly reduces the effect of supply rail inductance  $L_2$  on  $V_{CL}$  by clamping  $V_P$  at the breakdown voltage of the Zener diode. However, for the lowest possible  $V_{CL}$ , especially when  $V_P$  is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22  $\mu\text{F}$  ceramic chip capacitor be connected between  $V_P$  and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the  $V_P$  pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

**Additional Information**

See also ON Semiconductor Application Note, "Design Considerations for ESD Protection", in the Applications section.

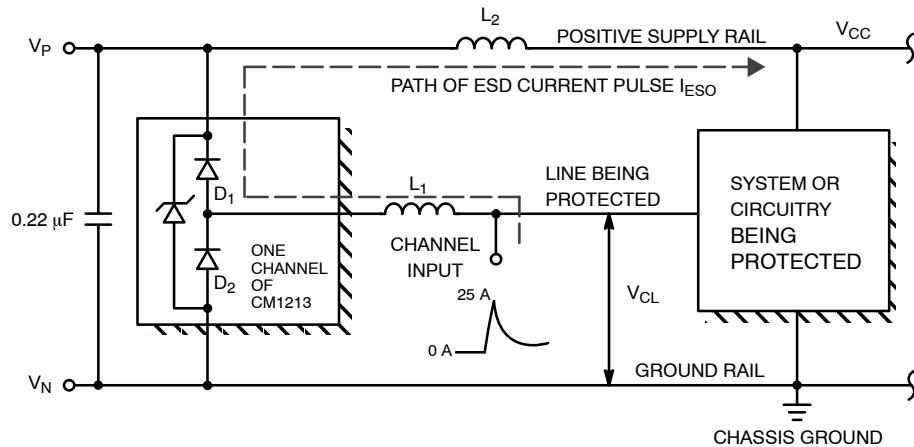
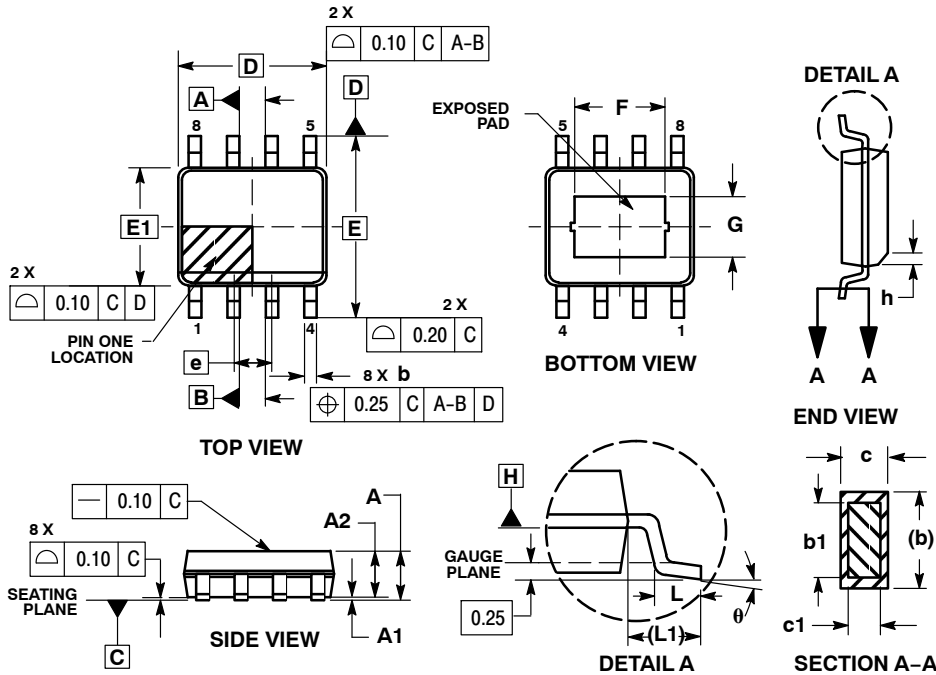


Figure 5. Application of Positive ESD Pulse between Input Channel and Ground

# CM1213

## PACKAGE DIMENSIONS

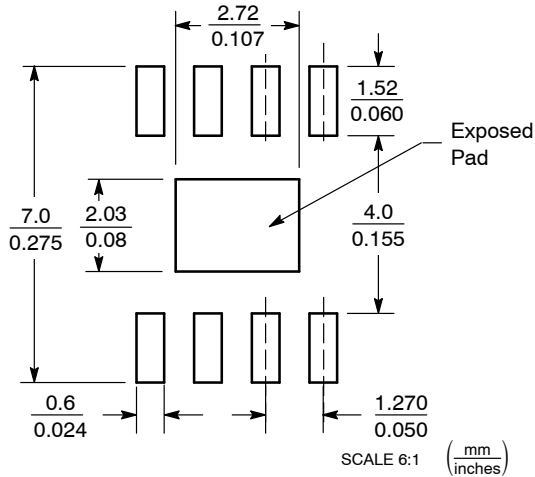
SOIC-8 EP  
CASE 751AC  
ISSUE B



**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

**SOLDERING FOOTPRINT\***

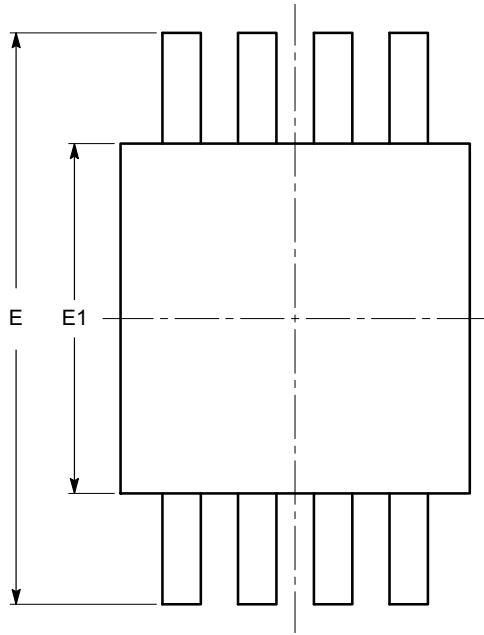


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# CM1213

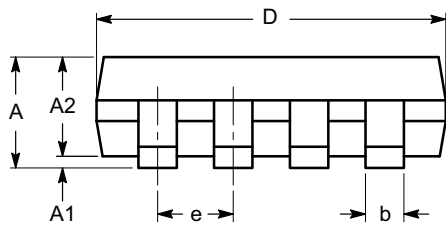
## PACKAGE DIMENSIONS

MSOP 8, 3x3  
CASE 846AD  
ISSUE O

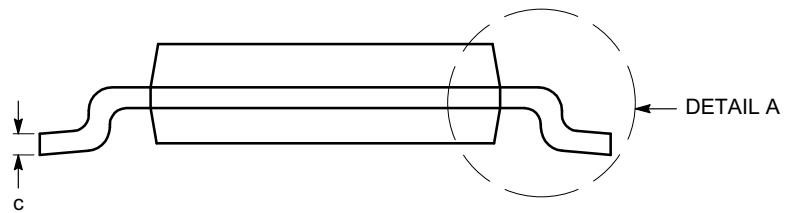


TOP VIEW

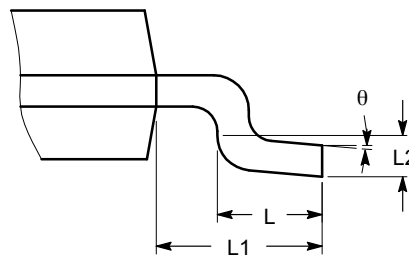
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
$\theta$	0°		6°



SIDE VIEW



END VIEW



DETAIL A

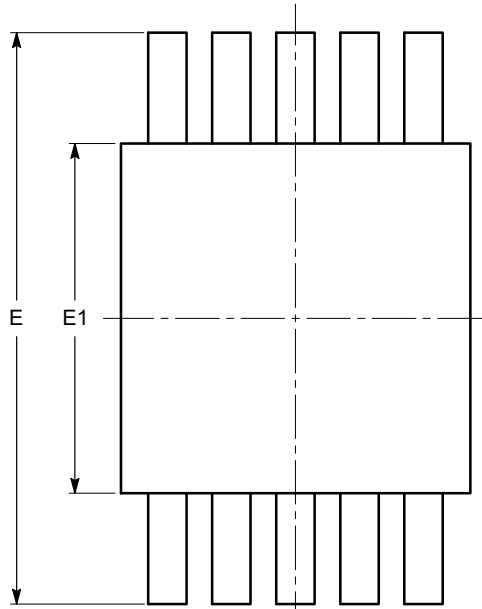
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

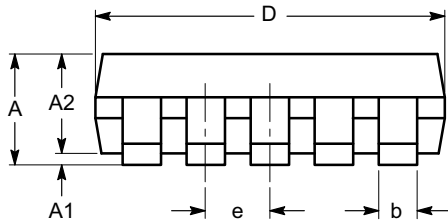
# CM1213

## PACKAGE DIMENSIONS

MSOP 10, 3x3  
CASE 846AE  
ISSUE O

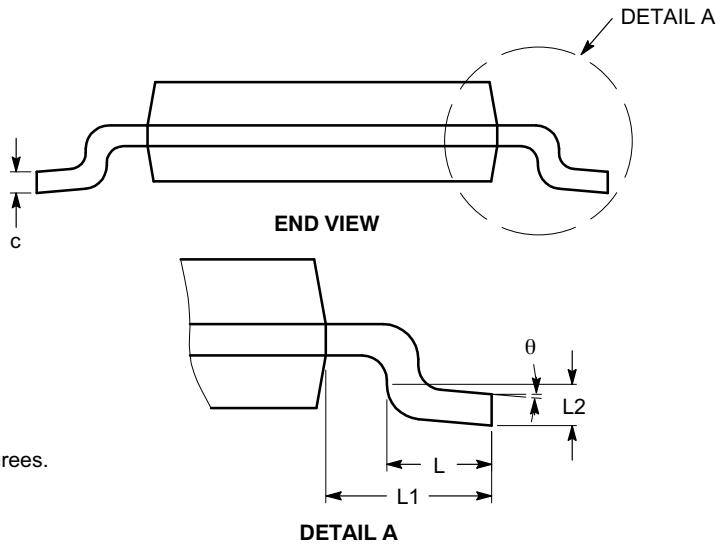


TOP VIEW



SIDE VIEW


SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17		0.27
c	0.13		0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
$\theta$	0°		8°



**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

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