



# 16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: [SN74LVCH16T245-EP](#)

## FEATURES

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, All Outputs Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}/125^{\circ}\text{C}$ ) Temperature Range <sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

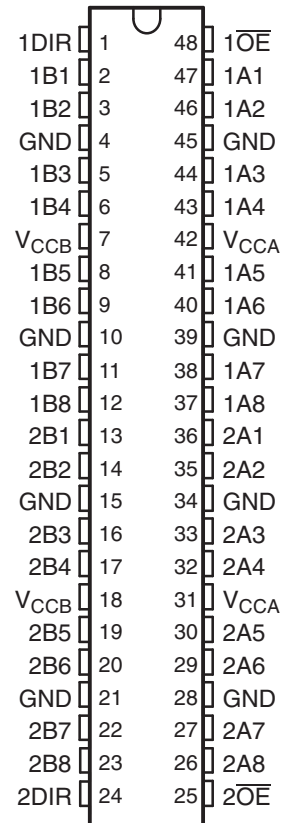
(1) Custom temperature ranges available

## DESCRIPTION

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVCH16T245 is designed so that the control pins (1DIR, 2DIR,  $\overline{1OE}$ , and  $\overline{2OE}$ ) are supplied by  $V_{CCA}$ .

DGV PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**DESCRIPTION (CONTINUED)**

The SN74LVCH16T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, then all outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-50°C to 125°C	TVSOP – DGV	Tape and reel	CLVCH16T245MDGVREP	LDHT245MEP
	TSSOP - DGG	Tape and reel	CLVCH16T245MDGGREP	8UT245MEP

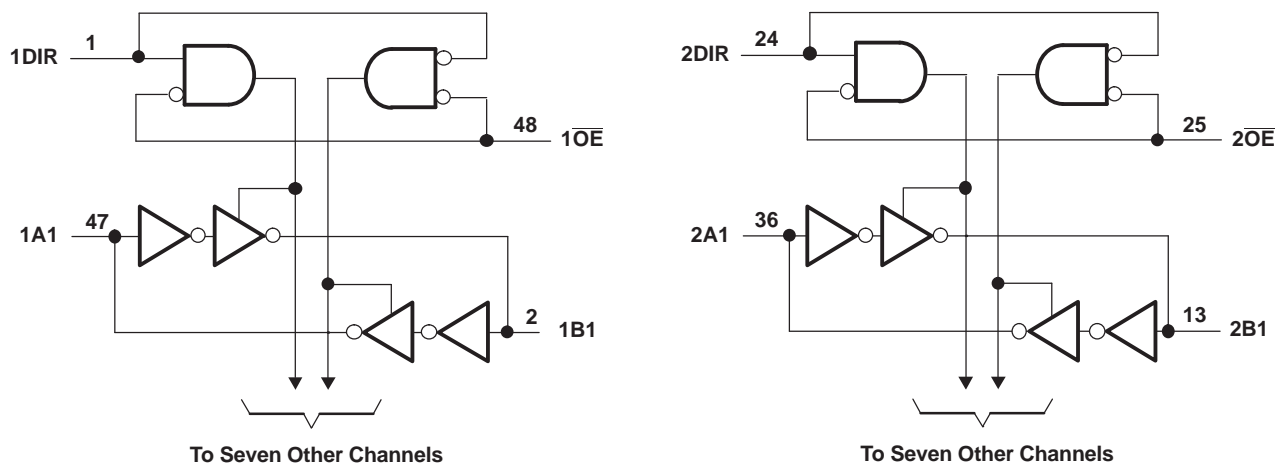
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE<sup>(1)</sup>  
(EACH 16-BIT SECTION)**

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
$V_{CCA}$ $V_{CCB}$	Supply voltage range		-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	I/O ports (A port)	-0.5	6.5	V
		I/O ports (B port)	-0.5	6.5	
		Control inputs	-0.5	6.5	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	-0.5	6.5	V
		B port	-0.5	6.5	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through each $V_{CCA}$ , $V_{CCB}$ , and GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>			58	°C/W
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions**<sup>(1) (2) (3)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.65	5.5	V
V <sub>CCB</sub>					1.65	5.5	
V <sub>IH</sub>	High-level input voltage	Data inputs <sup>(4)</sup>	1.65 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V <sub>CCI</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(4)</sup>	1.65 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			2.3 V to 2.7 V		0.7		
			3 V to 3.6 V		0.8		
			4.5 V to 5.5 V		V <sub>CCI</sub> × 0.3		
V <sub>IH</sub>	High-level input voltage	Control inputs (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.65 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V <sub>CCA</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	Control inputs (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.65 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			2.3 V to 2.7 V		0.7		
			3 V to 3.6 V		0.8		
			4.5 V to 5.5 V		V <sub>CCA</sub> × 0.3		
V <sub>I</sub>	Input voltage	Control inputs			0	5.5	V
V <sub>I/O</sub>	Input/output voltage	Active state			0	V <sub>CCO</sub>	V
		3-State			0	5.5	
I <sub>OH</sub>	High-level output current		1.65 V to 1.95 V		-4		mA
			2.3 V to 2.7 V		-8		
			3 V to 3.6 V		-24		
			4.5 V to 5.5 V		-32		
I <sub>OL</sub>	Low-level output current		1.65 V to 1.95 V		4		mA
			2.3 V to 2.7 V		8		
			3 V to 3.6 V		24		
			4.5 V to 5.5 V		32		
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V		20		ns/V
			2.3 V to 2.7 V		20		
			3 V to 3.6 V		10		
			4.5 V to 5.5 V		5		
T <sub>A</sub>	Operating free-air temperature				-40	85	°C

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.

(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(3) All unused control inputs of the device must be held at V<sub>CCA</sub> GND to ensure proper device operation and minimize power consumption. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V.

(5) For V<sub>CCA</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V.

**Electrical Characteristics<sup>(1) (2)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNIT						
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA, V <sub>I</sub> = V <sub>IH</sub>		1.65 V to 4.5 V	1.65 V to 4.5 V				V <sub>CCO</sub> - 0.1		V						
	I <sub>OH</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>		1.65 V	1.65 V				1.2								
	I <sub>OH</sub> = -8 mA, V <sub>I</sub> = V <sub>IH</sub>		2.3 V	2.3 V				1.9								
	I <sub>OH</sub> = -24 mA, V <sub>I</sub> = V <sub>IH</sub>		3 V	3 V				2.4								
	I <sub>OH</sub> = -32 mA, V <sub>I</sub> = V <sub>IH</sub>		4.5 V	4.5 V				3.8								
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA, V <sub>I</sub> = V <sub>IL</sub>		1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V						
	I <sub>OL</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>		1.65 V	1.65 V					0.45							
	I <sub>OL</sub> = 8 mA, V <sub>I</sub> = V <sub>IL</sub>		2.3 V	2.3 V					0.3							
	I <sub>OL</sub> = 24 mA, V <sub>I</sub> = V <sub>IL</sub>		3 V	3 V					0.55							
	I <sub>OL</sub> = 32 mA, V <sub>I</sub> = V <sub>IL</sub>		4.5 V	4.5 V					0.55							
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.65 V to 5.5 V	1.65 V to 5.5 V	±0.5		±1		±2	μA						
I <sub>BHL</sub> <sup>(3)</sup>	V <sub>I</sub> = 0.58 V		1.65 V	1.65 V					15	μA						
	V <sub>I</sub> = 0.7 V		2.3 V	2.3 V					45							
	V <sub>I</sub> = 0.8 V		3 V	3 V					75							
	V <sub>I</sub> = 0.1.35 V		4.5 V	4.5 V					100							
I <sub>BHH</sub> <sup>(4)</sup>	V <sub>I</sub> = 1.07 V		1.65 V	1.65 V					-15	μA						
	V <sub>I</sub> = 1.7 V		2.3 V	2.3 V					-45							
	V <sub>I</sub> = 2 V		3 V	3 V					-75							
	V <sub>I</sub> = 3.15 V		4.5 V	4.5 V					-100							
I <sub>BHLO</sub> <sup>(5)</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.95 V	1.95 V					200	μA						
			2.7 V	2.7 V					300							
			3.6 V	3.6 V					500							
			5.5 V	5.5 V					900							
I <sub>BHHO</sub> <sup>(6)</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.95 V	1.95 V					-200	μA						
			2.7 V	2.7 V					-300							
			3.6 V	3.6 V					-500							
			5.5 V	5.5 V					-900							
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	0 to 5.5 V	±0.5		±1		±2	μA						
	B port		0 to 5.5 V	0 V	±0.5		±1		±2							
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND	$\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V		±1		±2	μA						
	B port										$\overline{OE} = \text{don't care}$	0 V	5.5 V		±1	±2
	A port											5.5 V	0 V		±1	±2
I <sub>CCA</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					20	μA						
			5 V	0 V					20							
			0 V	5 V					-2							
I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					20	μA						
			5 V	0 V					-2							
			0 V	5 V					20							
I <sub>CCA</sub> + I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V	1.65 V to 5.5 V					30	μA						

 (1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

 (2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

 (3) The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

 (4) The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

 (5) An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

 (6) An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

## Electrical Characteristics<sup>(1) (2)</sup> (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	MIN	MAX	UNIT
$\Delta I_{CCA}$	DIR	DIR at V <sub>CCA</sub> – 0.6 V, B port = open, A port at V <sub>CCA</sub> or GND	3 V to 5.5 V	3 V to 5.5 V				50		μA
C <sub>i</sub>	Control inputs	V <sub>i</sub> = V <sub>CCA</sub> or GND	3.3 V	3.3 V		4		5		pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	3.3 V	3.3 V		8.5		10		pF

## Switching Characteristics

over recommended operating free-air temperature range, V<sub>CCA</sub> = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	1.7	21.9	1.3	9.2	1	7.4	0.4	7.1	ns
t <sub>PHL</sub>											
t <sub>PLH</sub>	B	A	0.9	23.8	0.8	23.8	0.7	23.4	0.7	23.4	ns
t <sub>PHL</sub>											
t <sub>PHZ</sub>	$\overline{OE}$	A	1.5	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t <sub>PLZ</sub>											
t <sub>PHZ</sub>	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t <sub>PLZ</sub>											
t <sub>PZH</sub>	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t <sub>PZL</sub>											
t <sub>PZH</sub>	$\overline{OE}$	B	1.8	32	1.5	18	1.2	12.6	0.9	10.8	ns
t <sub>PZL</sub>											

## Switching Characteristics

over recommended operating free-air temperature range, V<sub>CCA</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		V <sub>CCB</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	1.5	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t <sub>PHL</sub>											
t <sub>PLH</sub>	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t <sub>PHL</sub>											
t <sub>PHZ</sub>	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t <sub>PLZ</sub>											
t <sub>PHZ</sub>	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t <sub>PLZ</sub>											
t <sub>PZH</sub>	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t <sub>PZL</sub>											
t <sub>PZH</sub>	$\overline{OE}$	B	1.7	28.2	1.5	12.9	1.2	9.4	1	6.9	ns
t <sub>PZL</sub>											

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.6	21.2	1.1	8.8	0.8	6.2	0.6	4.4	ns
$t_{PHL}$											
$t_{PLH}$	B	A	0.8	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
$t_{PHL}$											
$t_{PHZ}$	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	ns
$t_{PLZ}$											
$t_{PHZ}$	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.8	0.8	6.3	ns
$t_{PLZ}$											
$t_{PZH}$	$\overline{OE}$	A	0.8	7.8	0.8	8.1	0.8	8.1	0.8	8.1	ns
$t_{PZL}$											
$t_{PZH}$	$\overline{OE}$	B	1.8	27.7	1.4	12.4	1.1	8.5	0.8	6.4	ns
$t_{PZL}$											

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.5	21.4	1	8.8	0.7	6	0.4	4.2	ns
$t_{PHL}$											
$t_{PLH}$	B	A	0.7	7	0.4	4.8	0.3	4.5	0.3	4.3	ns
$t_{PHL}$											
$t_{PHZ}$	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	ns
$t_{PLZ}$											
$t_{PHZ}$	$\overline{OE}$	B	2	28.7	1.8	9.7	1.4	8	0.7	5.7	ns
$t_{PLZ}$											
$t_{PZH}$	$\overline{OE}$	A	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	ns
$t_{PZL}$											
$t_{PZH}$	$\overline{OE}$	B	1.5	27.6	1.3	11.4	1	8.1	0.9	6	ns
$t_{PZL}$											

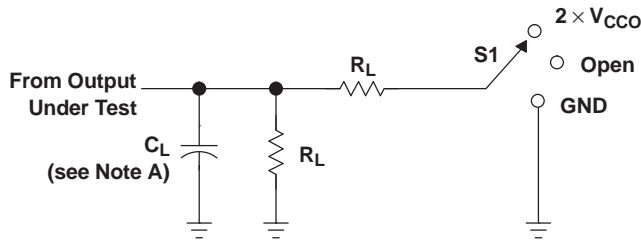
## Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.8 \text{ V}$	$V_{CCA} = V_{CCB} = 2.5 \text{ V}$	$V_{CCA} = V_{CCB} = 3.3 \text{ V}$	$V_{CCA} = V_{CCB} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pdA}$ (1)	A-port input, B-port output	2	2	2	3	pF
	B-port input, A-port output	18	19	19	22	
$C_{pdB}$ (1)	A-port input, B-port output	18	19	20	22	
	B-port input, A-port output	2	2	2	2	

(1) Power dissipation capacitance per transceiver

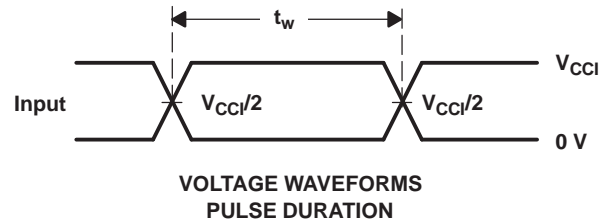
PARAMETER MEASUREMENT INFORMATION



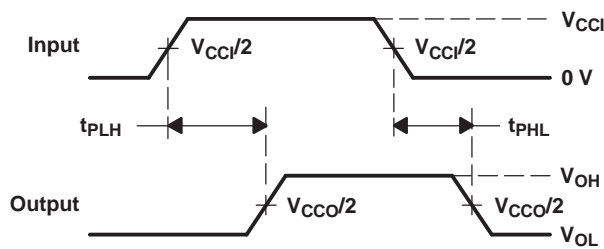
LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

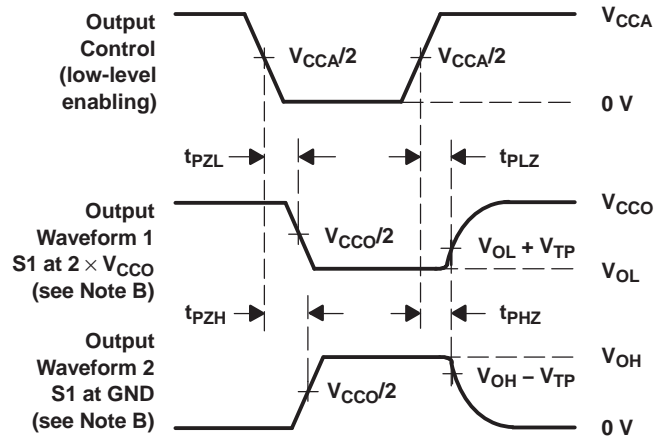
$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.8\text{ V} \pm 0.15\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	15 pF	2 k $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	15 pF	2 k $\Omega$	0.3 V



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $dv/dt \geq 1\text{ V/ns}$ ,  $dv/dt \geq 1\text{ V/ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H.  $V_{CCi}$  is the  $V_{CC}$  associated with the input port.
  - I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
  - J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVCH16T245MDGGREP	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	8UT245MEP	<a href="#">Samples</a>
CLVCH16T245MDGVREP	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LDHT245MEP	<a href="#">Samples</a>
V62/09605-01XE	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	8UT245MEP	<a href="#">Samples</a>
V62/09605-01YE	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LDHT245MEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVCH16T245-EP :**

- Catalog: [SN74LVCH16T245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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