THE DATASHEET OF

MP4001DS-LF

www.win-source.net 0086-755-83957316

MP4001

Universal Input High Brightness White LED Driver

DESCRIPTION

The MP4001 is a high efficiency step-down converter designed for driving the high brightness Light Emitting Diodes (LEDs).

The MP4001 drives external MOSFET with boundary conduction mode which features no reverse recovery loss in the freewheeling diode, soft turn on with zero-current and valley voltage for the power MOSFET. Such operation mode can achieve very high efficiency and in the same time minimize the inductor value and size. With the boundary conduction control mode, the LED current can be well regulated by control the MOSFET peak current which is sensed through an external resistor. Its low 300mV feedback voltage reduces power loss and improves the efficiency.

The MP4001 integrates a high-voltage smart LDO, which allows the AC input to power up the IC directly. The smart LDO sinks current when the input voltage is lower than 24V to achieve higher efficiency.

The MP4001 implements both PWM and DC input burst dimming The MP4001 features output short protections, maximum switching frequency limitation, under-voltage lockout and thermal shut down.

FEATURES

- Constant-current LED Driver
- Universal AC Input (85VAC-305VAC)
- Power MOSFET Zero-Current Turn On
- High Efficiency Boundary Mode Operation
- Integrated High-voltage Smart LDO
- Low 1mA Operation Current
- PWM or DC Input Burst Dimming Control
- Hiccup Short Circuit Protection
- Maxim Frequency Limited to 110kHz
- Thermal Shutdown
- Available in SOIC8 Package

APPLICATIONS

- Non-Isolated Lighting
- General Illumination
- Industrial Lighting
- Automotive/ Decorative LED Lighting
- LCD TV Backlighting
- DC/DC or AC/DC LED Driver Applications

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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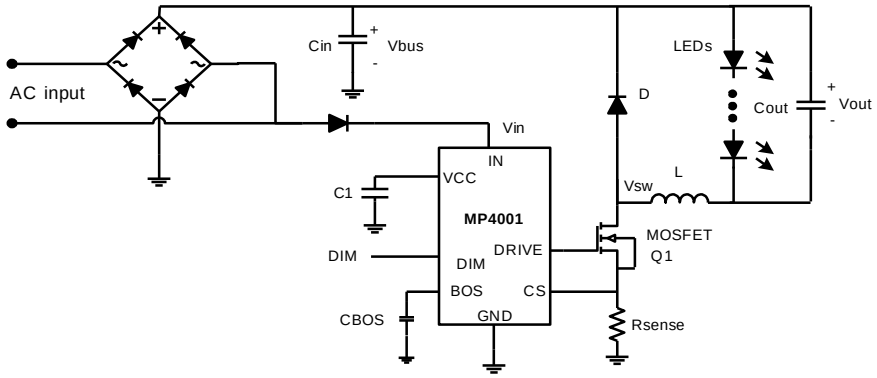
TYPICAL APPLICATION



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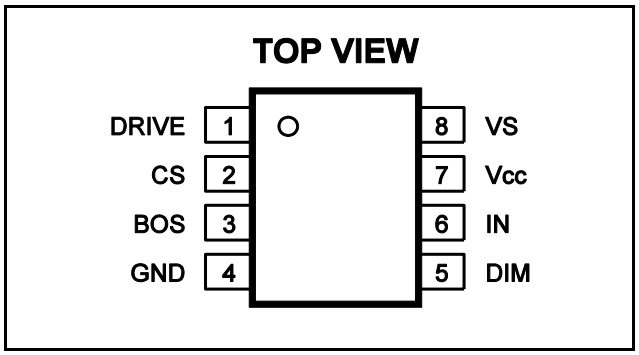
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4001DS	SOIC8	MP4001

*For Tape & Reel, add suffix –Z (eg. MP4001DS-Z)
For RoHS Compliant Packaging, add suffix –LF (eg. MP4001DS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.5V to 500V
VCC, DRIVE .....-0.3V to 11V
DIM, BOS, CS, VS.....-0.3V to 6.5V
Continuous Power Dissipation (T_A=25°C) (2)
SOIC8……..1.3W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

IN Supply 50/60Hz
AC RMS Voltage.....12V to 350V
IN Supply DC Voltage.....12V to 450V
VCC, DRIVE…….-0.3V to 10.5V
Operating Junct. Temp(T_J)..... –40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 .....96 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on approximately 1” square of 1 oz copper.

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ELECTRICAL CHARACTERISTICS

V_{IN} =24VDC, no load on pin Drive, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input with An AC Voltage	V_{INAC}	50/60Hz AC RMS at Pin IN	9		350	V
Input with A DC Voltage	V_{INDC}	A DC voltage at Pin IN	9		450	V
Input Supply Current (Quiescent)	I_{INQS}	V_{DIM} = 0V		0.64		mA
Input Supply Current (Operation)	I_{INRUN}	V_{DIM} = 5 V		1		mA
VCC Internal Regulated Voltage	VCC_H	V_{IN}=14-24V, VCC Peak Voltage		9.8		V
	VCC_L	V_{IN}=14-24V, VCC Valley Voltage		8.9		V
	VCC	V_{IN}=10.5V or V_{IN}=35V		8.5		V
VCC Hysteresis	VCC_{HYS}			0.88		V
VCC UVLO	VCC_{UVLO}		6.5	7.25	8	V
VCC UVLO Hysteresis	VCC_{UVLO_HYS}			1		V
DIM Input High	V_{DIMH}	V_{DIM} rising, V_{BOS}=1.2V	1.5			V
DIM Input Low	V_{DIML}	V_{DIM} falling, V_{BOS}=1.2V			0.9	V
DIM Pull up Current	$I_{DIM\_PULL\_UP}$	V_{DIM}=0V		10		μA
BOS Charge Current	I_{BOS}		3	4	5	μA
BOS High Threshold	V_{BOSH}	BOS connect with a capacitor	2.1	2.42	2.6	V
PWM Dimming on Propagation Delay	$T_{PWM\_ON\_PD}$	PWM rising edge to Drive rising edge		540		ns
PWM Dimming off Propagation Delay	$T_{PWM\_OFF\_PD}$	PWM falling edge to Drive falling edge		3		μs
CS Pin Reference Voltage	V_{RS}	V_{DIM}=VCC, @TA = -40°C to +85°C	270	300	330	mV
Turn-off Propagation Delay	t_{OFF_PD}				100(4)	ns
Leading Edge Blanking Time	t_{LEB}		290		450	ns
CS Bias Current	I_{CS}		-1		1	μA
Gate Drive Source Current	I_{DRV_SOURCE}	V_{DRV}=0V		400(5)		mA
Gate Drive Sink Current	I_{DRV_SINK}	V_{DRV}=VCC		-1.2(5)		A
Drive Low Level Output Voltage	V_{DRVL}	I_{DRV}=10mA		43		mV
Drive High Level Output Voltage to Rail	V_{DRVH}	I_{DRV}=-10mA		110		mV
Gate Minimal Turn-on Time	t_{ON_MIN}				400(5)	ns
Maxim Switching Frequency	f_{SW_MAX}			110(5)		kHz
Over Temperature Protection Threshold	T_{OTP}			150		°C
Over Temperature Protection Threshold Hysteresis	T_{OTP_HYS}			30		°C
Output Short Shut Down Time	t_{SD_SHORT}	When short circuit occurs		1.7		ms

Notes:

5) Guarantee by design.

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PIN FUNCTIONS

Pin #	Name	Description
1	DRIVE	External MOSFET drive output. The zero current crossing signal is detected from this pin.
2	CS	LED current sense input. Connect the current sense resistor that programs the LED current.
3	BOS	Burst Oscillator Setting. For the DC input burst dimming, connect a capacitor from this pin to GND to program the burst dimming frequency. For the external PWM dimming, connect a resistor such as 300kΩ from this pin to GND and apply the logic signal to the DIM pin.
4	GND	Ground.
5	DIM	Dimming Control Input. For DC input burst dimming control, the voltage of 0V to 2.42V at DIM pin linearly sets the burst-mode duty cycle from minimum to 100%. For external PWM dimming control, connect the PWM signal to DIM pin. Open DIM pin or pull it high if no dimming control is applied.
6	IN	Input Supply Pin. By connecting the IN pin to AC input as power source of VCC.
7	VCC	Internal regulated supply voltage output. Must be locally bypassed. The VCC voltage provides the power for IC logic and driving external MOSFET.
8	VS	Test pin. Connect to GND for normal operation.

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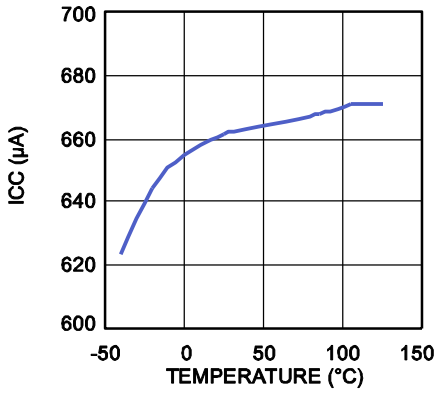
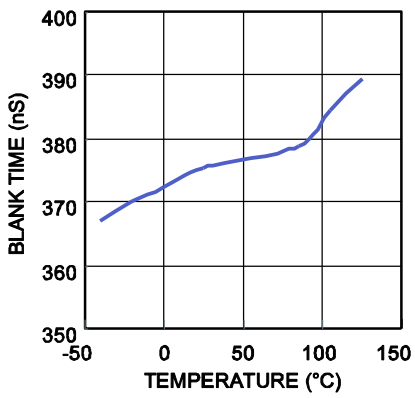
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =90-265VAC, V_{LED}=10-30V, 3-9LEDS, I_{LED}=350mA, T_A = +25°C, unless otherwise noted.

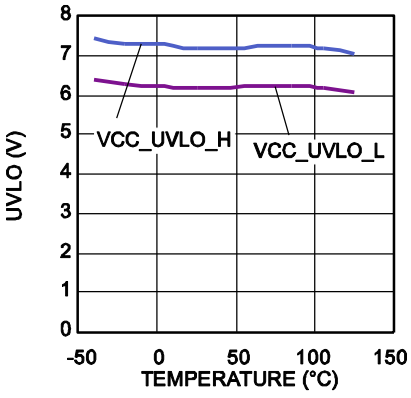
ICC_10.5V_CS=5V vs. Temp



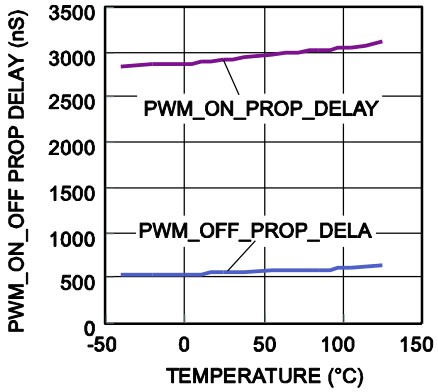
T_L_EDGE_BLANK_TIME vs. Temp



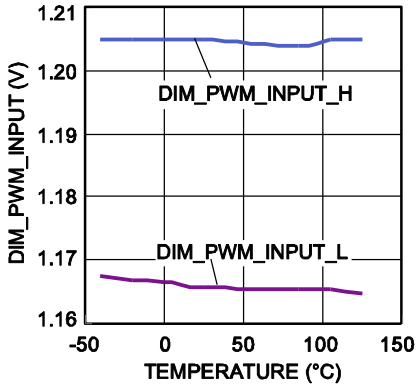
VCC_UVLO vs. Temp



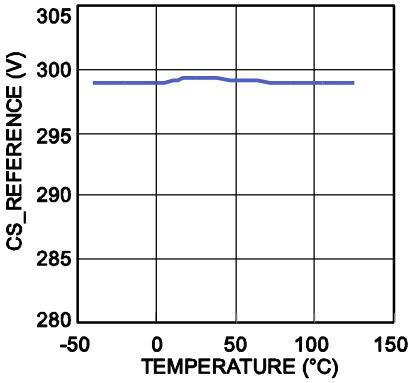
PWM_ON_OFF PROP DELAY vs. Temp



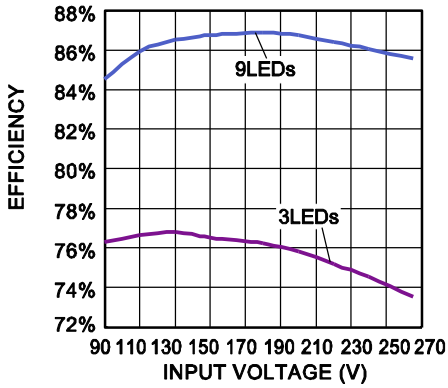
DIM_PWM_INPUT vs. Temp



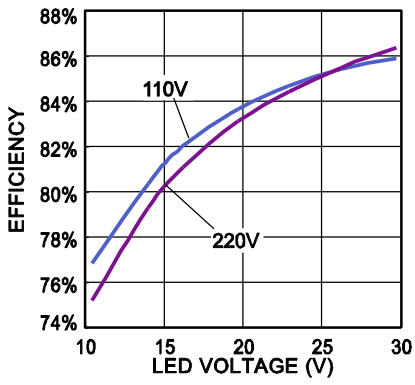
CS_Reference vs. Temp



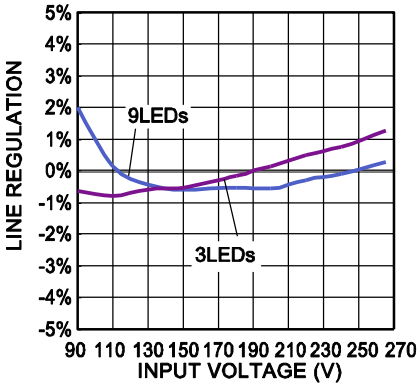
Efficiency Vs. Input Voltage



Efficiency Vs. LED Voltage



Line Regulation



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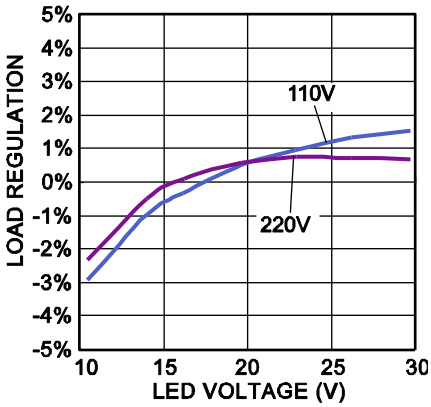
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =90-265VAC, V_{LED}=10-30V, 3-9LEDS, I_{LED}=350mA, T_A = +25°C, unless otherwise noted.

Load Regulation



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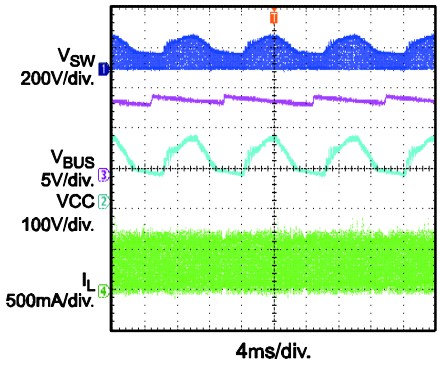
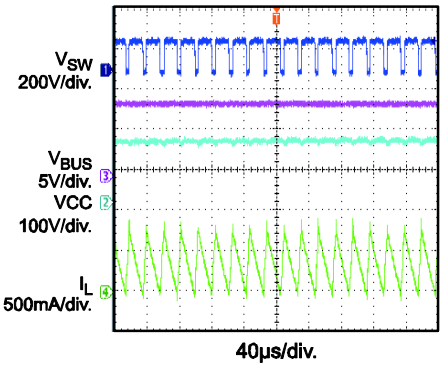
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =90-265VAC, V_{LED}=10-30V, 3-9LEDS, I_{LED}=350mA, T_A = +25°C, unless otherwise noted.

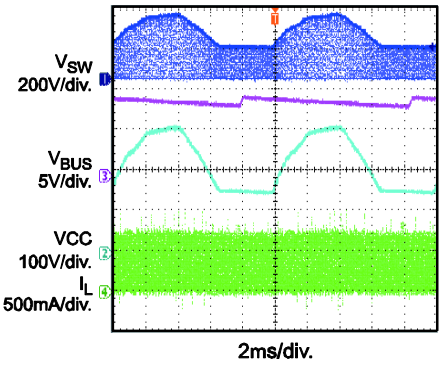
Steady State@110VAC



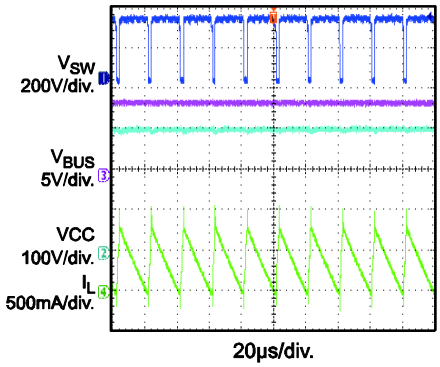
Steady State@110VAC



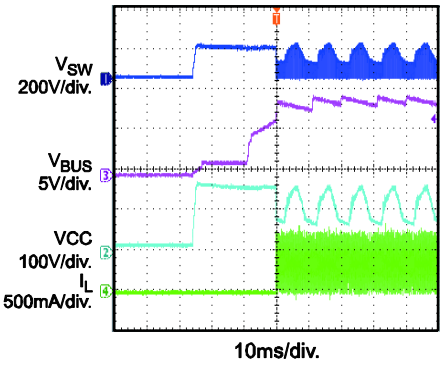
Steady State@220VAC



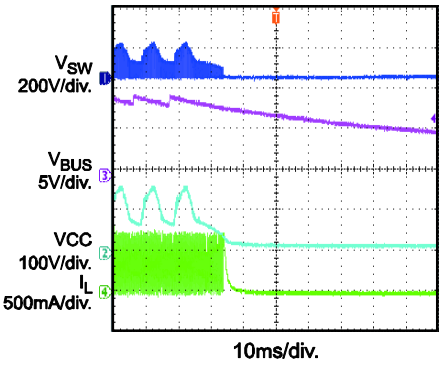
Steady State@220VAC



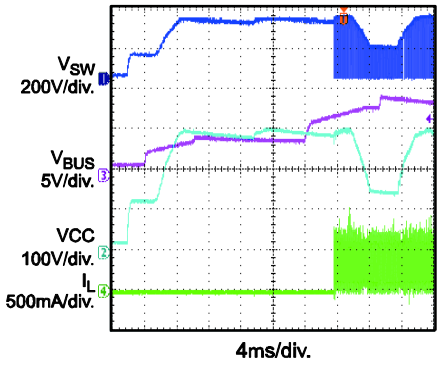
Power Up@110VAC



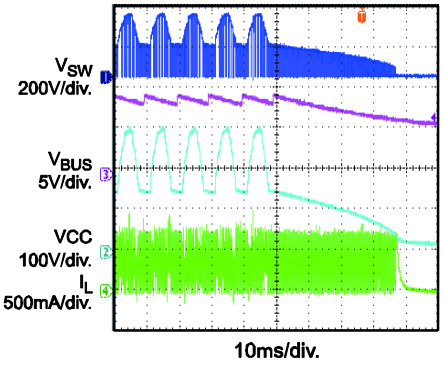
Power Down@110VAC



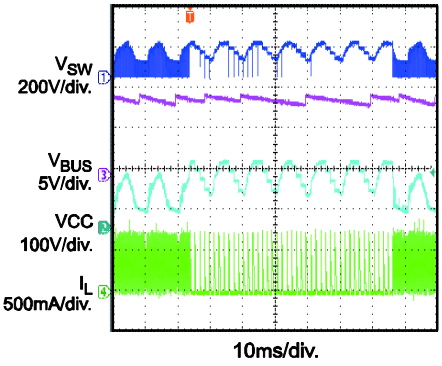
Power Up@220VAC



Power Down@220VAC



Short Load and Recover @110VAC



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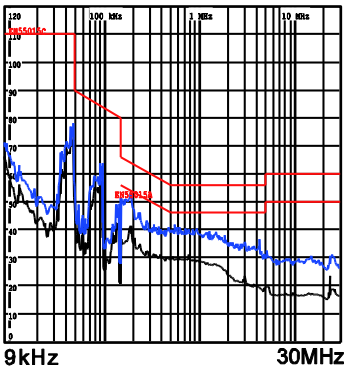
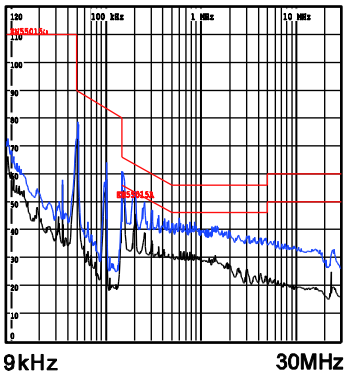
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =90-265VAC, V_{LED}=10-30V, 3-9LEDS, I_{LED}=350mA, T_A = +25°C, unless otherwise noted.

EMI VIN=120VAC, VLED=30V



EMI VIN=230VAC, VLED=30V



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FUNCTIONAL BLOCK DIAGRAM

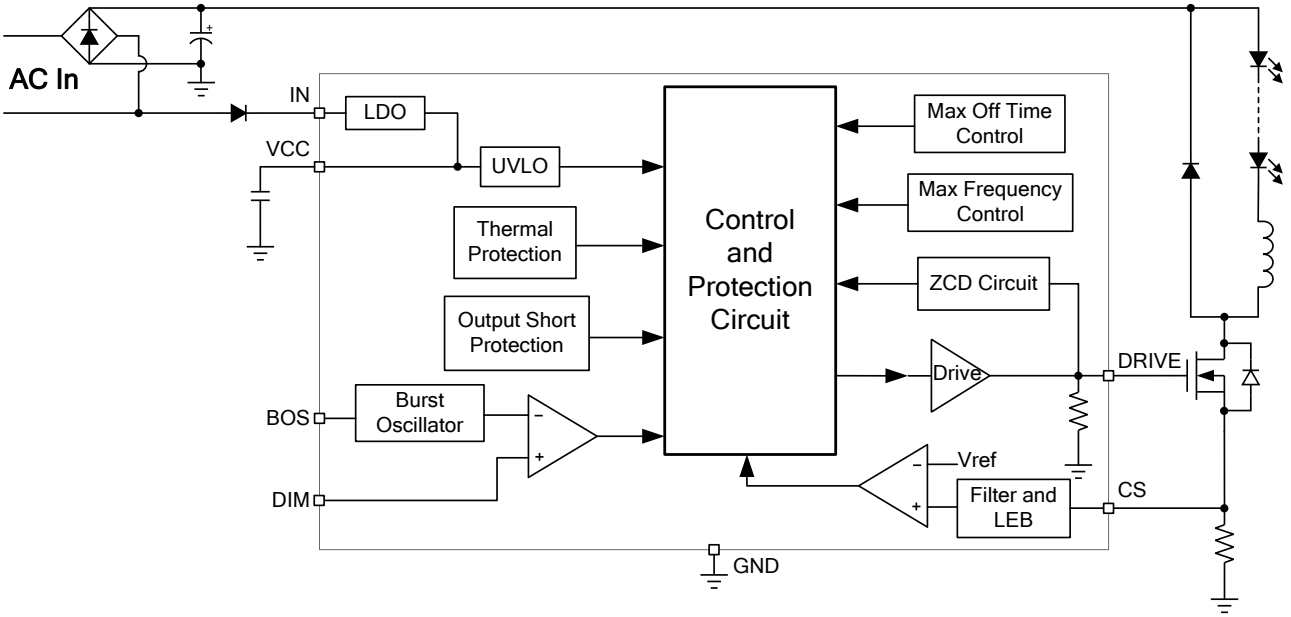

Figure 1: Function Block Diagram.

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OPERATION

Internal Regulator

MP4001 employs a high-voltage with 500V break down voltage JFET circuit, which allows the universal AC line input to power the IC directly. The MP4001 integrated a smart LDO which conducts only when the voltage on IN pin is lower than 24V. With such smart LDO design, the IC power dissipation is significantly reduced and high frequency operation is feasible. The output waveform of VCC voltage is a sawtooth wave when this LDO is active, the peak and valley value of this sawtooth wave are 9.8V and 8.9V.

To avoid the risk that the VCC voltage drops too low to cause the driving capability of DRIVE signal, the MP4001 integrated another LDO to regulate the VCC voltage to 8.5V. The following figure shows the structure of internal LDO.

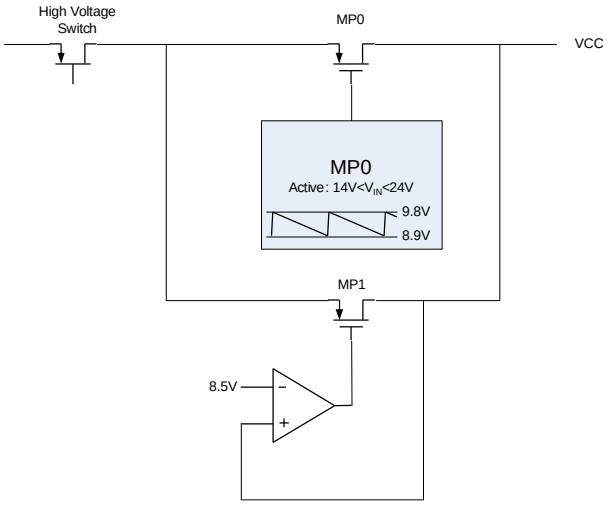

Figure 2: Functional Block Diagram of LDO

The MP0 is the smart LDO active only when V_{IN} is at the range of 14V-24V and MP1 is the 8.5V LDO.

Figure3 shows the waveform of VCC voltage in different VCC capacitance. To design the VCC capacitor value, the following conditions must be satisfied:

1. The MP0 should be active every time the IN voltage gets to 14V-24V.

2. The MP1 should NOT be active when the IN voltage is higher than 24V to ensure the high efficiency.

3. the VCC voltage can NOT drop to lower than VCC UVLO value.

The following is to follow these limitations

$$(9.8V - 8.9V) < \Delta VCC < (9.8V - 8.5V)$$

$$\Delta t \approx \frac{1}{2 * f_{line}}$$

$$I_{VCC} = I_Q + f_s * Q_g$$

$$C_{VCC} * \frac{\Delta VCC}{\Delta t} = I_{VCC}$$

Where, f_{line} is frequency of AC input, I_Q is the quiescent current of MP4001, fs is switching frequency, Q_g is the total gate charge of Power MOSFET.

For most application a 10uF-22uF VCC capacitor is recommended.

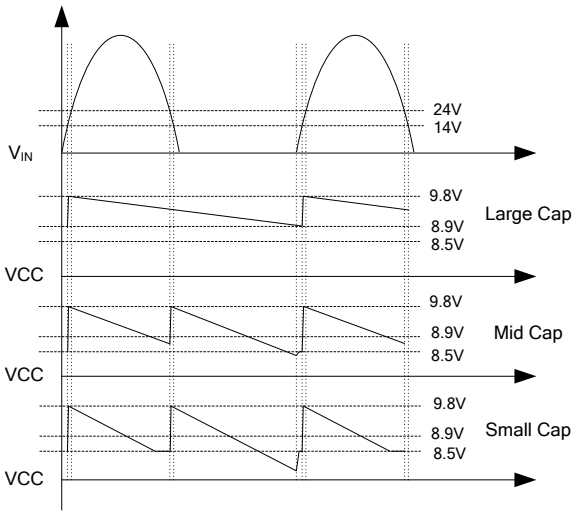

Figure 3: VCC Voltage in Different Capacitance

LED Current Regulation and Valley Detection

With a floating buck converter configuration, as shown in the typical application circuit, MP4001 turns off the MOSFETs Q1 with a peak current control. The peak current is sensed with a resistor R_{sense} and feeds back to CS pin. The peak current is regulated as:

$$I_{L\_PEAK} = \frac{300mV}{R_{sense}}$$

In normal operations, MP4001 turns on Q1 when the current in the freewheeling diode goes to zero. As a result, the average LED current is well regulated as:

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$$I_{LED} = \frac{VREF}{2R_{sense}}$$

The zero-current detection is realized at DRIVE pin by sensing the MOSFET drain dv/dt current through the Q1's miller cap. When the current of freewheeling diode goes to zero, Q1 drain voltage (V_{SW}) drops from V_{BUS} to (V_{BUS} -V_{OUT}) and starts oscillation caused by the inductor and the parasitic caps. When V_{SW} reaches the minimum value, the dv/dt current through the miller cap changes from negative to zero. At this time, the MP4001 turns on Q1. As a result, MP4001 turns on Q1 when the inductor current goes to zero and Q1 drain voltage is at the minimum. MP4001 controls the buck converter operation in current boundary conduction mode.

It is usually recommended to add a 10pF cap between the drain and source of Q1 to help for the zero current detection.

A cap Cout can be used in parallel with the LED string to reduce the current ripple.

Such boundary operation mode can minimize the Q1 turn on loss and eliminate the freewheeling diode reverse recovery loss so that high switching frequency is possible to reduce passive components' size. Furthermore, the required inductance value is small, which can help further inductor size reduction.

Brightness Dimming Control

MP4001 can employs a burst dimming control scheme so that a DC signal can control the dimming by varying the DC voltage level, or an external PWM signal can control the dimming by varying the duty cycle.

For the DC input dimming control, a voltage from 0V to 2.42V is recommended to connect to the DIM pin. 2.42V and above is for the 100% brightness. 120mV and below is for the 5% minimal brightness. A cap C_{BOS} is connected from BOS pin to GND to program the burst frequency f_{DIM}:

$$C_{BOS} = i_{BOS}/(V_{BOSH} \times f_{DIM})$$

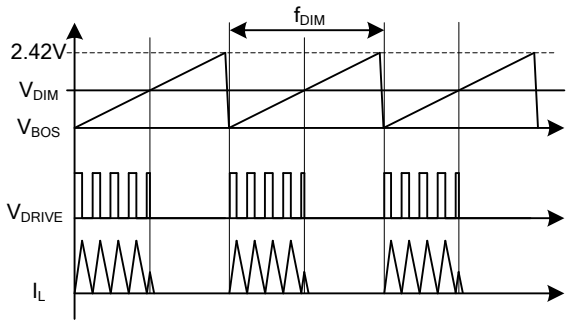

Figure 4: DC Burst Dimming

For the PWM input dimming control, a 100Hz to 2kHz PWM signal is recommended to connect to the DIM pin. BOS pin is connected to GND through a 300kΩ resistor, setting about 1.2V reference for the PWM input logic signal. PWM input high will make the IC switching. PWM input low turns off the IC.

While doing dimming, the dimming high signal force the DRIVE signal high and the dimming low signal force the DRIVE signal to low. There will be a case that the dimming low interval is too small for Inductor current reaching zero, the CCM will be observed. So the rectifying diode (D in Typical Application) must be Ultra-Fast diode or Super-Fast diode.

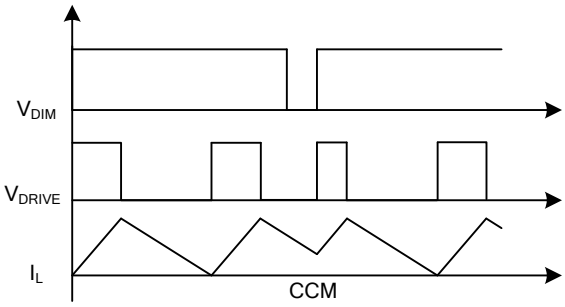

Figure 5: CCM in Large Dimming Duty

For application that do not need burst dimming control, open DIM pin and short BOS pin to GND

Frequency Setting and Inductor Design

In case the zero-current detection circuit fails, which can happens in start up with a large output cap and in output short condition, a maximum off time of about 1.7ms is applied to make sure MP4001 is still in operation and the short current doesn't run away.

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A maximum 110kHz switching frequency is set by MP4001 to avoid extreme losses in the circuit and ensure better EMI performance. If the converter reaches the maximum frequency, it will operate in discontinuous current conduction mode. Such operation mode should be avoided since the LED current is out of regulation.

In order to design the switching frequency f_s within the 30kHz to 110kHz range, inductor design is critical.

$$L = \frac{1}{f_s \cdot 2 \cdot I_{LED}} \cdot \frac{(V_{bus} - V_{out}) \cdot V_{out}}{V_{bus}},$$

where, V_{BUS} is the input voltage of the Buck converter, V_{OUT} is the LED voltage.

Hiccup Output Short Protection

If the entire LED string is shorted, V_{OUT} is zero. Due to the minimal on time limitation, the inductor current will be out of regulation. The MP4001 can detect such failure and shut down for about 1.7ms, and then re-tries the operation. Such hiccup protection can not only eliminate the thermal issue due to short circuit current, but also maintain normal operation if the protection is mis-triggered.

Under-Voltage Lockout (UVLO) Protection

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 7.25V while its falling threshold is a consistent 6.25V.

Thermal Shut down Protection

An accurate temperature protection is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, it shuts down the whole chip. When the temperature is lower than its lower threshold, the chip is enabled again.

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DESIGN EXAMPLE

The design example introduces a typical application of non-isolated LED lighting base on MP4001. Figure 6 shows the schematic of this application.

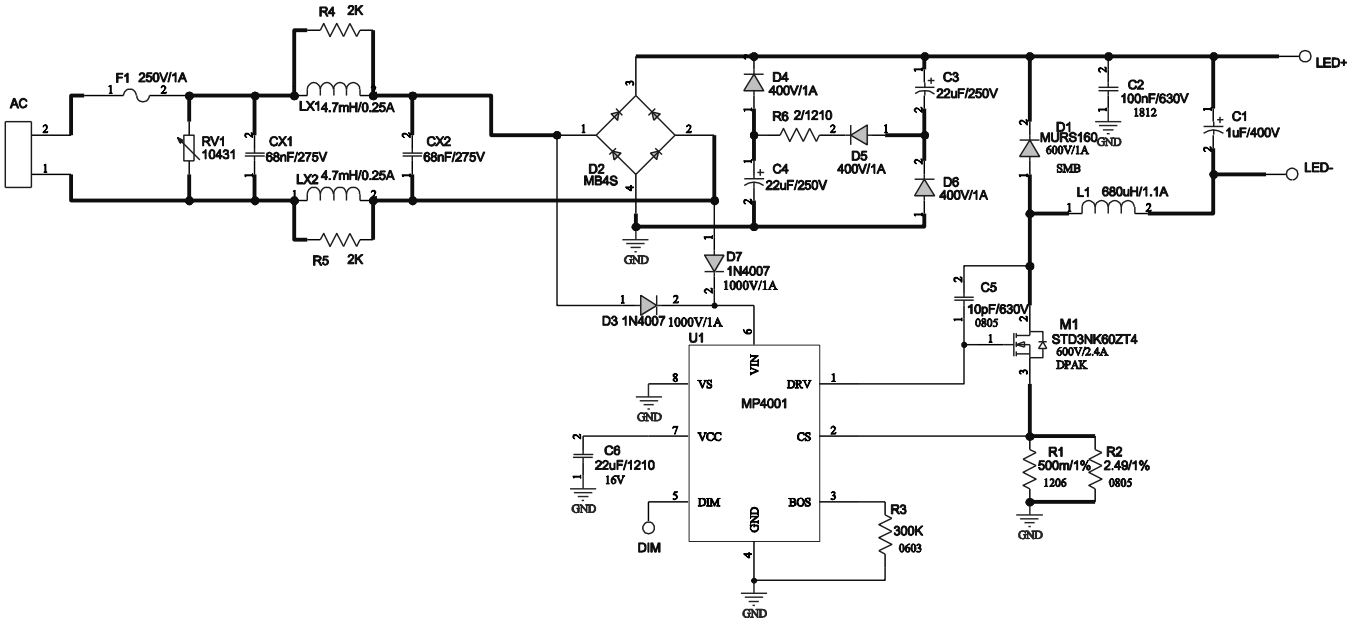

Figure 6: Schematic

Specification:
Input Voltage: Universal Input (90-265VAC)
LED Voltage: 10-30V
LED Current: 350mA

Passive PFC Circuit

To improve the Power Factor of this circuit, the valley fill circuit is employed.

The following figures show the operation process of Valley Fill Circuit.

Stage A: The AC line voltage rises from Va to twice of Va, the circuit is powered by AC line

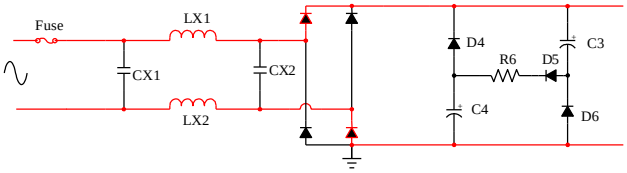

Figure 7: Stage A of Valley Fill Circuit

Stage B: The AC line voltage rises from $2V_a$ to peak voltage of AC line voltage V_p. The capacitor C3and C4 is charged up by AC line, the circuit is powered by AC line.

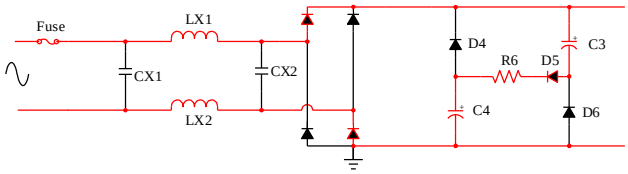

Figure 8: Stage B of Valley Fill Circuit

Stage C: The AC line voltage drops from peak voltage of AC line voltage V_p to half of AC line peak voltage, the circuit is powered by AC line.

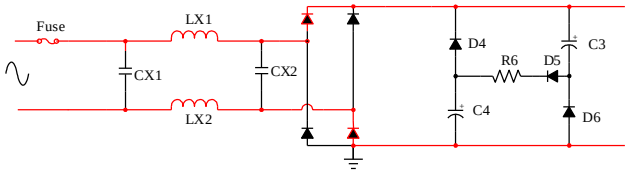

Figure 9: Stage C of Valley Fill Circuit

Stage D: The AC line voltage drops from half of AC line peak voltage to the minimum value of bus voltage V_a, the C3 and C4 paralleled to power the circuit.

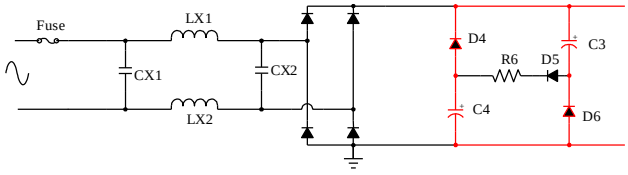

Figure 10: Stage D of Valley Fill Circuit

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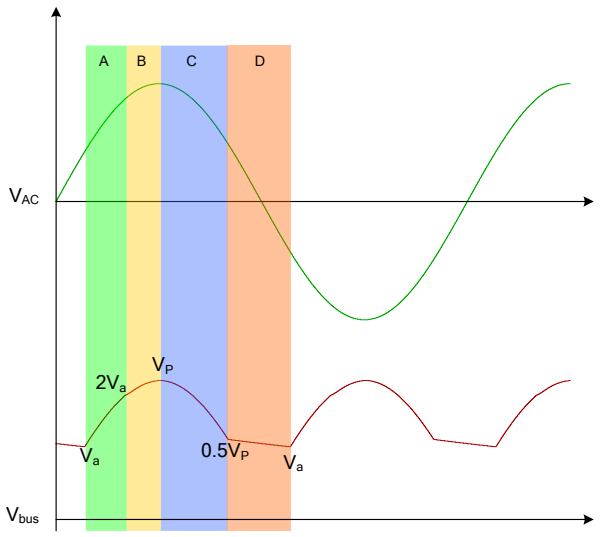

Figure 11: Waveform of Valley Fill Circuit

The valley fill circuit makes the interval that the circuit is powered by AC line extremely increased to make increase the power factor.

Here choose two 22uF/250V capacitors and three 400V/1A diode to construct the valley fill circuit.

Select the Inductor

The MP4001 work in BCM, select a proper inductor value to ensure the operating frequency is at the design range: The maximum operating frequency for MP4001 is 110kHz, the frequency must set higher than 20kHz to avoid noise.

$$L >= \frac{1}{f_{s\_max} \cdot 2 \cdot I_{LED}} \cdot \frac{(V_{bus\_max} - V_{out\_min}) \cdot V_{out\_min}}{V_{bus\_max}}$$

$$L <= \frac{1}{f_{s\_min} \cdot 2 \cdot I_{LED}} \cdot \frac{(V_{bus\_min} - V_{out\_max}) \cdot V_{out\_max}}{V_{bus\_min}}$$

Choose a 680uH inductor with the maximum operating frequency around 60kHz and minimum operating frequency around 20kHz.

The saturated current of inductor must be greater than twice of LED current.

Select Power MOSFET

The voltage stress of MOS must be greater than the maximum input voltage (375V).

The peak current through the MOSFET is the peak value of inductor current, which equals twice of LED current. The RMS current of MOS can be gotten from the following equation.

$$I_{MOS\_RMS} = 2 * I_{LED} * \sqrt{\frac{V_{out}}{3 * V_{bus}}}$$

Choose a MOSFET with 600V voltage rating and 2.4A current rating.

Select Rectifying Diode

The voltage stress of the rectifying diode must be greater than the maximum input voltage (375V).

The average current of the rectifying diode can be calculated by following equation.

$$I_{D\_AVG} = 2 * I_{LED} * (1 - \frac{V_{out}}{V_{bus}})$$

Choose an ultra-fast diode with 600V voltage rating and 1A current rating.

Select Current Sense Resistor

The current sense resistor is selected by the following.

$$R_{CS} = \frac{300mV}{2 * I_{LED}}$$

Use a 500mOhm and a 2.49Ohm resistor parallel as the current sense resistor.

Select the Output Capacitor

The output capacitor should be large enough to filter the output ripple current and so that the LED current ripple is in a desired range.

For a ceramic output capacitor, its value should be:

$$C_{OUT} \geq \frac{I_{L\_PEAK}}{8 f_{s\_min} \cdot R_{LED} \cdot I_{LED\_ripple\_pk\_pk}}$$

Where RLED is the dynamic resistor of LED load.

$$R_{LED} = \frac{\Delta V_{LED}}{\Delta I_{LED}}$$

f_{s_min} is the minimum operating frequency, which occurs at the minimum input voltage and maximum output voltage condition for this application.

$$f_{s\_min} = \frac{(V_{bus\_min} - V_{LED\_max}) * V_{LED\_max}}{L * I_{L\_PEAK} * V_{bus\_min}}$$

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Considering the $I_{L\_PEAK}=2*I_{LED}$, Then the value of output capacitor is:

$$C_{OUT} \geq \frac{L*I_{LED}^{2}*V_{bus\_min}}{2(V_{bus\_min}-V_{LED\_max})*V_{LED\_max}\cdot R_{LED}\cdot I_{LED\_ripple\_pk\_pk}}$$

If using an electrolytic output capacitor, its ESR dominates its impedance. The ESR value should be:

$$R_{ESR\_COUT} < \frac{R_{LED}\cdot I_{LED\_ripple\_pk\_pk}}{I_{L\_PEAK}}$$

Choose 1uF/400V electrolytic capacitor as the output capacitor.

Select VCC Capacitor

To ensure the high efficiency, the VCC capacitor must be designed carefully.

$$(9.8V-8.9V) < \Delta VCC < (9.8V-8.5V)$$

$$\Delta t \approx \frac{1}{2*f_{line}}$$

$$I_{VCC} = I_Q + f_s * Q_g$$

$$C_{VCC} = \frac{I_{VCC}*\Delta t}{\Delta VCC}$$

From the formulas, choose a 22uF/16V ceramic capacitor as VCC capacitor.

EMI and Surge

To pass the surge test, the full-wave rectifying circuit should be adopted for supplying the VIN pin.

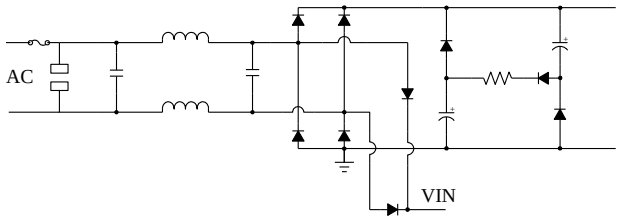

Figure 12 Full-Wave Rectification for VIN Pin

To achieve good EMI result, differential capacitors and differential inductors are needed. Make sure NO differential inductor exist between rectifying bridge and the bus capacitor; otherwise it can NOT pass the surge test.

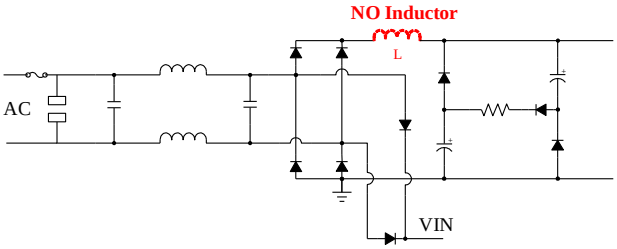

Figure 13: EMI Structure

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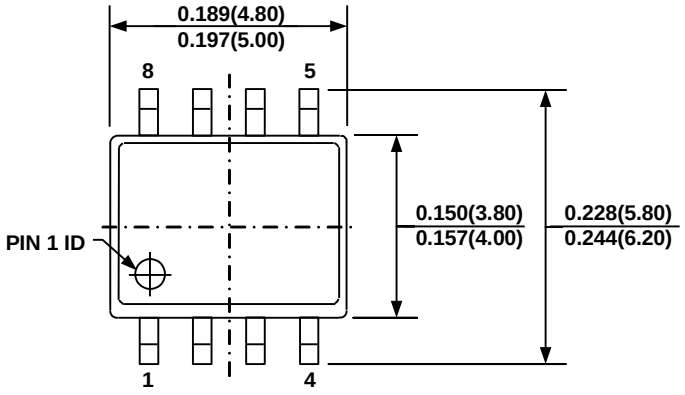
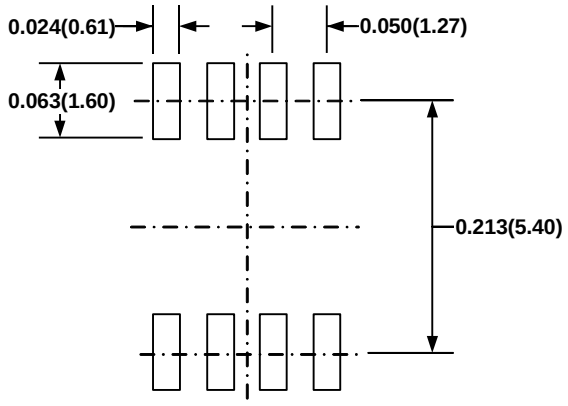
PACKAGE INFORMATION

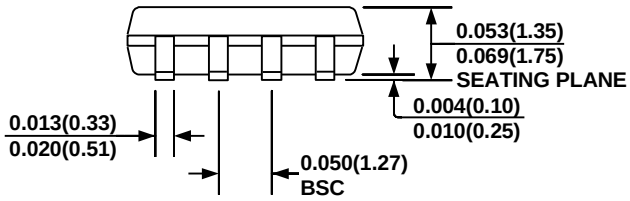
SOIC8



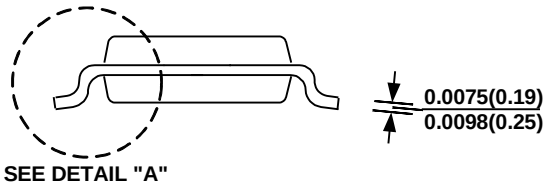
TOP VIEW



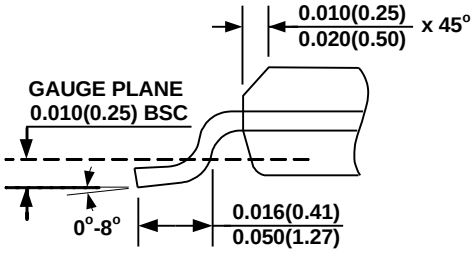
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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