

VMMK-3503

0.5 - 18 GHz Variable Gain Amplifier in SMT Package



Data Sheet



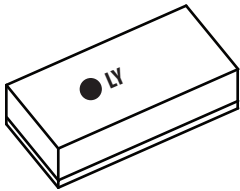
Lead (Pb) Free
RoHS 6 fully
compliant



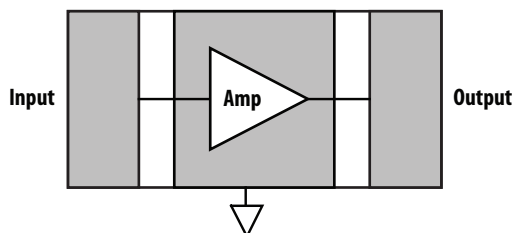
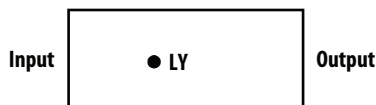
Description

The VMMK-3503 is a small and easy-to-use, broadband, variable gain amplifier operating in various frequency bands from 0.5-18 GHz. It is housed in the Avago Technologies' industry-leading and revolutionary sub-miniature chip scale package (GaAsCap wafer scale leadless package) which is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly equipment. The VMMK-3503 provides maximum gain of 12 dB with a typical gain range of 23 dB where the gain control is accessed from the input port by way of a large value external resistor. It can be operated from 3 V to 5 V power supply. It is fabricated using Avago Technologies unique 0.25 μm E-mode PHEMT technology which eliminates the need for negative gate biasing voltage.

WLP0402, 1 mm x 0.5 mm x 0.25 mm



Pin Connections (Top View)



Note:
"L" = Device Code
"Y" = Month Code

Features

- 1 x 0.5 mm surface mount package
- Ultrathin (0.25 mm)
- Broadband frequency range: 0.5 to 18 GHz
- In and output match: 50 ohm
- All Positive DC Voltage Supply and Control
- CMOS-compatible gain control voltage

Specifications (6 GHz, V_{dd} = 5 V, Z_{in} = Z_{out} = 50 Ω)

- Small signal gain: 12 dB typ
- Gain control range: 23 dB typ
- Noise Figure = 3.5 dB typ

Applications

- 2.4, 3.5, and 5-6 GHz WLAN and WiMax
- 802.16 & 802.20 BWA systems
- Radar and ECM systems
- UWB
- Generic IF amplifier and VGA



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 50 V
ESD Human Body Model = 450 V
Refer to Avago Application Note A004R:
Electrostatic Discharge, Damage and Control.

Electrical Specifications

Table 1. Absolute Maximum Rating [1]

Symbol	Parameters/Condition	Unit	Absolute Max
Vdd	Supply Voltage (RF Output) [2]	V	6
Vc	Gain Control Voltage	V	2
Id	Supply Current [2]	mA	70
P _{in, max}	CW RF Input Power (RF Input) [3]	dBm	+15
P _{diss}	Total Power Dissipation	mW	420
T _{ch}	Max Channel Temperature	°C	+150
θ _{jc}	Thermal Resistance [4]	°C/W	103

Notes

1. Operation of this device above any one of these parameters may cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature T_b = 25° C
4. Thermal resistance is measured from junction to board using IR method

Table 2. DC and RF Specifications [1]

T_A = 25° C, Frequency = 6 GHz, Vdd = 5 V, Z_{in} = Z_{out} = 50 Ω (unless otherwise specified)

Symbol	Parameters/Condition	Unit	Minimum	Typical	Maximum
Id_Max_Gain	Supply Current at Vc = 1.8 V	mA	50	58	66
Id_Min_Gain	Supply Current at Vc = 0.65 V	mA	17	24	31
Max_Gain	Gain at Vc = 1.8 V	dB	10.5	12	
Min_Gain	Gain at Vc = 0.65	dB		-11	-9
Gain Control Range	Max_Gain – Min_Gain	dB	19.5	23	
NF	Noise Figure at Vc = 1.8 V	dB		3.5	4.2

Table 3. Typical Performance [2]

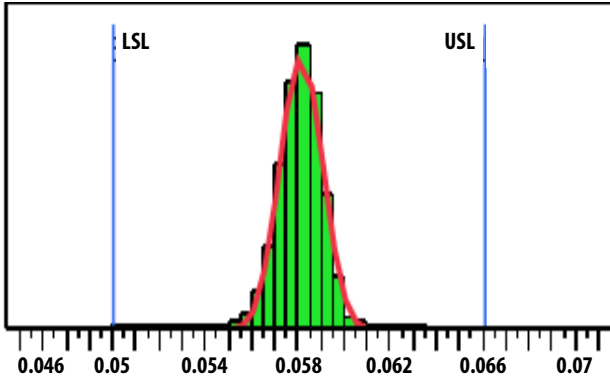
T_A = 25° C, Frequency = 6 GHz, Vdd = 5 V, Z_{in} = Z_{out} = 50 Ω (unless otherwise specified)

Vc V	Id mA	Gain dB	NF dB	IIP3 [3] dB	OP1dB dBm	OPsat dBm	IRL dB	ORL dB
1.8	58	12	3.5	9	8	12	-12	-13
0.9	42	-2		0		5.8		
0.65	24	-11	19	3		-0.5	-8	-18

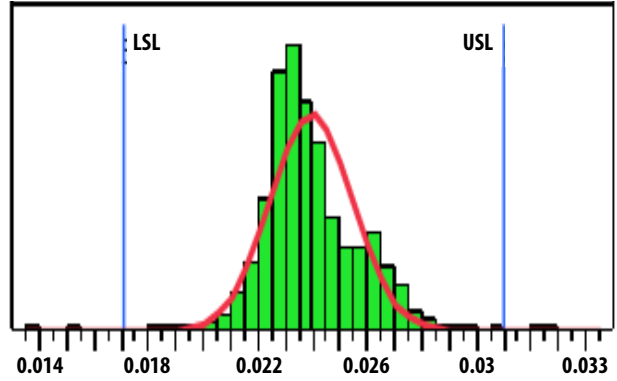
Notes

1. Measured Data obtained from G-S probing on wafer. Losses of test fixture have been de-embedded.
2. Measured Data obtained from G-S-G probing on substrate. Losses of test fixture have been de-embedded.
3. IIP3 test condition: 2-tone freq. separation = 10 MHz, Pin = -20 dBm

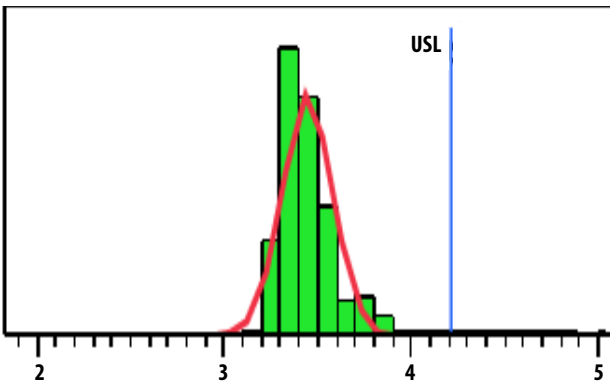
Product Consistency Distribution Charts at 6.0 GHz, Vdd = 5 V, Vc = 1.8 V unless specified otherwise



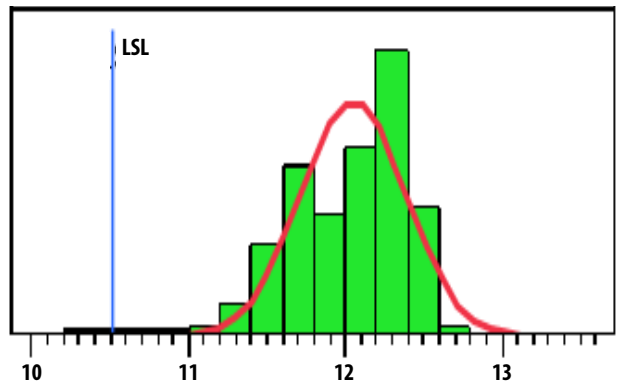
ID_MAX_1.8 @ Vdd = 5 V, Vc = 1.8 V, Mean = 58 mA, LSL = 50 mA, USL = 66 mA



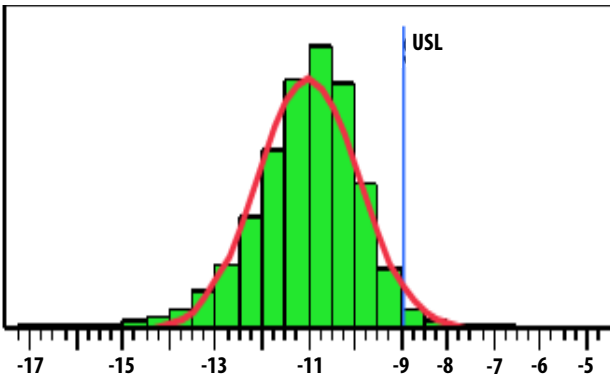
ID_MIN_0.65 @ Vdd = 5 V, Vc = 0.65 V, Mean = 24 mA, LSL = 17 mA, USL = 31 mA



NF @ 6GHz, Mean = 3.5 dB, USL = 4.2 dB



GAIN_MAX_1.8 @ 6 GHz, Mean = 12 dB, LSL = 10.5 dB



GAIN_MIN_0.65 @ 6 GHz, Mean = -11 dB, USL = -9 dB

Notes:
 Distribution data based on 54 Kpcs part sample size from MPV lots.
 Future wafers allocated to this product may have nominal values
 anywhere between the upper and lower limits.

VMMK-3503 Typical Performance

Data obtained using GSG probing on substrate, broadband bias-T's, losses calibrated out to the package reference plane. ($T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{V}$, $Z_{in} = Z_{out} = 50\ \Omega$ unless noted)

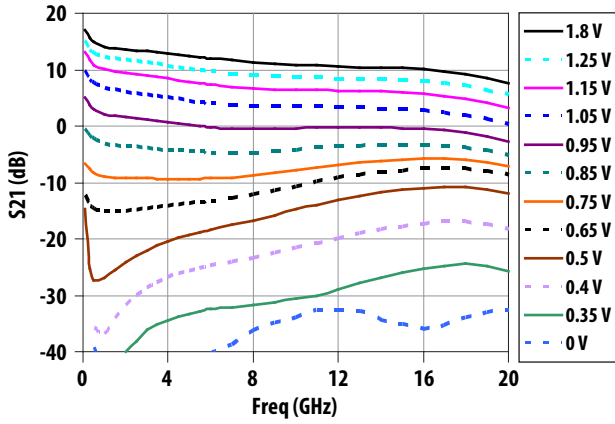


Figure 1. Gain Range vs. Vcontrol

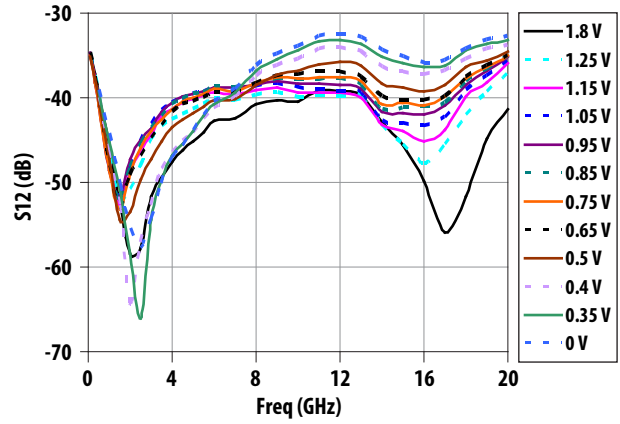


Figure 2. Reverse Isolation vs. Vc

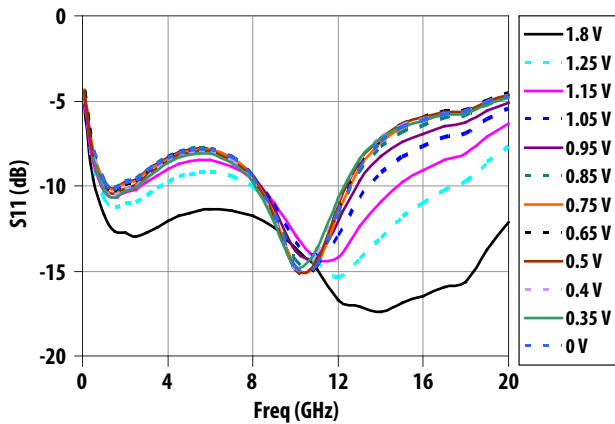


Figure 3. Input Return Loss vs. Vc

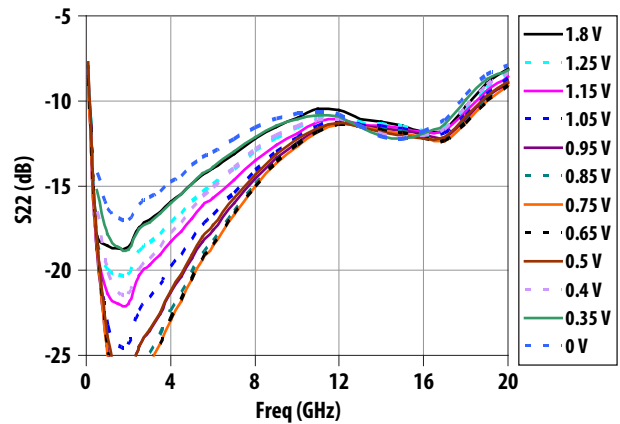


Figure 4. Output Return Loss vs. Vc

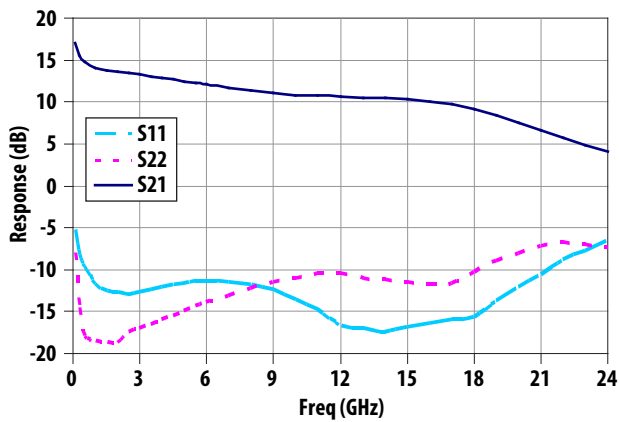


Figure 5. Broadband Gain and Return Losses ($V_c = 1.8\text{V}$)

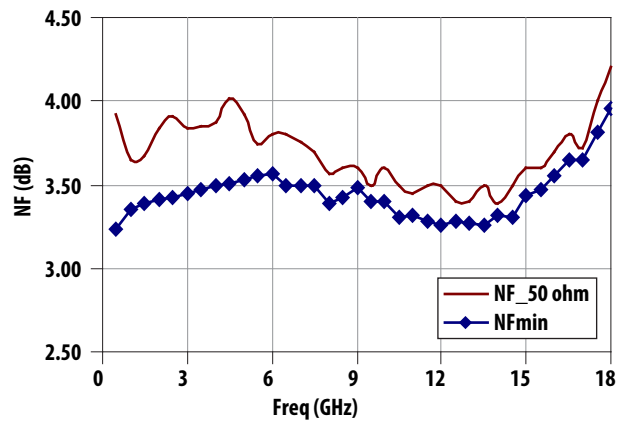


Figure 6. Noise Figure ($V_c = 1.8\text{V}$)

VMMK-3503 Typical Performance

($T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{ V}$, $Z_{in} = Z_{out} = 50\ \Omega$ unless noted)

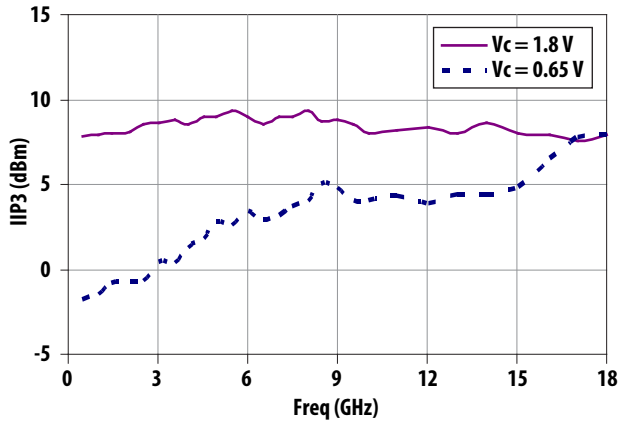


Figure 7. Input IP3 vs. Freq

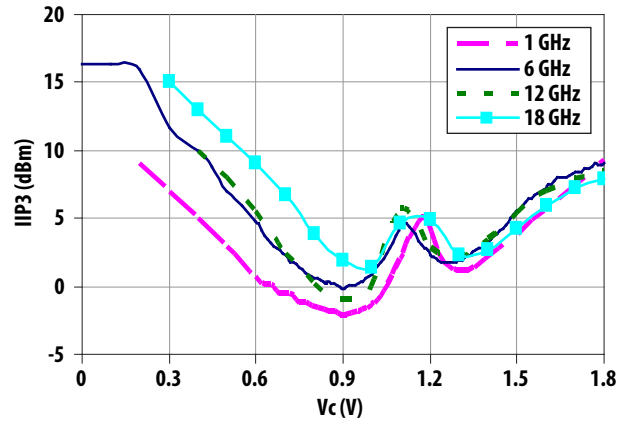


Figure 8. Input IP3 vs. Vc

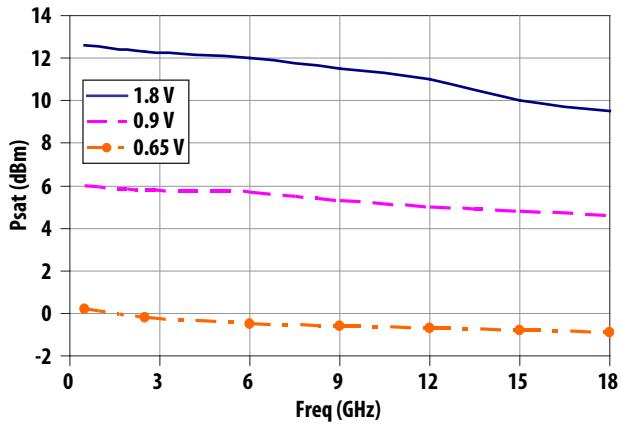


Figure 9. Saturated Power

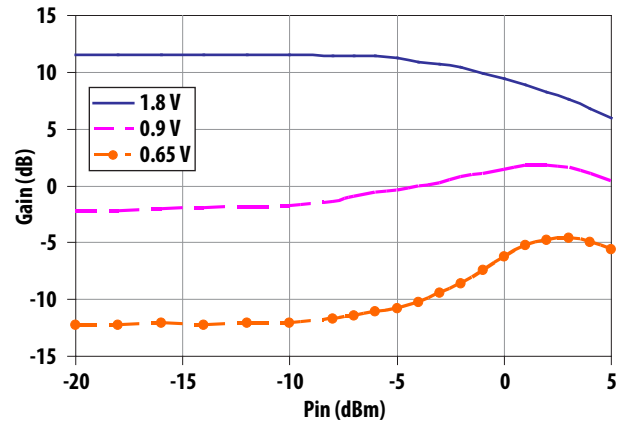


Figure 10. Gain vs. Pin at 6 GHz

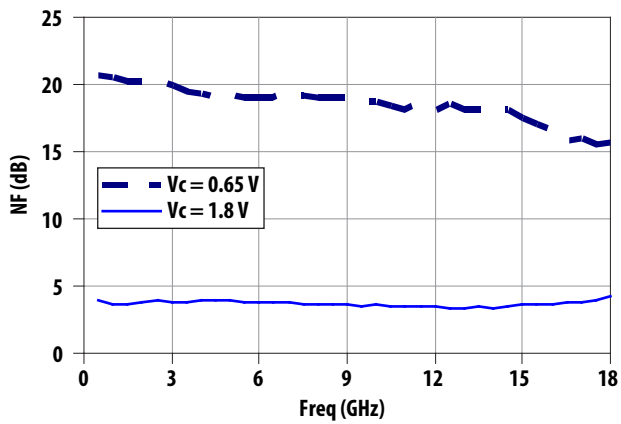


Figure 11. Noise Figure at Min and Max Gain

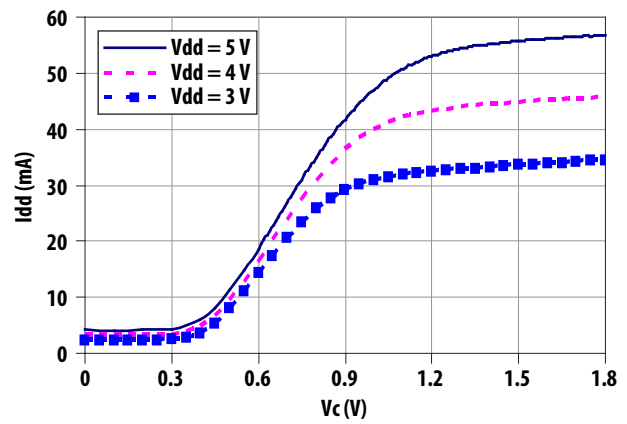


Figure 12. Supply Current over Bias

VMMK-3503 Typical Performance

($T_A = 25^\circ\text{C}$, $V_c = 1.8\text{V}$, $Z_{in} = Z_{out} = 50\ \Omega$ unless noted)

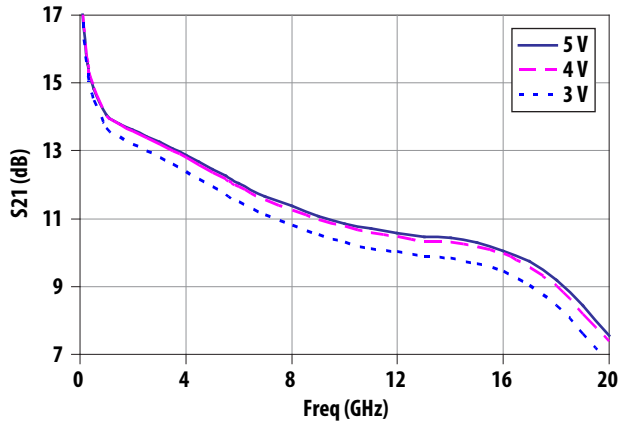


Figure 13. Max. Gain over Vdd

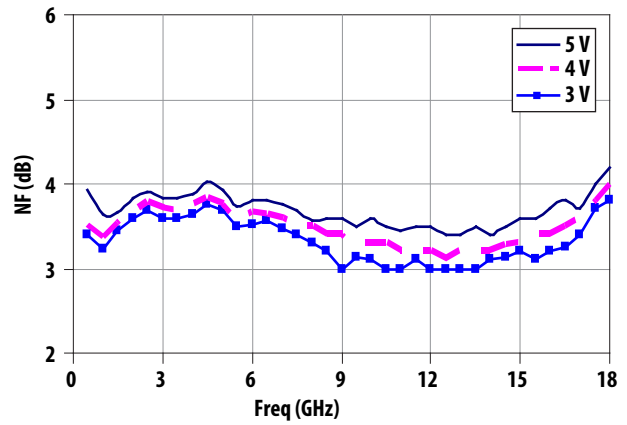


Figure 14. Noise Figure over Vdd

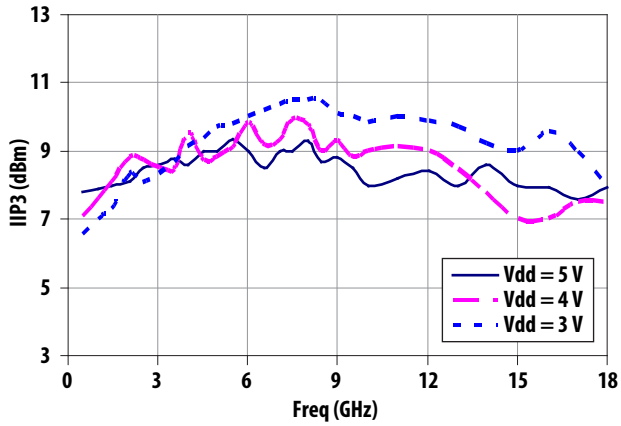


Figure 15. Input IP3 over Vdd

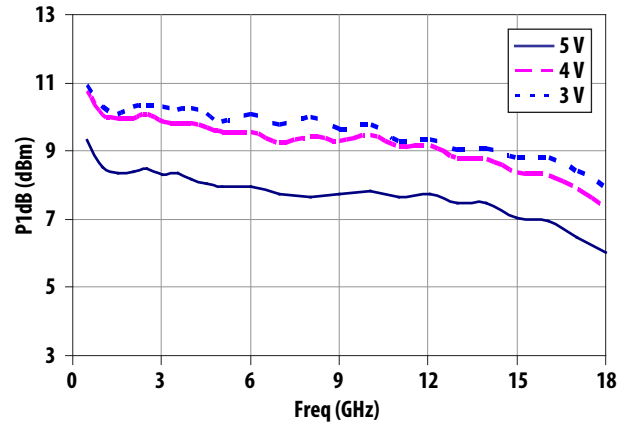


Figure 16. Output P1dB over Vdd

VMMK-3503 Typical Performance

($T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{V}$, $V_c = 1.8\text{V}$, $Z_{in} = Z_{out} = 50\ \Omega$ unless noted)

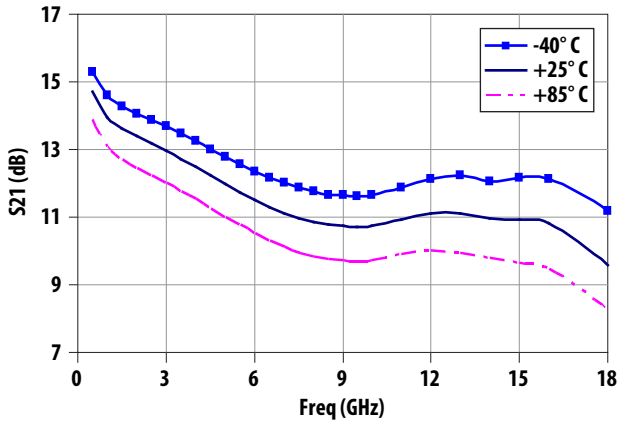


Figure 17. Max Gain ($V_c = 1.8\text{V}$) over Temp

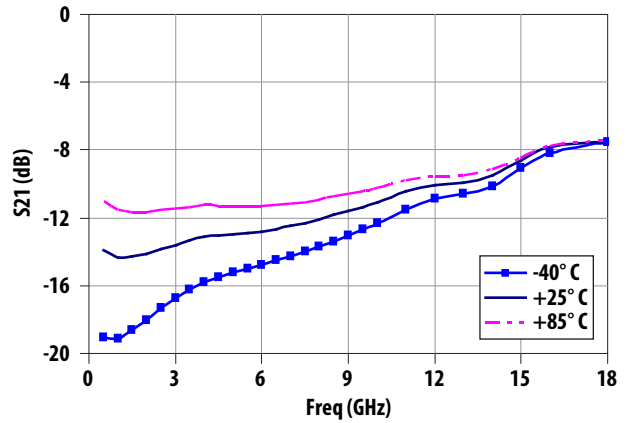


Figure 18. Min. Gain ($V_c = 0.65\text{V}$) over Temp

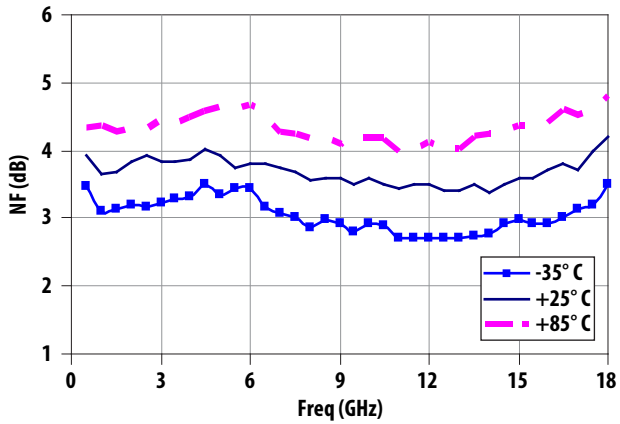


Figure 19. Noise Figure ($V_c = 1.8\text{V}$) over Temp

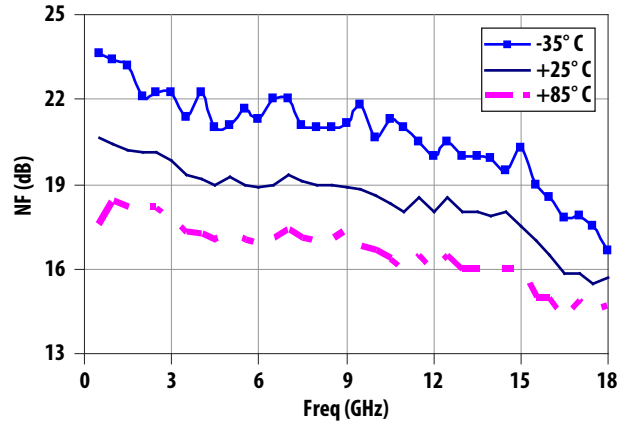


Figure 20. Noise Figure ($V_c = 0.65\text{V}$) over Temp

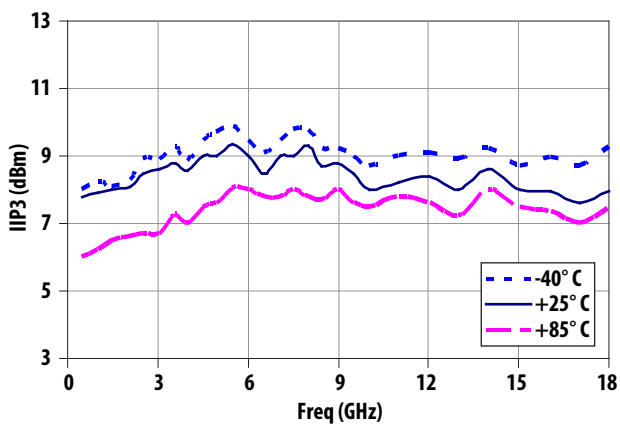


Figure 21. Input IP3 over Temp

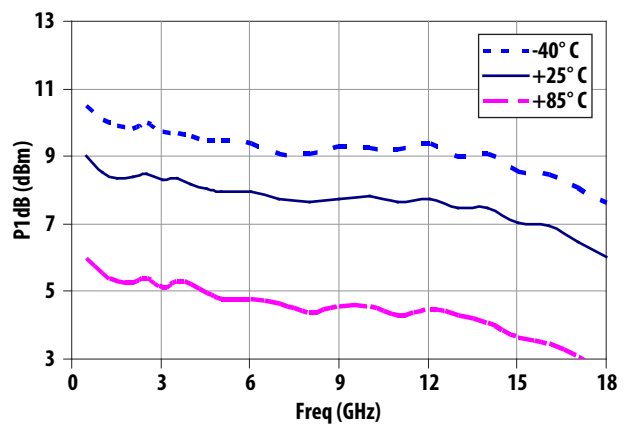


Figure 22. Output P1dB over Temp

Typical Scattering Parameters (Data obtained using GSG probing on substrate, broadband bias-T's, losses calibrated out to the package reference plane.)

Maximum Gain State

$T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{V}$, $V_c = 1.8\text{V}$, $Z_{in} = Z_{out} = 50\ \Omega$

Freq GHz	S11			S21			S12			S22		
	dB	mag	phase	dB	mag	phase	dB	mag	phase	dB	mag	phase
0.1	-5.234	0.547	-36.340	17.088	7.152	-169.066	-34.704	0.018	5.347	-7.950	0.400	-29.145
0.3	-8.205	0.389	-44.110	15.553	5.993	168.608	-37.140	0.014	-33.799	-14.430	0.190	-57.539
0.5	-9.630	0.330	-55.860	14.833	5.517	163.240	-39.576	0.011	-46.674	-17.910	0.127	-57.577
1	-11.674	0.261	-68.772	14.058	5.045	154.656	-45.514	0.005	-61.653	-18.526	0.119	-35.198
1.5	-12.638	0.233	-82.810	13.785	4.890	145.361	-52.396	0.002	-56.465	-18.711	0.116	-37.816
2	-12.716	0.231	-96.505	13.608	4.791	135.797	-58.416	0.001	-27.711	-18.644	0.117	-44.636
2.5	-12.945	0.225	-105.988	13.434	4.696	126.210	-57.721	0.001	22.831	-17.464	0.134	-52.561
3	-12.724	0.231	-117.938	13.253	4.599	116.602	-51.701	0.003	55.942	-17.009	0.141	-60.588
3.5	-12.443	0.239	-129.488	13.079	4.508	107.020	-49.370	0.003	57.247	-16.530	0.149	-67.722
4	-12.086	0.249	-140.327	12.878	4.405	97.488	-47.535	0.004	58.962	-15.950	0.159	-75.685
4.5	-11.781	0.258	-151.034	12.675	4.303	88.039	-46.196	0.005	55.451	-15.499	0.168	-83.369
5	-11.624	0.262	-160.567	12.464	4.199	78.800	-45.193	0.006	54.829	-14.899	0.180	-89.351
5.5	-11.415	0.269	-169.866	12.260	4.102	69.643	-44.152	0.006	54.633	-14.361	0.191	-96.382
6	-11.337	0.271	-179.510	12.054	4.006	60.519	-42.734	0.007	53.880	-13.962	0.200	-102.828
7	-11.460	0.267	162.515	11.657	3.827	42.602	-42.499	0.008	49.735	-13.167	0.220	-113.970
8	-11.751	0.259	147.995	11.367	3.701	24.988	-40.724	0.009	48.393	-12.203	0.245	-124.427
9	-12.472	0.238	133.404	11.060	3.573	7.241	-40.265	0.010	39.885	-11.542	0.265	-134.913
10	-13.635	0.208	121.211	10.846	3.486	-10.571	-40.446	0.010	36.647	-11.010	0.282	-143.067
11	-14.866	0.181	114.429	10.711	3.432	-28.787	-39.094	0.011	35.737	-10.492	0.299	-151.617
12	-16.695	0.146	106.812	10.563	3.374	-47.576	-39.251	0.011	20.424	-10.527	0.298	-158.331
13	-17.096	0.140	95.686	10.455	3.332	-66.978	-39.743	0.010	6.426	-11.103	0.279	-163.704
14	-17.413	0.135	93.664	10.440	3.327	-87.377	-42.853	0.007	3.082	-11.239	0.274	-166.829
15	-16.893	0.143	84.178	10.301	3.274	-109.043	-45.680	0.005	-7.975	-11.493	0.266	-169.735
16	-16.467	0.150	63.202	10.045	3.179	-131.594	-49.897	0.003	-4.888	-11.866	0.255	-166.983
17	-15.945	0.160	37.802	9.750	3.073	-154.810	-55.918	0.002	-52.259	-11.681	0.261	-160.052
18	-15.614	0.166	12.088	9.197	2.883	-179.066	-51.701	0.003	158.277	-10.357	0.304	-158.139
19	-13.752	0.205	-21.118	8.448	2.645	157.015	-44.883	0.006	152.925	-8.966	0.356	-157.243
20	-12.157	0.247	-41.042	7.561	2.388	133.864	-41.310	0.009	154.431	-8.145	0.392	-162.711
21	-10.669	0.293	-63.873	6.683	2.159	111.260	-37.393	0.014	138.895	-7.153	0.439	-169.348
22	-8.874	0.360	-80.568	5.735	1.935	89.380	-36.363	0.015	136.236	-6.840	0.455	-175.654
23	-7.819	0.407	-95.270	4.875	1.753	68.283	-33.231	0.022	129.780	-7.107	0.441	173.963
24	-6.567	0.470	-112.606	4.083	1.600	46.380	-31.972	0.025	123.391	-7.300	0.432	164.987
25	-5.575	0.526	-123.992	3.420	1.483	24.873	-30.117	0.031	117.009	-8.683	0.368	155.499
26	-5.033	0.560	-138.591	2.789	1.379	1.758	-28.730	0.037	106.595	-10.707	0.292	142.046
27	-4.273	0.611	-152.269	2.192	1.287	-22.954	-27.787	0.041	101.488	-15.310	0.172	134.713
28	-3.947	0.635	-167.334	1.493	1.188	-49.141	-26.994	0.045	92.314	-32.041	0.025	144.283
29	-3.541	0.665	176.086	0.621	1.074	-77.446	-25.832	0.051	86.534	-16.851	0.144	-90.456
30	-3.351	0.680	158.427	-0.400	0.955	-106.679	-25.209	0.055	79.495	-9.935	0.319	-100.759

Typical Scattering Parameters (Data obtained using GSG probing on substrate, broadband bias-T's, losses calibrated out to the package reference plane.)

Maximum Gain State

$T_A = 25^\circ\text{C}$, $V_{dd} = 5\text{V}$, $V_c = 0.65\text{V}$, $Z_{in} = Z_{out} = 50\ \Omega$

Freq GHz	S11			S21			S12			S22		
	dB	mag	phase	dB	mag	phase	dB	mag	phase	dB	mag	phase
0.1	-4.384	0.604	-29.869	-12.146	0.247	129.090	-34.657	0.019	-1.087	-8.629	0.370	-52.821
0.3	-6.657	0.465	-45.824	-14.204	0.195	147.959	-37.721	0.013	-29.210	-15.050	0.177	-91.600
0.5	-8.022	0.397	-60.936	-14.780	0.182	147.676	-40.446	0.010	-44.324	-18.294	0.122	-109.111
1	-9.851	0.322	-79.444	-15.244	0.173	138.353	-47.959	0.004	-46.248	-24.837	0.057	-106.341
1.5	-10.291	0.306	-96.760	-15.254	0.173	124.975	-53.152	0.002	4.863	-27.131	0.044	-114.720
2	-9.960	0.318	-112.225	-15.095	0.176	110.896	-49.119	0.004	34.160	-27.535	0.042	-120.614
2.5	-9.789	0.324	-123.981	-14.875	0.180	97.127	-46.745	0.005	38.796	-26.321	0.048	-105.494
3	-9.279	0.344	-136.890	-14.666	0.185	83.680	-44.731	0.006	46.700	-25.368	0.054	-106.252
3.5	-8.838	0.362	-149.098	-14.434	0.190	70.694	-43.223	0.007	39.610	-24.336	0.061	-105.204
4	-8.423	0.379	-160.463	-14.186	0.195	58.511	-41.618	0.008	38.334	-22.878	0.072	-107.122
4.5	-8.112	0.393	-171.556	-13.966	0.200	46.636	-40.819	0.009	35.552	-21.766	0.082	-109.935
5	-7.983	0.399	178.119	-13.727	0.206	35.372	-40.446	0.010	31.845	-20.491	0.095	-110.216
5.5	-7.862	0.405	168.168	-13.498	0.211	24.634	-40.000	0.010	30.148	-19.307	0.108	-113.744
6	-7.896	0.403	157.747	-13.251	0.218	14.151	-39.412	0.011	27.547	-18.496	0.119	-117.260
7	-8.352	0.382	138.626	-12.765	0.230	-6.012	-39.332	0.011	22.649	-16.624	0.148	-123.666
8	-9.484	0.336	121.545	-12.174	0.246	-25.240	-38.344	0.012	20.228	-15.006	0.178	-131.066
9	-11.724	0.259	108.205	-11.457	0.267	-45.069	-37.458	0.013	10.631	-13.630	0.208	-139.041
10	-14.914	0.180	109.544	-10.704	0.292	-65.979	-37.329	0.014	-0.050	-12.634	0.234	-146.650
11	-14.746	0.183	133.101	-9.990	0.317	-87.815	-37.016	0.014	-6.566	-11.842	0.256	-153.905
12	-11.411	0.269	133.477	-9.304	0.343	-110.934	-36.954	0.014	-29.419	-11.418	0.269	-160.153
13	-8.709	0.367	113.491	-8.754	0.365	-135.002	-37.523	0.013	-52.510	-11.545	0.265	-165.869
14	-7.250	0.434	92.561	-8.327	0.383	-159.201	-39.914	0.010	-77.826	-11.764	0.258	-170.850
15	-6.417	0.478	70.306	-7.950	0.400	176.550	-40.355	0.010	-111.180	-11.941	0.253	-174.141
16	-6.028	0.500	45.905	-7.654	0.414	151.174	-40.355	0.010	-145.319	-12.206	0.245	-172.586
17	-5.647	0.522	21.999	-7.498	0.422	125.597	-39.914	0.010	-169.517	-12.385	0.240	-167.794
18	-5.552	0.528	-1.777	-7.570	0.418	99.059	-37.523	0.013	169.891	-11.299	0.272	-164.225
19	-5.004	0.562	-26.985	-8.013	0.398	72.637	-36.138	0.016	155.878	-9.984	0.317	-161.776
20	-4.614	0.588	-47.372	-8.759	0.365	47.014	-35.041	0.018	150.938	-9.134	0.349	-167.187
21	-4.252	0.613	-69.196	-9.651	0.329	22.400	-32.217	0.025	137.411	-8.097	0.394	-175.258
22	-3.650	0.657	-86.503	-10.672	0.293	-1.960	-31.437	0.027	130.598	-8.161	0.391	177.319
23	-3.451	0.672	-103.378	-11.948	0.253	-25.748	-29.422	0.034	121.759	-8.981	0.356	164.378
24	-3.045	0.704	-121.052	-13.195	0.219	-51.026	-28.683	0.037	110.392	-10.223	0.308	155.184
25	-2.790	0.725	-133.752	-14.512	0.188	-76.900	-27.723	0.041	101.985	-13.846	0.203	148.226
26	-2.787	0.726	-148.672	-15.918	0.160	-105.090	-27.033	0.045	90.855	-20.491	0.095	149.827
27	-2.648	0.737	-163.119	-17.127	0.139	-136.314	-26.878	0.045	85.725	-20.696	0.092	-122.188
28	-2.761	0.728	-178.128	-18.366	0.121	-167.459	-26.651	0.047	77.935	-13.560	0.210	-108.378
29	-2.874	0.718	165.731	-19.062	0.111	160.383	-25.934	0.051	73.541	-9.709	0.327	-115.177
30	-3.145	0.696	148.147	-19.601	0.105	131.274	-25.564	0.053	70.374	-7.404	0.426	-122.966

VMMK-3503 Applications and Usage Information

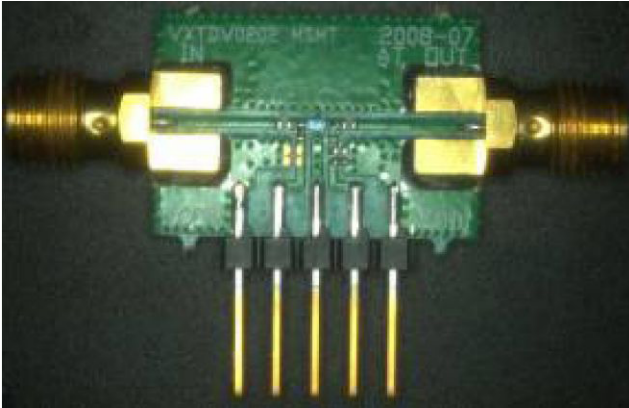


Figure 23. Evaluation/Test Board (available to qualified customers upon request)

Biasing and Operation

The VMMK-3503 is biased with a positive supply connected to the output pin Vd through an external user supplied bias decoupling network. Nominal current draw is 59 mA from a 5 V power supply. A typical biasing scheme is shown in Figure 23. Maximum gain occurs when Vc is 1.8 V and minimum gain occurs with Vc set to 0.65 V.

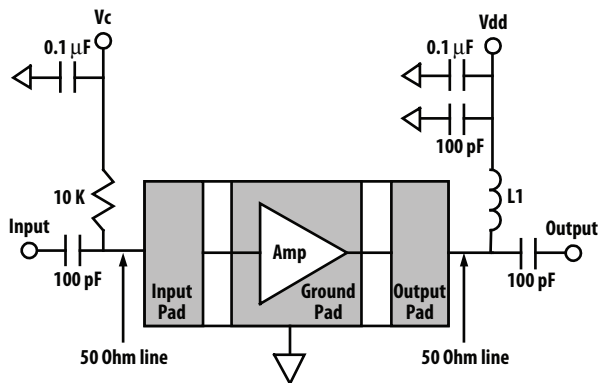


Figure 24. Example demonstration circuit of VMMK-3503 for broadband operation (RF choke value selected for best performance at 12 GHz).

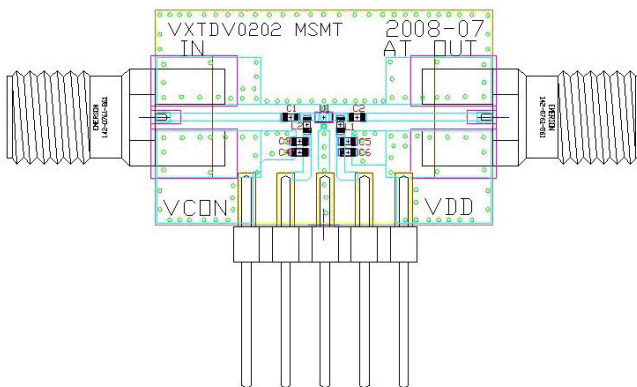


Figure 25. Biasing the VMMK-3503

Table 4. VMMK-3503 Demo Board BOM

Component	Value
DUT	VMMK-3503
C1	100 pF
C2	100 pF
R1	10 KOhms
C5	0.1 μ F
C6	100 pF
L1	2 nH

A layout of a typical demo board is shown in Figure 25. The demo board uses small 0402 style surface mount components. Due to the broad bandwidth of the VMMK-3503 devising a bias decoupling network to work well over the entire 0.5 to 18 GHz frequency range will be a challenge.

Conical wound broad band inductors will work well but may be pricy. The demo board uses a 2.2 nH output inductor which provides good bandwidth from about a 1 GHz to beyond 6 GHz. The input and output blocking capacitors are 100 pF.

Typically a passive component company like Murata does not specify S parameters at frequencies higher than 5 or 6 GHz for larger values of inductance making it difficult to properly simulate amplifier performance at higher frequencies. It has been observed that the Murata LQW15AN series of 0402 inductors actually works quite well above their normally specified frequency.

Another scheme for increasing the bandwidth would be to install two small chip inductors in series. A smaller value would favor the higher frequencies while the larger value will work better at low frequencies. Putting a few ohms of resistance in series with the inductors will also tend to smooth out the response by minimizing resonances in the bias decoupling networks.

The parallel combination of the 100 pF and 0.1 μ F capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be generated when multiple in-band signals are injected into any amplifier.

The 10K ohm resistor at the input provides a reasonably wide bandwidth way of injecting Vc at the input to the device without adversely affecting RF performance.

S Parameter Measurements

The S parameters are measured on a 300 μm G-S-G (ground signal ground) printed circuit board substrate. Calibration is achieved with a series of through, short and open substrates from which an accurate set of S parameters is created. The test board is 0.016 inch thickness RO4350. Grounding of the device is achieved with a single plated through hole directly under the device. The effect of this plated through hole is included in the S parameter measurements and is difficult to de-embed accurately. Since the maximum recommended printed circuit board thickness is nominally 0.020 inch, then the nominal effect of printed circuit board grounding can be considered to have already been included the published S parameters.

Package and Assembly Note

For detailed description of the device package, handling and assembly, please refer to Application Note 5378.

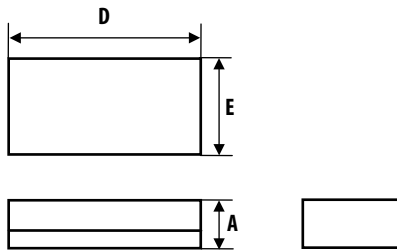
ESD Precautions

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Ordering Information

Part Number	Devices Per Container	Container
VMMK-3503-BLKG	100	Antistatic Bag
VMMK-3503-TR1G	5000	7" Reel

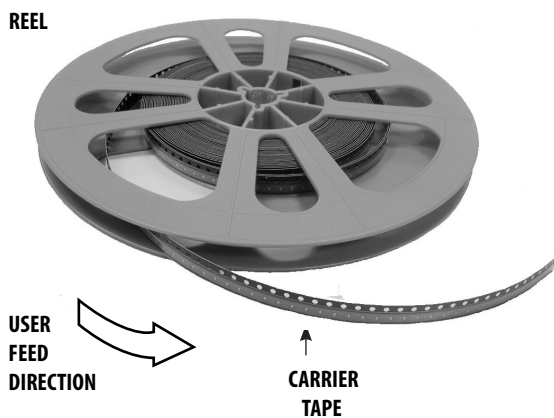
Package Dimension Outline



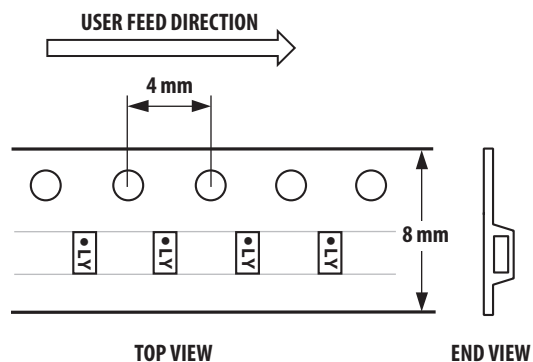
Dimensions Symbol	Min (mm)	Max (mm)
E	0.500	0.585
D	1.004	1.085
A	0.225	0.275

Note:
All dimensions are in mm

Reel Orientation

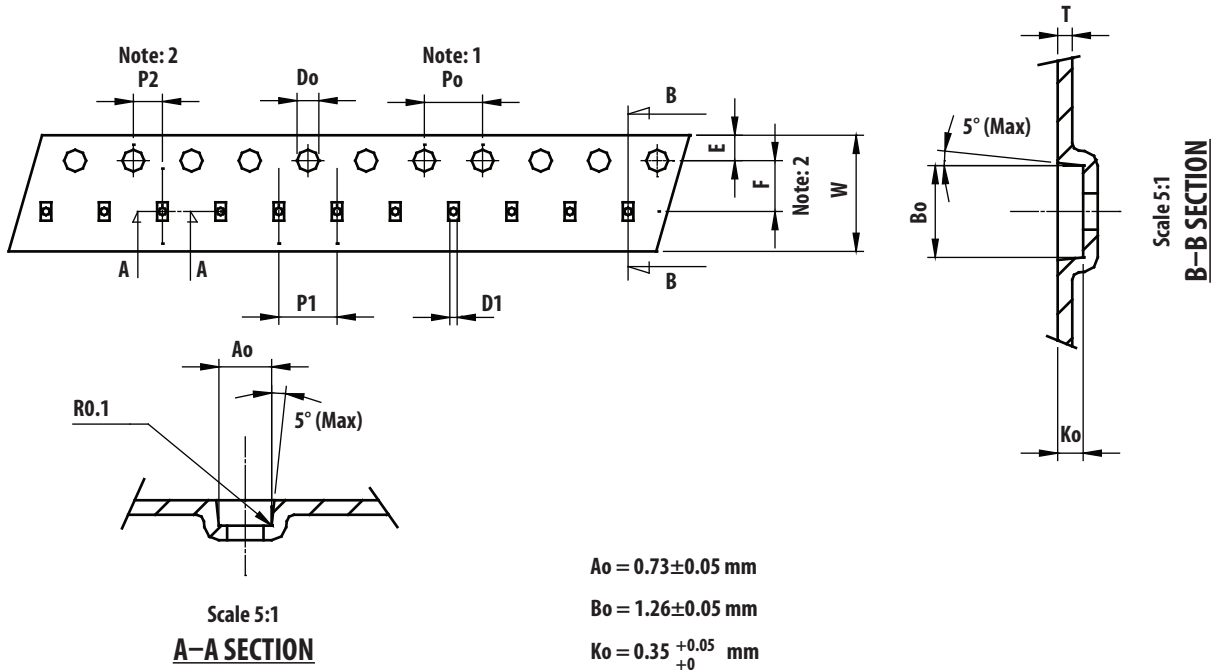


Device Orientation



Notes:
"L" = Device Code
"Y" = Month Code

Tape Dimensions



Unit: mm

Symbol	Spec.
K1	-
Po	4.0 ± 0.10
P1	4.0 ± 0.10
P2	2.0 ± 0.05
Do	1.55 ± 0.05
D1	0.5 ± 0.05
E	1.75 ± 0.10
F	3.50 ± 0.05
10Po	40.0 ± 0.10
W	8.0 ± 0.20
T	0.20 ± 0.02

Notice:

- 10 Sprocket hole pitch cumulative tolerance is $\pm 0.1 \text{ mm}$.
- Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
- A_o & B_o measured on a plane 0.3 mm above the bottom of the pocket to top surface of the carrier.
- K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- Carrier camber shall be not than 1 m per 100 mm through a length of 250 mm.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries. Data subject to change. Copyright © 2005-2012 Avago Technologies. All rights reserved. AV02-2918EN - December 26, 2012

AVAGO
TECHNOLOGIES

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View VMMK-3503-TR2G on WIN SOURCE](#)

 [Broadcom Limited](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management