



# CHY100 ChiPhy™ Family



## Charger Interface Physical Layer IC

### Product Highlights

- Fully supports Quick Charge 2.0 specification
  - Class A: 5 V, 9 V, and 12 V output voltage
  - Class B: 5 V, 9 V, 12 V, and 20 V output voltage
- USB battery charging specification revision 1.2 compatible
  - Automatic USB DCP shorting D+ to D- line
  - Default 5 V mode operation
- Supports TOPSwitch and TinySwitch
- Very low power consumption
  - Below 1 mW at 5 V output
- Fail safe operation
  - Adjacent pin-to-pin short-circuit fault
  - Open circuit pin fault

### Typical Applications

- Battery chargers for smart phones, tablets, netbooks, digital cameras, and bluetooth accessories
- USB power output ports

### Description

CHY100 is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 2.0 specification. It incorporates all necessary functions to add Quick Charge 2.0 capability to Power Integrations' switcher ICs such as TOPSwitch or TinySwitch and other solutions employing traditional feedback schemes.

CHY100 supports the full output voltage range of either Class A or Class B. Optionally Class B can be inhibited for protecting the battery charger from accidental damage.

CHY100 automatically detects whether a connected Powered Device (PD) is Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 is detected the CHY100 disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

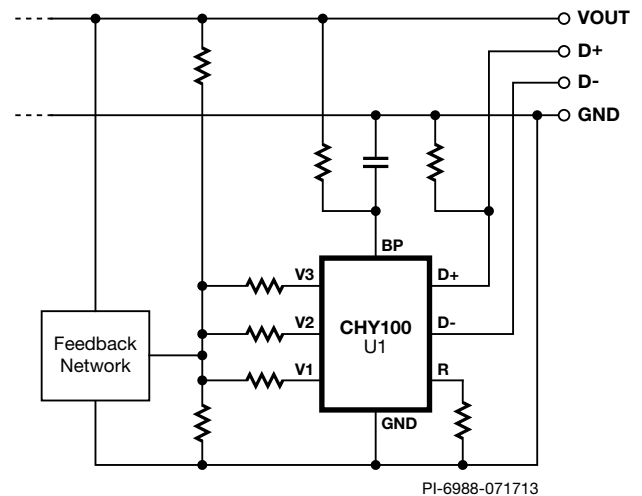
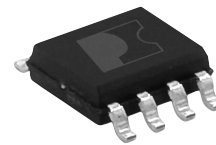


Figure 1. Typical Application Schematic.



SO-8 (D Package)

Figure 2. Package Option.

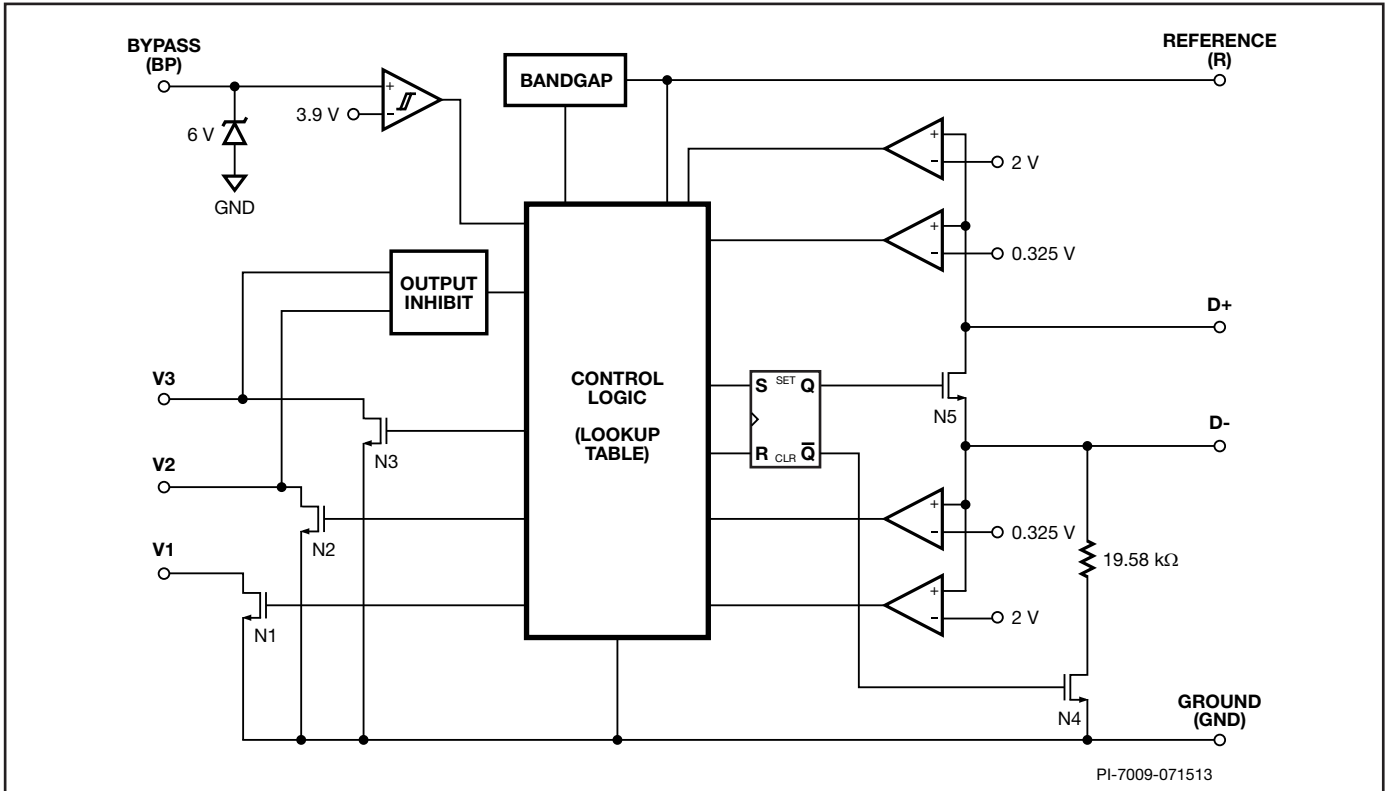


Figure 3. Functional Block Diagram.

## Pin Functional Description

### GROUND (GND) Pin

Ground.

### V1 Pin

Open Drain input of output voltage adjustment switch. Active for 9 V, 12 V, and 20 V output setting.

### V2 Pin

Open Drain input of output voltage adjustment switch. Active for 12 V, and 20 V output setting.

### V3 Pin

Open Drain input of output voltage adjustment switch. Active for 20 V output setting.

### BYPASS (BP) Pin

Connection point for an external bypass capacitor for the internally generated supply voltage.

### REFERENCE (R) Pin

Connected to internal band-gap reference. Provides reference current through connected resistor.

### DATA LINE D+ Pin

USB D+ data line input.

### DATA LINE D- Pin

USB D- data line input.

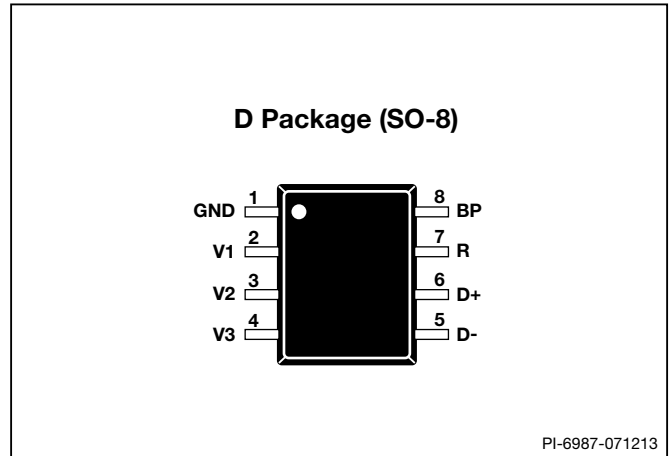


Figure 4. Pin Configuration.



## Absolute Maximum Ratings

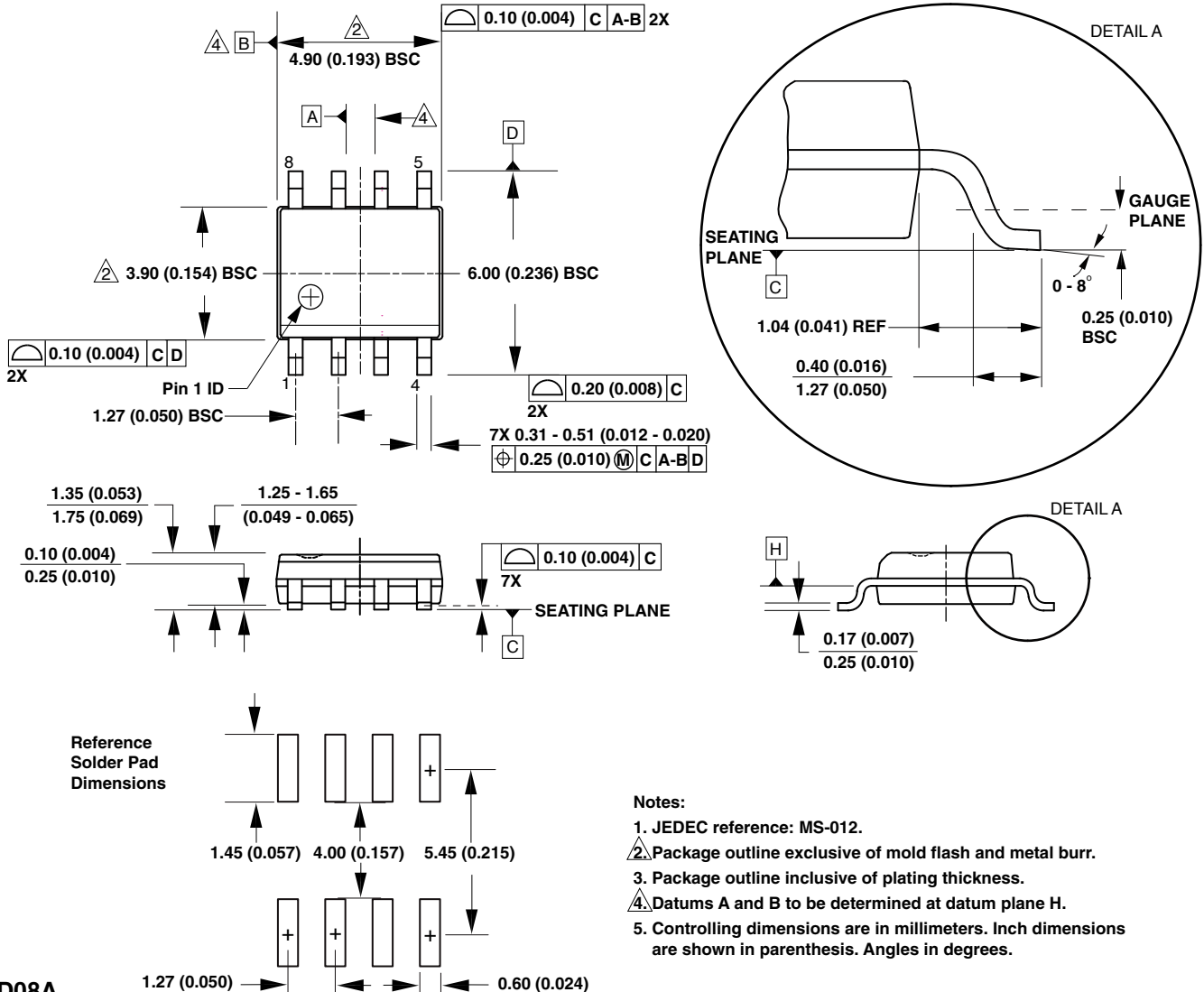
BYPASS Pin Voltage	-0.3 to 9 V	Operating Junction Temperature	-40 °C to +150 °C
REFERENCE Pin Voltage	-0.3 to 9 V	Operating Ambient Temperature	-40 °C to 105 °C
V1/V2/V3 Pin Voltage	-0.3 to 9 V	Storage Temperature	-65 °C to 150 °C
D+/D- Pin Voltage	-0.3 to 5 V	Lead Temperature <sup>(1)</sup>	260 °C
BYPASS Pin Current	25 mA	Notes:	
V1/V2/V3 Pin Current	0.5 mA	1. 1/16 in. from case for 5 seconds.	
D+/D- Pin Current	1 mA		

Parameter	Symbol	Conditions SOURCE = 0 V; T <sub>J</sub> = -20 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
<b>Supply, Reference and Protection Functions</b>						
<b>BYPASS Pin Voltage</b>	V <sub>BP</sub>		4	5	6	V
<b>Power-Up Reset Threshold Voltage</b>	V <sub>BP(RESET)</sub>		2.0		3.9	V
<b>BYPASS Pin Source Current</b>	I <sub>BPSC</sub>	V <sub>BP</sub> = 4.3 V, T <sub>J</sub> = 25 °C N1 = N2 = N3 = Off			135	μA
<b>BYPASS Pin Shunt Voltage</b>	V <sub>BP(SHUNT)</sub>	I <sub>BP</sub> = 3 mA	5.7	6	6.3	V
<b>REFERENCE Pin Voltage</b>	V <sub>R</sub>		1.18	1.23	1.28	V
<b>HVDCP Functions</b>						
<b>Data Detect Voltage</b>	V <sub>DAT(REF)</sub>		0.25	0.325	0.4	V
<b>Output Voltage Selection Reference</b>	V <sub>SEL(REF)</sub>		1.8	2	2.2	V
<b>12 V / 20 V Output Inhibit Threshold</b>	V <sub>INH</sub>		V <sub>BP</sub> - 0.6			V
<b>Data Lines Short-Circuit Delay</b>	T <sub>DAT(SHORT)</sub>	V <sub>OUT</sub> ≥ 0.8 V See Figure 5		10	20	ms
<b>D+ High Glitch Filter Time</b>	T <sub>GLITCH(BC) DONE</sub>		1000	1250	1500	ms
<b>Output Voltage Glitch Filter Time</b>	T <sub>GLITCH(V) CHANGE</sub>		20	40	60	ms
<b>D- Pull-Down Resistance</b>	R <sub>DM(DWN)</sub>		14.25	19.53	24.5	kΩ
<b>Switch N1 On-Resistance</b>	R <sub>DS(ON)N1</sub>	I <sub>N1</sub> = 200 μA			300	Ω
<b>Switch N2 On-Resistance</b>	R <sub>DS(ON)N2</sub>	I <sub>N2</sub> = 200 μA			300	Ω
<b>Switch N3 On-Resistance</b>	R <sub>DS(ON)N3</sub>	I <sub>N3</sub> = 200 μA			300	Ω
<b>Switch N4 On-Resistance</b>	R <sub>DS(ON)N4</sub>	I <sub>N4</sub> = 200 μA			300	Ω
<b>Switch N5 On-Resistance</b>	R <sub>DS(ON)N5</sub>	I <sub>N5</sub> = 200 μA, V <sub>(D+)</sub> ≤ 3.6 V		20	40	Ω
<b>Data Line Capacitance</b>	C <sub>DCP(PWR)</sub>	See Note A			1	nF

NOTES:

A. Guaranteed by design. Not tested in production.

SO-8 (D Package)

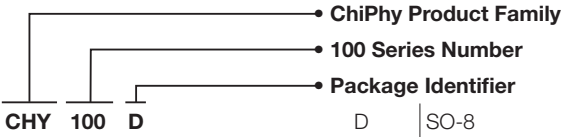


- Notes:**
- 1. JEDEC reference: MS-012.
  - 2. Package outline exclusive of mold flash and metal burr.
  - 3. Package outline inclusive of plating thickness.
  - 4. Datums A and B to be determined at datum plane H.
  - 5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D08A

PI-5615-041210

Part Ordering Information



Revision	Notes	Date
A	Initial Release.	07/13
B	Extended Ambient Temperature to -40 °C.	01/14
C	Added Note for Class A Charger on page 3.	03/14

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## Power Integrations Worldwide Sales Support Locations

### World Headquarters

5245 Hellyer Avenue  
San Jose, CA 95138, USA.  
Main: +1-408-414-9200  
Customer Service:  
Phone: +1-408-414-9665  
Fax: +1-408-414-9765  
e-mail: [usasales@powerint.com](mailto:usasales@powerint.com)

### China (Shanghai)

Rm 2410, Charity Plaza, No. 88  
North Caoxi Road  
Shanghai, PRC 200030  
Phone: +86-21-6354-6323  
Fax: +86-21-6354-6325  
e-mail: [chinasales@powerint.com](mailto:chinasales@powerint.com)

### China (ShenZhen)

3rd Floor, Block A,  
Zhongtuo International Business  
Center, No. 1061, Xiang Mei Rd,  
FuTian District, ShenZhen,  
China, 518040  
Phone: +86-755-8379-3243  
Fax: +86-755-8379-5828  
e-mail: [chinasales@powerint.com](mailto:chinasales@powerint.com)

### Germany

Lindwurmstrasse 114  
80337 Munich  
Germany  
Phone: +49-895-527-39110  
Fax: +49-895-527-39200  
e-mail: [eurosales@powerint.com](mailto:eurosales@powerint.com)

### India

#1, 14th Main Road  
Vasanthanagar  
Bangalore-560052 India  
Phone: +91-80-4113-8020  
Fax: +91-80-4113-8023  
e-mail: [indiasales@powerint.com](mailto:indiasales@powerint.com)

### Italy

Via Milanese 20, 3rd. Fl.  
20099 Sesto San Giovanni (MI)  
Italy  
Phone: +39-024-550-8701  
Fax: +39-028-928-6009  
e-mail: [eurosales@powerint.com](mailto:eurosales@powerint.com)

### Japan

Kosei Dai-3 Bldg.  
2-12-11, Shin-Yokohama,  
Kohoku-ku  
Yokohama-shi Kanagawan  
222-0033 Japan  
Phone: +81-45-471-1021  
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### Korea

RM 602, 6FL  
Korea City Air Terminal B/D, 159-6  
Samsung-Dong, Kangnam-Gu,  
Seoul, 135-728, Korea  
Phone: +82-2-2016-6610  
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e-mail: [koreasales@powerint.com](mailto:koreasales@powerint.com)

### Singapore

51 Newton Road  
#19-01/05 Goldhill Plaza  
Singapore, 308900  
Phone: +65-6358-2160  
Fax: +65-6358-2015  
e-mail: [singaporesales@powerint.com](mailto:singaporesales@powerint.com)

### Taiwan

5F, No. 318, Nei Hu Rd., Sec. 1  
Nei Hu Dist.  
Taipei 11493, Taiwan R.O.C.  
Phone: +886-2-2659-4570  
Fax: +886-2-2659-4550  
e-mail: [taiwansales@powerint.com](mailto:taiwansales@powerint.com)

### Europe HQ

1st Floor, St. James's House  
East Street, Farnham  
Surrey GU9 7TJ  
United Kingdom  
Phone: +44 (0) 1252-730-141  
Fax: +44 (0) 1252-727-689  
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