



THE DATASHEET OF CHY100D



CHY100 ChiPhy™ Family



Charger Interface Physical Layer IC

Product Highlights

- Fully supports Quick Charge 2.0 specification
 - Class A: 5 V, 9 V, and 12 V output voltage
 - Class B: 5 V, 9 V, 12 V, and 20 V output voltage
- USB battery charging specification revision 1.2 compatible
 - Automatic USB DCP shorting D+ to D- line
 - Default 5 V mode operation
- Supports TOPSwitch and TinySwitch
- Very low power consumption
 - Below 1 mW at 5 V output
- Fail safe operation
 - Adjacent pin-to-pin short-circuit fault
 - Open circuit pin fault

Typical Applications

- Battery chargers for smart phones, tablets, netbooks, digital cameras, and bluetooth accessories
- USB power output ports

Description

CHY100 is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 2.0 specification. It incorporates all necessary functions to add Quick Charge 2.0 capability to Power Integrations' switcher ICs such as TOPSwitch or TinySwitch and other solutions employing traditional feedback schemes.

CHY100 supports the full output voltage range of either Class A or Class B. Optionally Class B can be inhibited for protecting the battery charger from accidental damage.

CHY100 automatically detects whether a connected Powered Device (PD) is Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 is detected the CHY100 disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

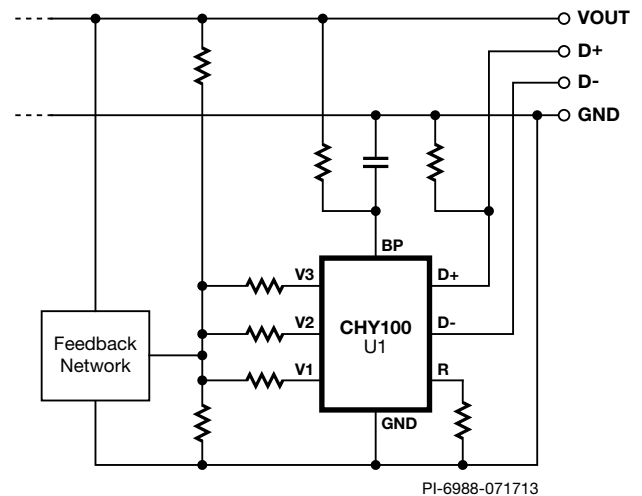
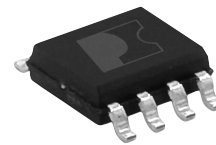


Figure 1. Typical Application Schematic.



SO-8 (D Package)

Figure 2. Package Option.

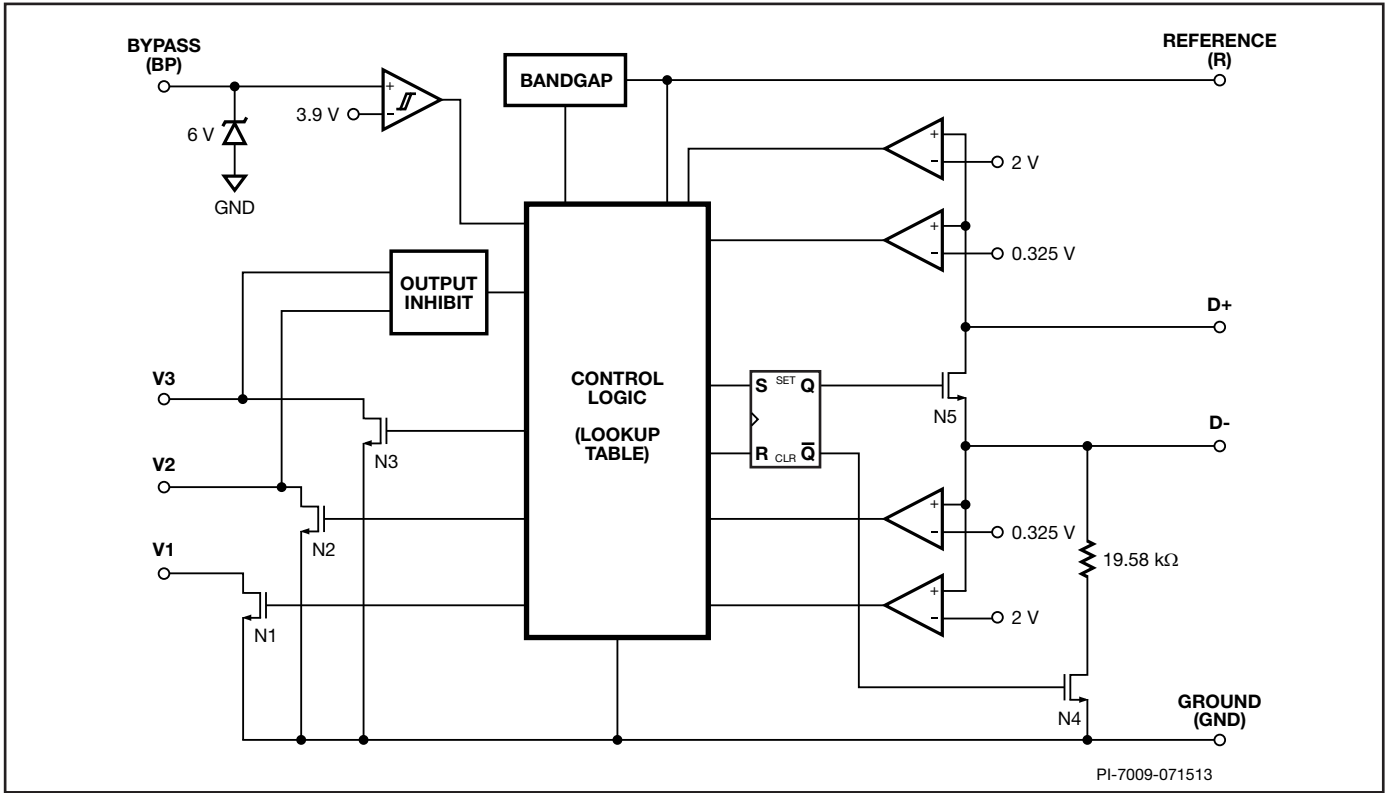


Figure 3. Functional Block Diagram.

Pin Functional Description

GROUND (GND) Pin

Ground.

V1 Pin

Open Drain input of output voltage adjustment switch. Active for 9 V, 12 V, and 20 V output setting.

V2 Pin

Open Drain input of output voltage adjustment switch. Active for 12 V, and 20 V output setting.

V3 Pin

Open Drain input of output voltage adjustment switch. Active for 20 V output setting.

BYPASS (BP) Pin

Connection point for an external bypass capacitor for the internally generated supply voltage.

REFERENCE (R) Pin

Connected to internal band-gap reference. Provides reference current through connected resistor.

DATA LINE D+ Pin

USB D+ data line input.

DATA LINE D- Pin

USB D- data line input.

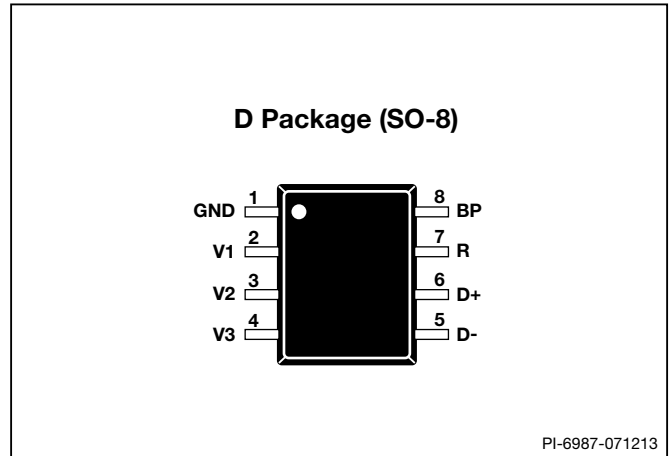


Figure 4. Pin Configuration.

Absolute Maximum Ratings

BYPASS Pin Voltage	-0.3 to 9 V	Operating Junction Temperature.....	-40 °C to +150 °C
REFERENCE Pin Voltage	-0.3 to 9 V	Operating Ambient Temperature.....	-40 °C to 105 °C
V1/V2/V3 Pin Voltage	-0.3 to 9 V	Storage Temperature	-65 °C to 150 °C
D+/D- Pin Voltage	-0.3 to 5 V	Lead Temperature ⁽¹⁾	260 °C
BYPASS Pin Current	25 mA	Notes:	
V1/V2/V3 Pin Current	0.5 mA	1. 1/16 in. from case for 5 seconds.	
D+/D- Pin Current	1 mA		

Parameter	Symbol	Conditions SOURCE = 0 V; T _J = -20 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Supply, Reference and Protection Functions						
BYPASS Pin Voltage	V _{BP}		4	5	6	V
Power-Up Reset Threshold Voltage	V _{BP(RESET)}		2.0		3.9	V
BYPASS Pin Source Current	I _{BPSC}	V _{BP} = 4.3 V, T _J = 25 °C N1 = N2 = N3 = Off			135	μA
BYPASS Pin Shunt Voltage	V _{BP(SHUNT)}	I _{BP} = 3 mA	5.7	6	6.3	V
REFERENCE Pin Voltage	V _R		1.18	1.23	1.28	V
HVDCP Functions						
Data Detect Voltage	V _{DAT(REF)}		0.25	0.325	0.4	V
Output Voltage Selection Reference	V _{SEL(REF)}		1.8	2	2.2	V
12 V / 20 V Output Inhibit Threshold	V _{INH}		V _{BP} - 0.6			V
Data Lines Short-Circuit Delay	T _{DAT(SHORT)}	V _{OUT} ≥ 0.8 V See Figure 5		10	20	ms
D+ High Glitch Filter Time	T _{GLITCH(BC) DONE}		1000	1250	1500	ms
Output Voltage Glitch Filter Time	T _{GLITCH(V) CHANGE}		20	40	60	ms
D- Pull-Down Resistance	R _{DM(DWN)}		14.25	19.53	24.5	kΩ
Switch N1 On-Resistance	R _{DS(ON)N1}	I _{N1} = 200 μA			300	Ω
Switch N2 On-Resistance	R _{DS(ON)N2}	I _{N2} = 200 μA			300	Ω
Switch N3 On-Resistance	R _{DS(ON)N3}	I _{N3} = 200 μA			300	Ω
Switch N4 On-Resistance	R _{DS(ON)N4}	I _{N4} = 200 μA			300	Ω
Switch N5 On-Resistance	R _{DS(ON)N5}	I _{N5} = 200 μA, V _(D+) ≤ 3.6 V		20	40	Ω
Data Line Capacitance	C _{DCP(PWR)}	See Note A			1	nF

NOTES:

A. Guaranteed by design. Not tested in production.

Revision	Notes	Date
A	Initial Release.	07/13
B	Extended Ambient Temperature to -40 °C.	01/14
C	Added Note for Class A Charger on page 3.	03/14

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