THE DATASHEET OF

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NXP Semiconductors
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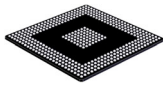
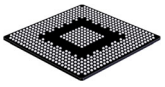
RoHS

MPC5674F

MPC5674F Microcontroller Data Sheet

Covers: MPC5674F and MPC5673F


TEPBGA–416
27mm x 27mm


TEPBGA–516
27mm x 27mm

TEPBGA–324
23mm x 23mm

- Dual issue, 32-bit CPU core complex (e200z7)
  - Compliant with the Power Architecture® embedded category
  - 16 KB I-Cache and 16 KB D-Cache
  - Includes an instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - Includes signal processing extension (SPE2) instruction support for digital signal processing (DSP) and single-precision floating point operations
- 4 MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 256 KB on-chip general-purpose SRAM including 32 KB of standby RAM
- Two direct memory access controller (eDMA2) blocks
  - One supporting 64 channels
  - One supporting 32 channels
- Interrupt controller (INTC)
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- External bus interface (EBI) for calibration and application development (not available on all packages)
- System integration unit (SIU)
- Error correction status module (ECSM)
- Boot assist module (BAM) supports serial bootload via CAN or SCI
- Two second-generation enhanced time processor units (eTPU2) that share code and data RAM.
  - 32 standard channels per eTPU2
  - 24 KB code RAM
  - 6 KB parameter (data) RAM
- Enhanced modular input output system supporting 32 unified channels (eMIOS) with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Four enhanced queued analog-to-digital converters (eQADC)
  - Support for 64 analog channels
  - Includes one absolute reference ADC channel
  - Includes eight decimation filters
- Four deserial serial peripheral interface (DSPI) modules
- Three enhanced serial communication interface (eSCI) modules
- Four controller area network (FlexCAN) modules
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003/5001-2008 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller regulates supply voltage down to 1.2 V for core logic

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

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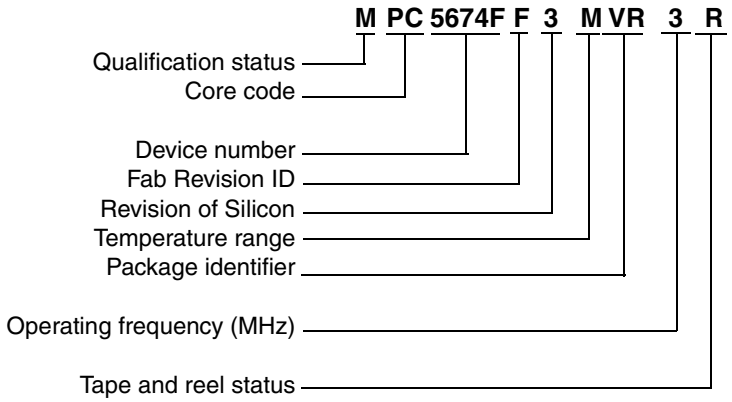
1 Ordering Information

1.1 Orderable Parts

Figure 1 and Table 1 describe and list the orderable part numbers for the MPC5674F.

Note: Not all options are available on all devices. Refer to Table 1.



Temperature Range
M = –40 °C to 125 °C

Package Identifier
VZ = 324 BGA Pb-free
VR = 416 BGA Pb-free
VY = 516 BGA Pb-free
VV = 516 BGA SnPb

Operating Frequency
2 = 200 MHz
3 = 264 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Fab and Mask Indicator
F = ATMC Fab
K = TSMC Fab
A = ATMC Fab or TSMC Fab
Second digit usually differentiate mask rev

Qualification Status
P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Revision of Silicon
3 = Rev 3 (ATMC)
0 = Rev 0 (TSMC14)

Figure 1. MPC5674F Orderable Part Number Description

Table 1. Orderable Part Numbers

NXP Part Number	Package Description	Speed (MHz)[1]		Operating Temperature[2]	
		Nominal	Max[3] (f_{MAX})	Min (T_L)	Max (T_H)
SPC5674FK0MVR3	416 PBGA, no EBI, Pb-free	264	270	–40 °C	125 °C
SPC5674FK0MVY3	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5674FK0MVV3R	516 PBGA, w/EBI, SnPb	264	270	–40 °C	125 °C
SPC5674FK0MVV3	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C
SPC5674FK0MVY3R	516 PBGA, w/EBI, Pb-free	264	270	–40 °C	125 °C
SPC5673FK0MVR2R	416 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FK0MVR2	416 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FK0MVV2R	324 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FK0MVV2	324 PBGA, no EBI, Pb-free	200	200	–40 °C	125 °C
SPC5673FF3MVR2	416 PBGA, no EBI, Pb-free	200	200	-40°C	125 °C
SPC5673FF3MVR3	416 PBGA, no EBI, Pb-free	200	200	-40°C	125 °C

Table 1. Orderable Part Numbers (continued)

NXP Part Number	Package Description	Speed (MHz)[1]		Operating Temperature[2]	
		Nominal	Max[3] (f_{MAX})	Min (T_L)	Max (T_H)
SPC5673FF3MVV2	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C
SPC5673FF3MVY2	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C
SPC5674FF3MVY3	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C
SPC5674FAMVR3	416 PBGA, no EBI, Pb-free	200	200	-40°C	125 °C
SPC5674FAMVY3	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C
SPC5674FF3MVR3	416 PBGA, no EBI, Pb-free	200	200	-40°C	125 °C
SPC5674FF3MVV3	516 PBGA, w/EBI, SnPb	264	200	–40 °C	125 °C

1 For the operating mode frequency of various blocks on the device, see Table 28.

2 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

3 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

1.2 MPC567xF Family Differences

Table 2 lists the differences between the MPC567xF devices. Refer to the *MPC5674F Reference Manual* for a full feature list and comparison.

Table 2. MPC567xF Family Differences

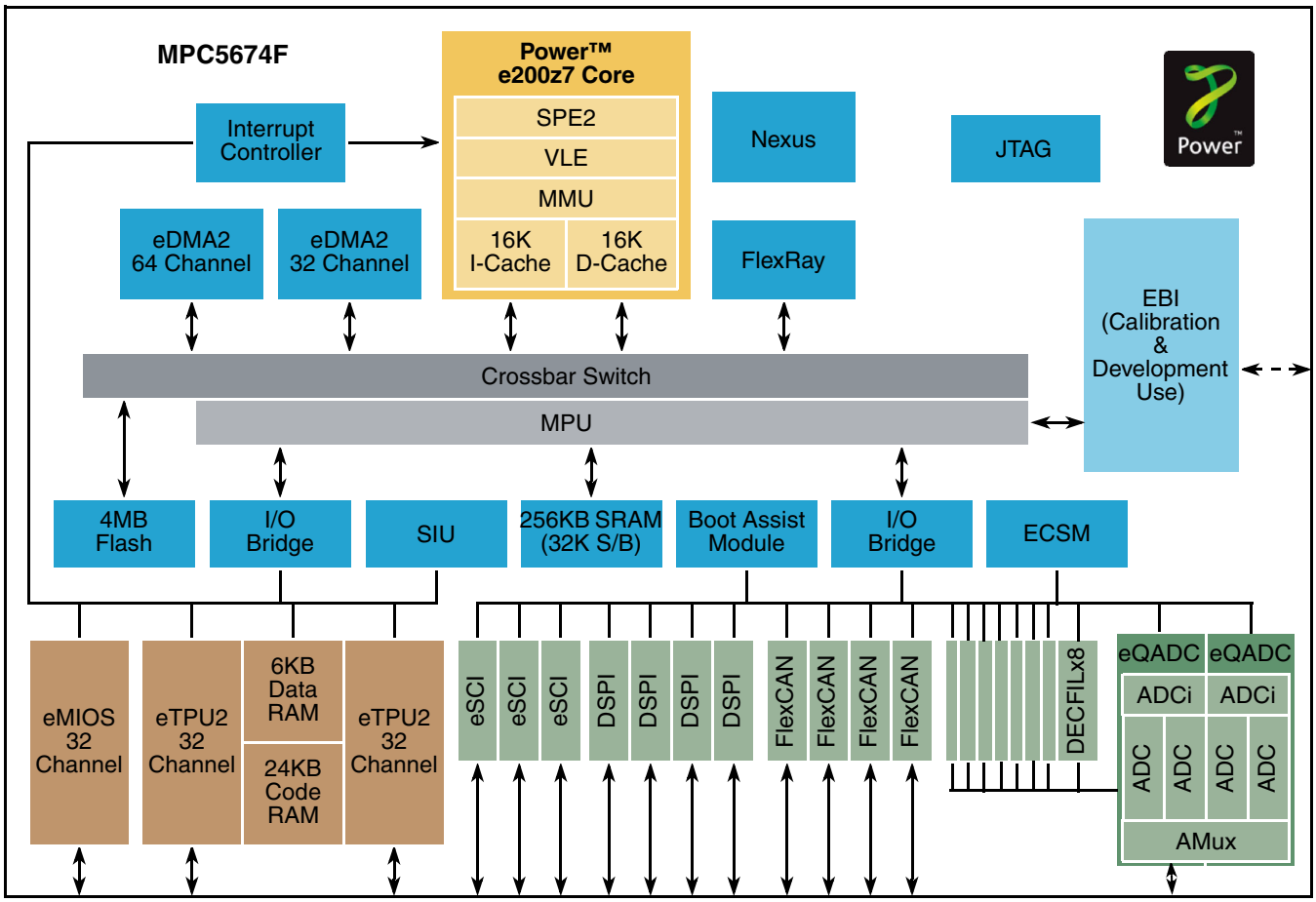
Feature	MPC5674F	MPC5674F	MPC5673F	MPC5673F
Package	416 BGA 516 BGA	324 BGA	416 BGA 516 BGA	324 BGA
Flash	4 MB	4 MB	3 MB	3 MB
SRAM	256 KB	256 KB	192 KB	192 KB
External bus	Yes (516 BGA only)	No	Yes (516 BGA only)	No
Serial	3	2	3	2
eSCI_A	Yes	Yes	Yes	Yes
eSCI_B	Yes	Yes	Yes	Yes
eSCI_C	Yes	No	Yes	No
SPI	4	3	4	3
DSPI_A	Yes	No	Yes	No
DSPI_B	Yes	Yes	Yes	Yes
DSPI_C	Yes	Yes	Yes	Yes
DSPI_D	Yes	Yes	Yes	Yes
eMIOS	32 channel	22 channel	32 channel	22 channel
eTPU2	64 channel	47 channel	64 channel	47 channel
eTPU_A	Yes (32 ch)	Yes (26 ch)	Yes	Yes (26 ch)
eTPU_B	Yes (32 ch)	Yes (21 ch, no TCRCLK)	Yes	Yes (21 ch, no TCRCLK)
ADC	64 channel	48 channel	64 channel	48 channel
eQADC_A	Yes (64 ch)[1]	Yes (24 ch)	Yes (64 ch)[1]	Yes (24 ch)
eQADC_B		Yes (24 ch)		Yes (24 ch)

1 There are are two pairs of 24 channels plus 16 shared channels. This gives 64 channels total: 40 per ADC (since 16 are shared).

2 MPC5674F Blocks

2.1 Block Diagram

Figure 2 shows a top-level block diagram of the MPC5674F device.



LEGEND

ADC	– Analog to digital convertor	**eSCI**	– Enhanced serial communications interface
ADCi	– ADC interface	**eTPU2**	– Enhanced time processing unit 2
AMux	– Analog multiplexer	**FlexCAN**	– Controller area network
DECFIL	– Decimation filter	**MMU**	– Memory management unit
DSPI	– Deserial/serial peripheral interface	**MPU**	– Memory protection unit
EBI	– External bus interface	**S/B**	– Stand-by
ECSM	– Error correction status module	**SIU**	– System integration unit
eDMA2	– Enhanced direct memory access	**SPE2**	– Signal processing engine 2
eMIOS	– Enhanced modular I/O system	**SRAM**	– General-purpose static RAM
eQADC	– Enhanced queued A/D converter module	**VLE**	– Variable length instruction encoding

Figure 2. Block Diagram

3 Pin Assignments

The figures in this section show the primary pin function. For the full signal properties and muxing table, see Appendix A, Signal Properties and Muxing.

3.1 324-ball TEPBGA Pin Assignments

Figure 3 shows the 324-ball TEPBGA pin assignments. The same information is shown in Figure 4 through Figure 5.

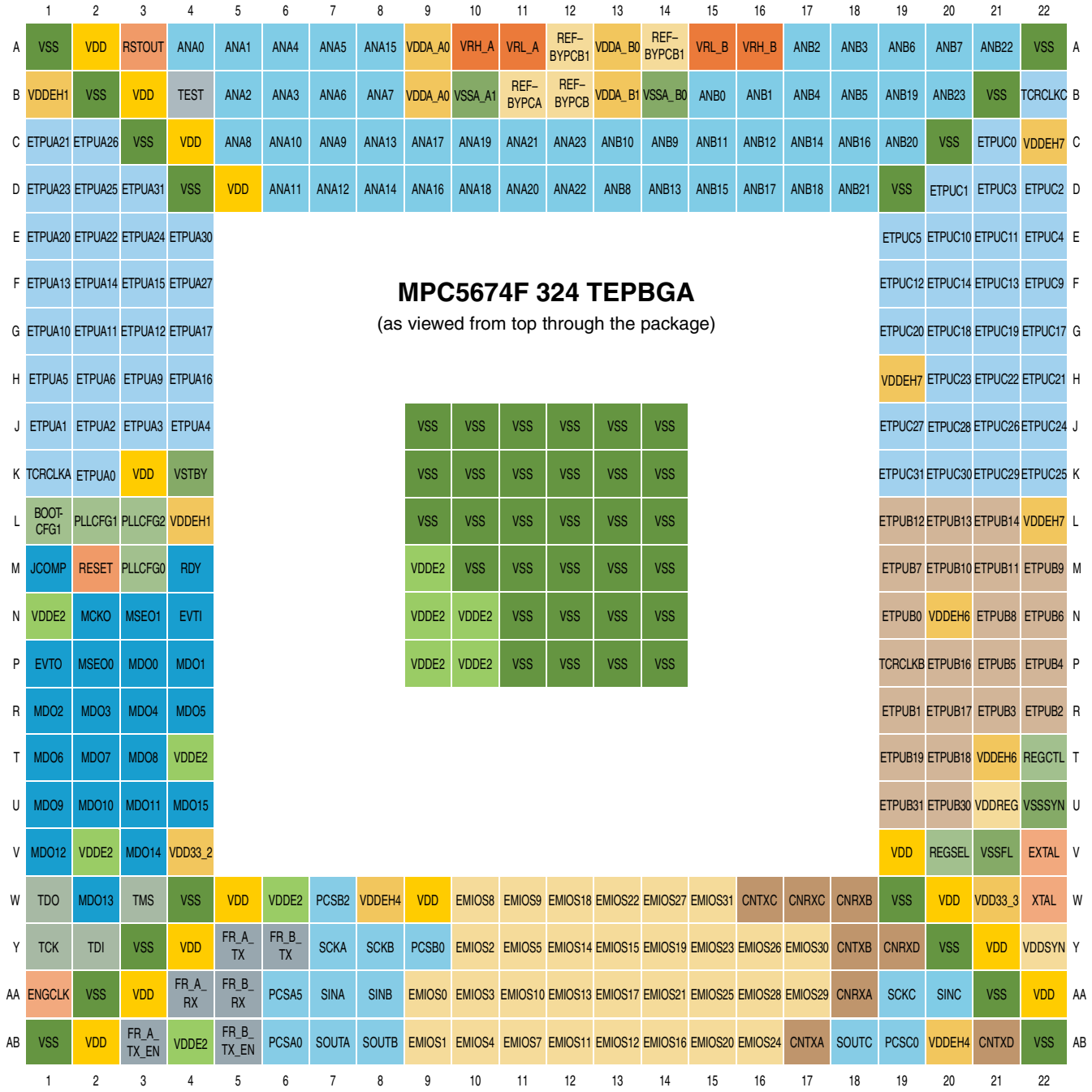


Figure 3. MPC5674F 324-ball TEPBGA (full diagram)

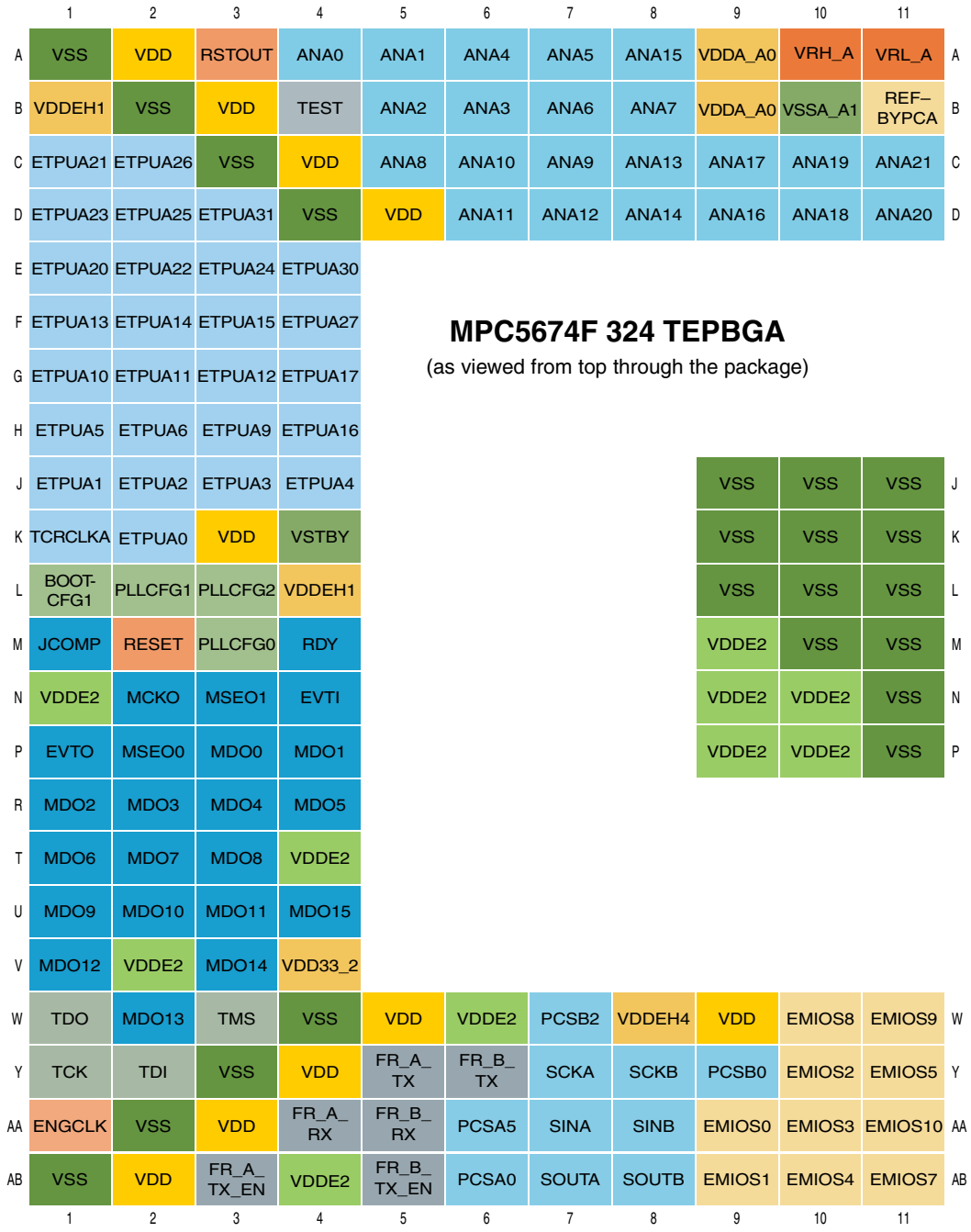


Figure 4. MPC5674F 324-ball TEPBGA (1 of 2)

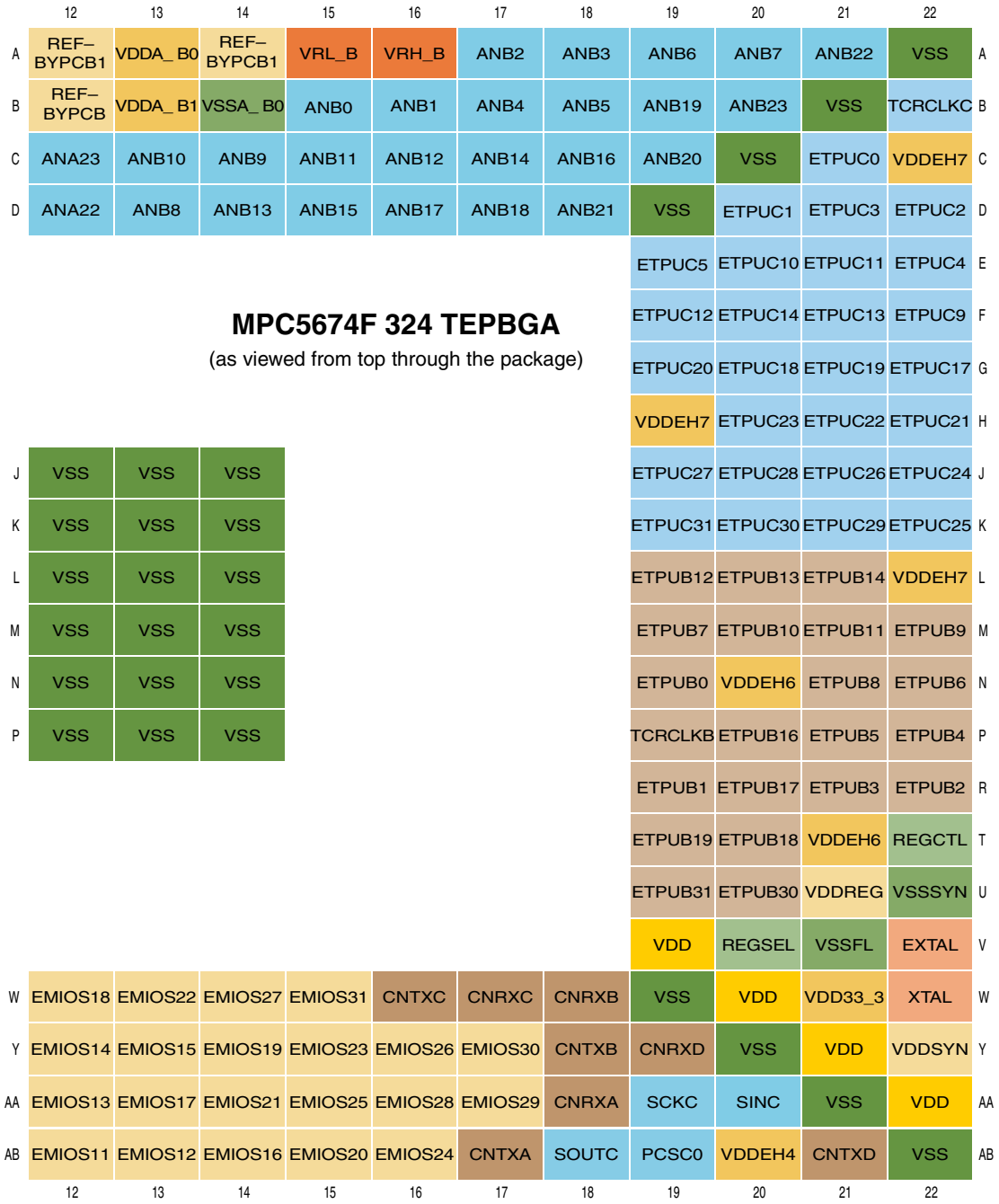


Figure 5. MPC5674F 324-ball TEPBGA (2 of 2)

3.2 416-ball TEPBGA Pin Assignments

Figure 6 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 7 through Figure 10.

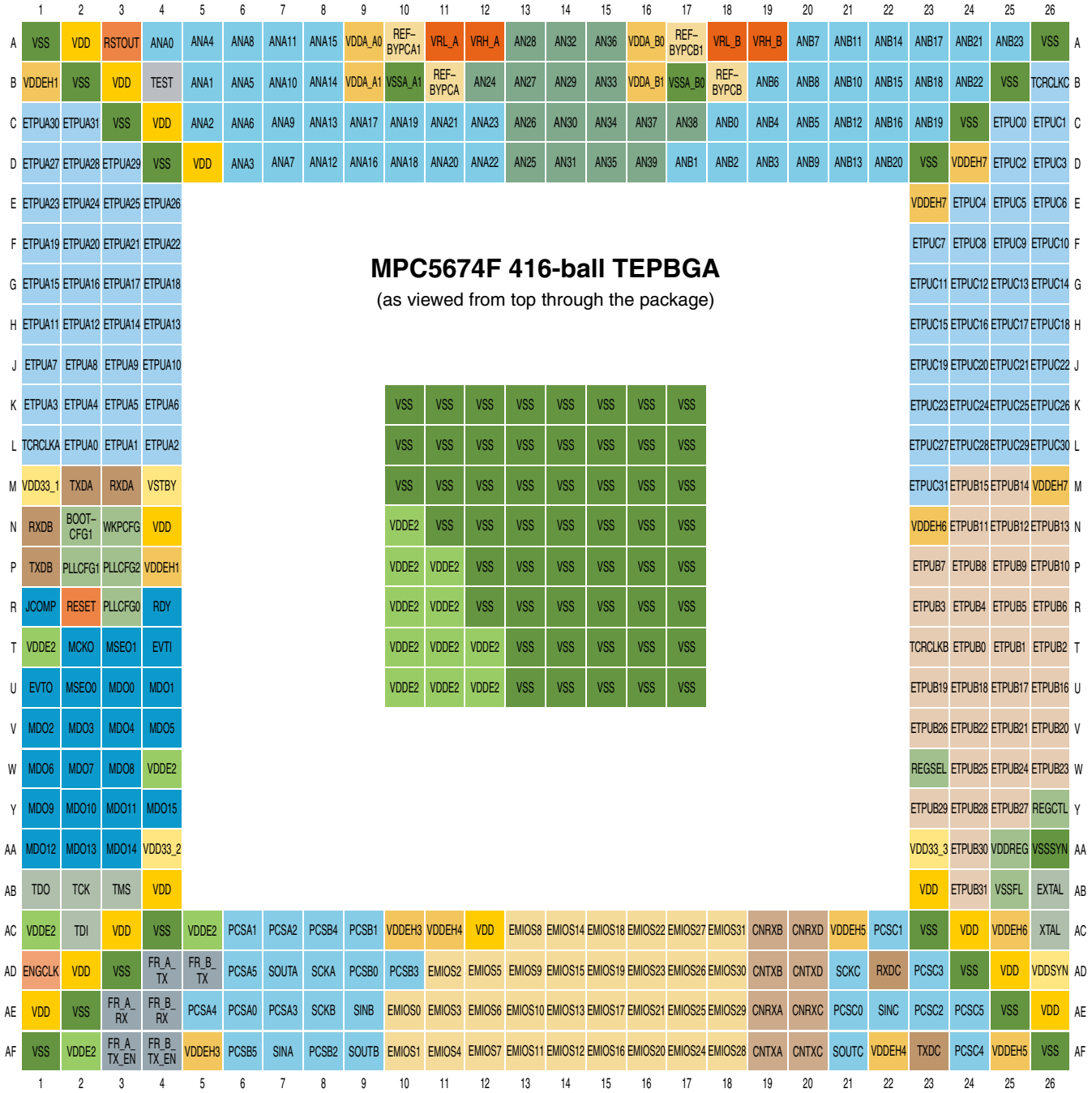


Figure 6. MPC5674F 416-ball TEPBGA (full diagram)

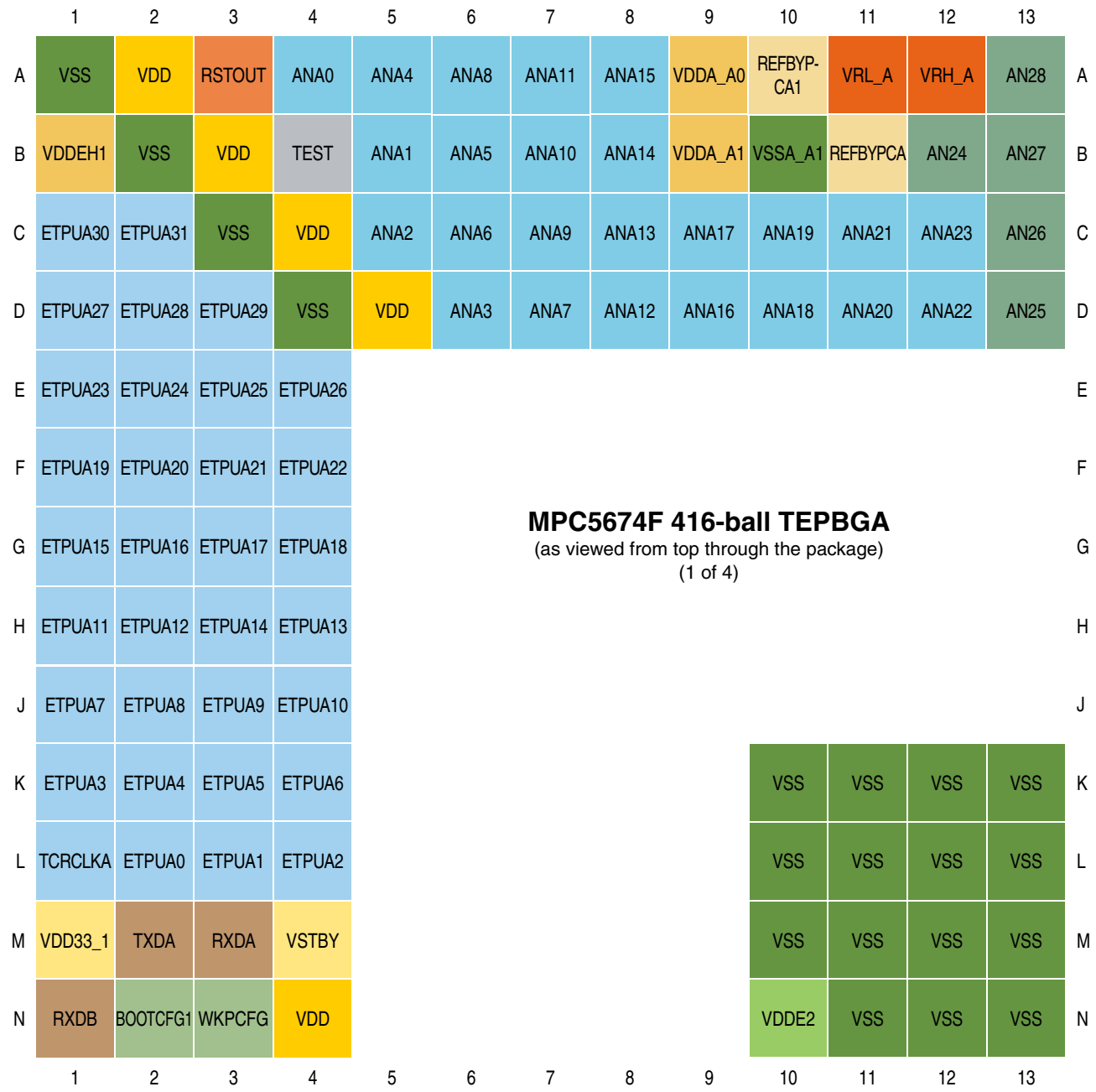
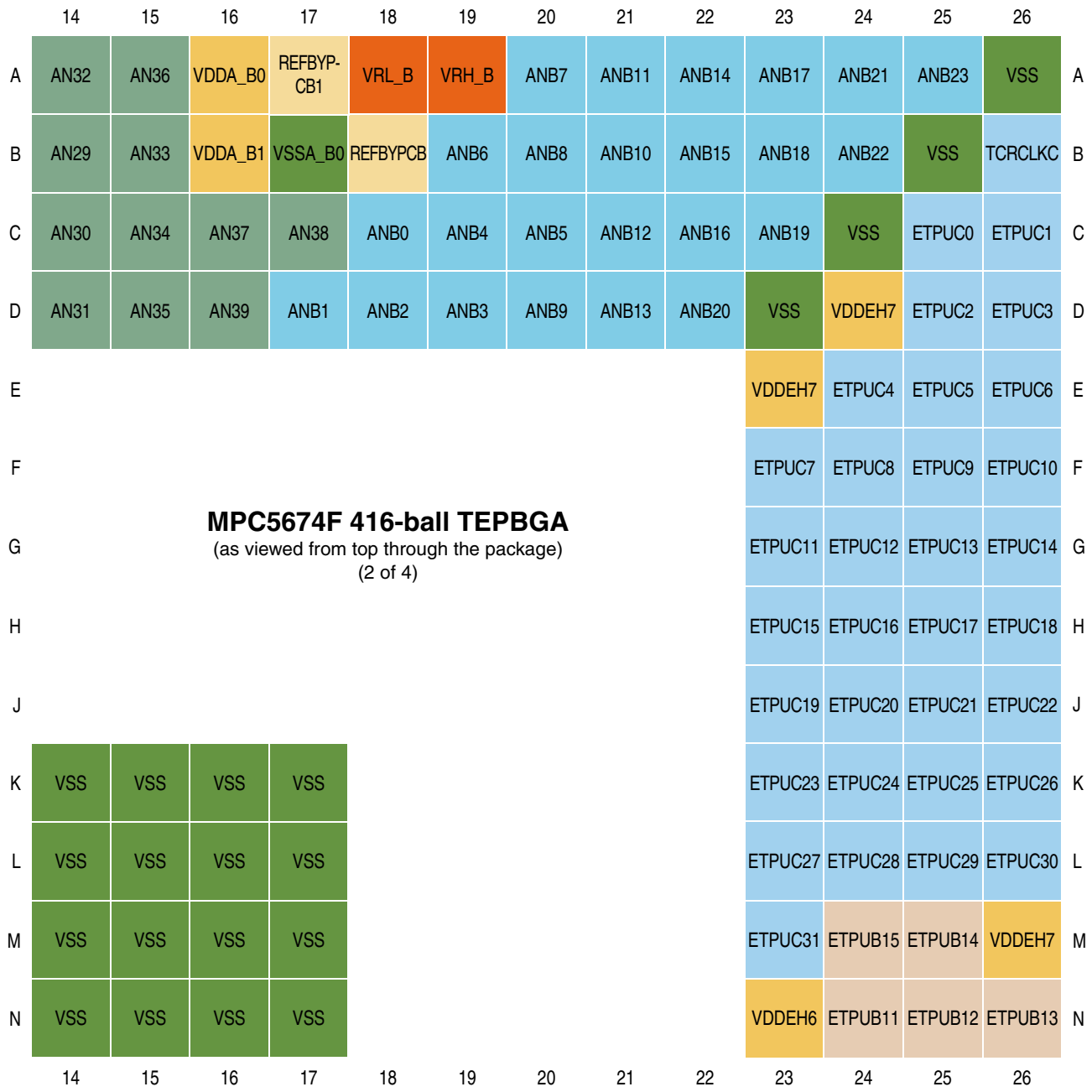
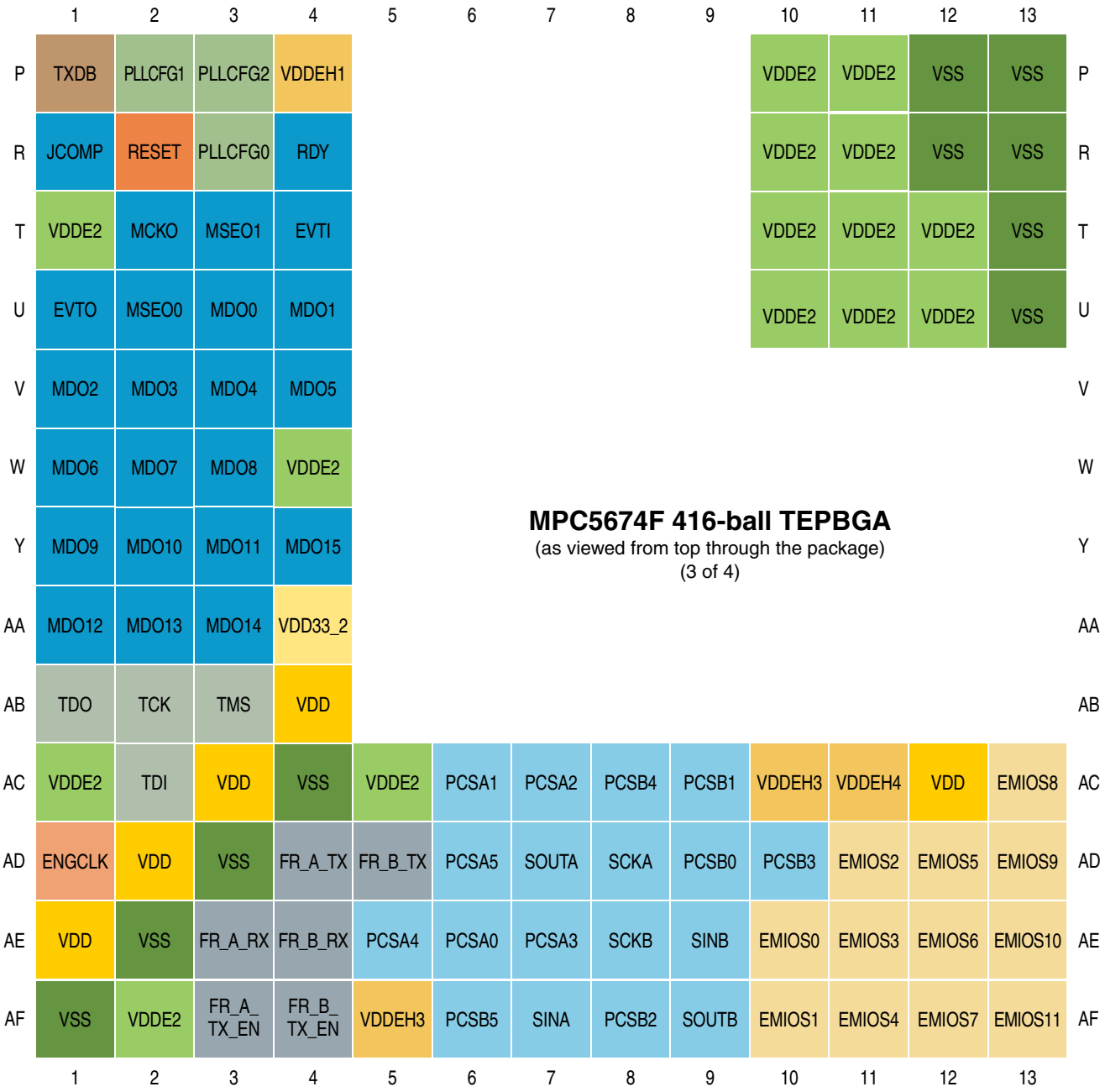


Figure 7. MPC5674F 416-ball TEPBGA (1 of 4)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN32	AN36	VDDA_B0	REFBYP-CB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	AN29	AN33	VDDA_B1	VSSA_B0	REFBYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E										VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F										ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G										ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H										ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J										ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 8. MPC5674F 416-ball TEPBGA (2 of 4)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	U
V	MDO2	MDO3	MDO4	MDO5										V
W	MDO6	MDO7	MDO8	VDDE2										W
Y	MDO9	MDO10	MDO11	MDO15										Y
AA	MDO12	MDO13	MDO14	VDD33_2										AA
AB	TDO	TCK	TMS	VDD										AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 9. MPC5674F 416-ball TEPBGA (3 of 4)

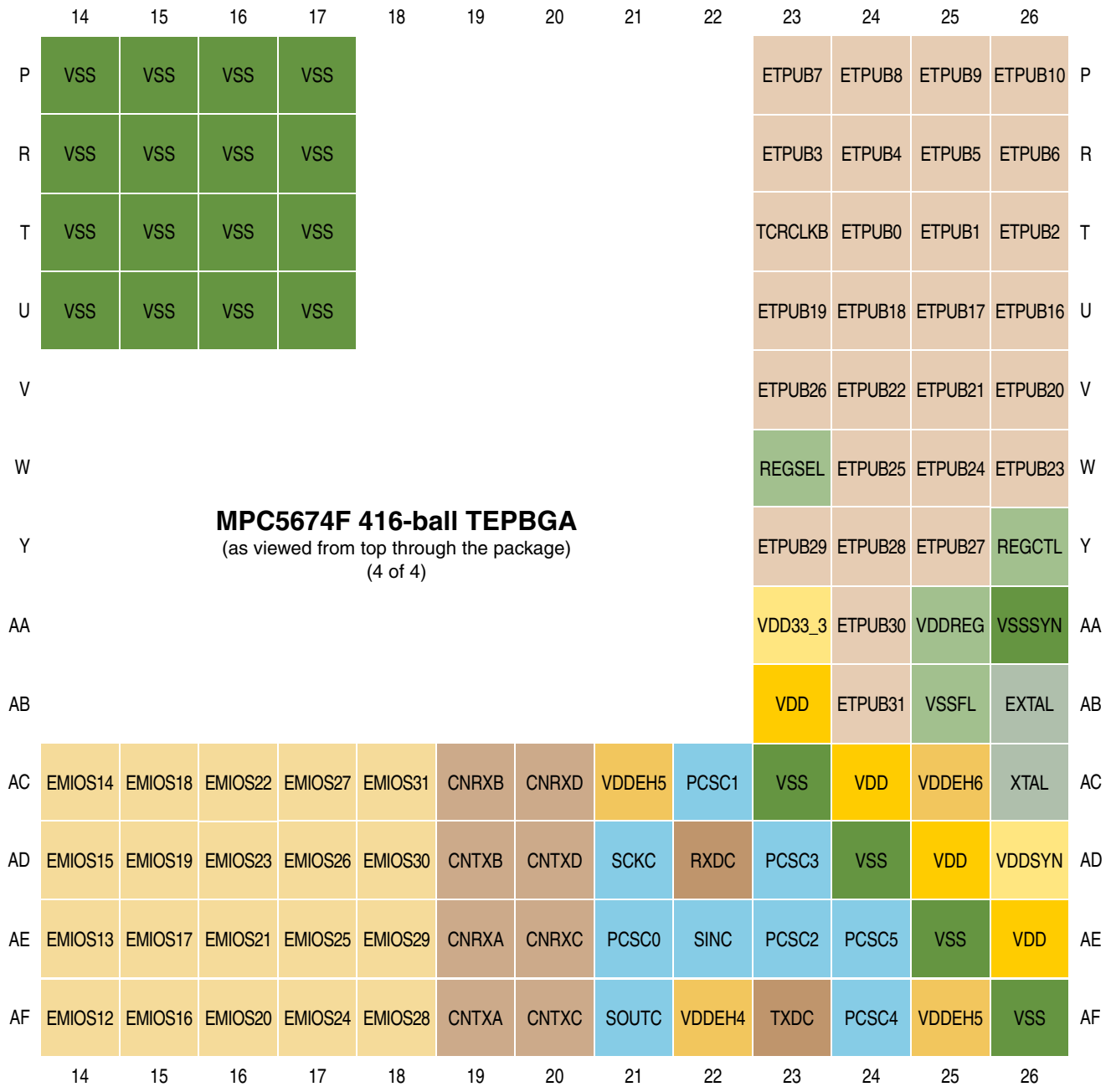


Figure 10. MPC5674F 416-ball TEPBGA (4 of 4)

3.3 516-ball TEPBGA Pin Assignments

Figure 11 shows the 516-ball TEPBGA pin assignments in one figure. The same information is shown split into four quadrants in Figure 12 through Figure 15.

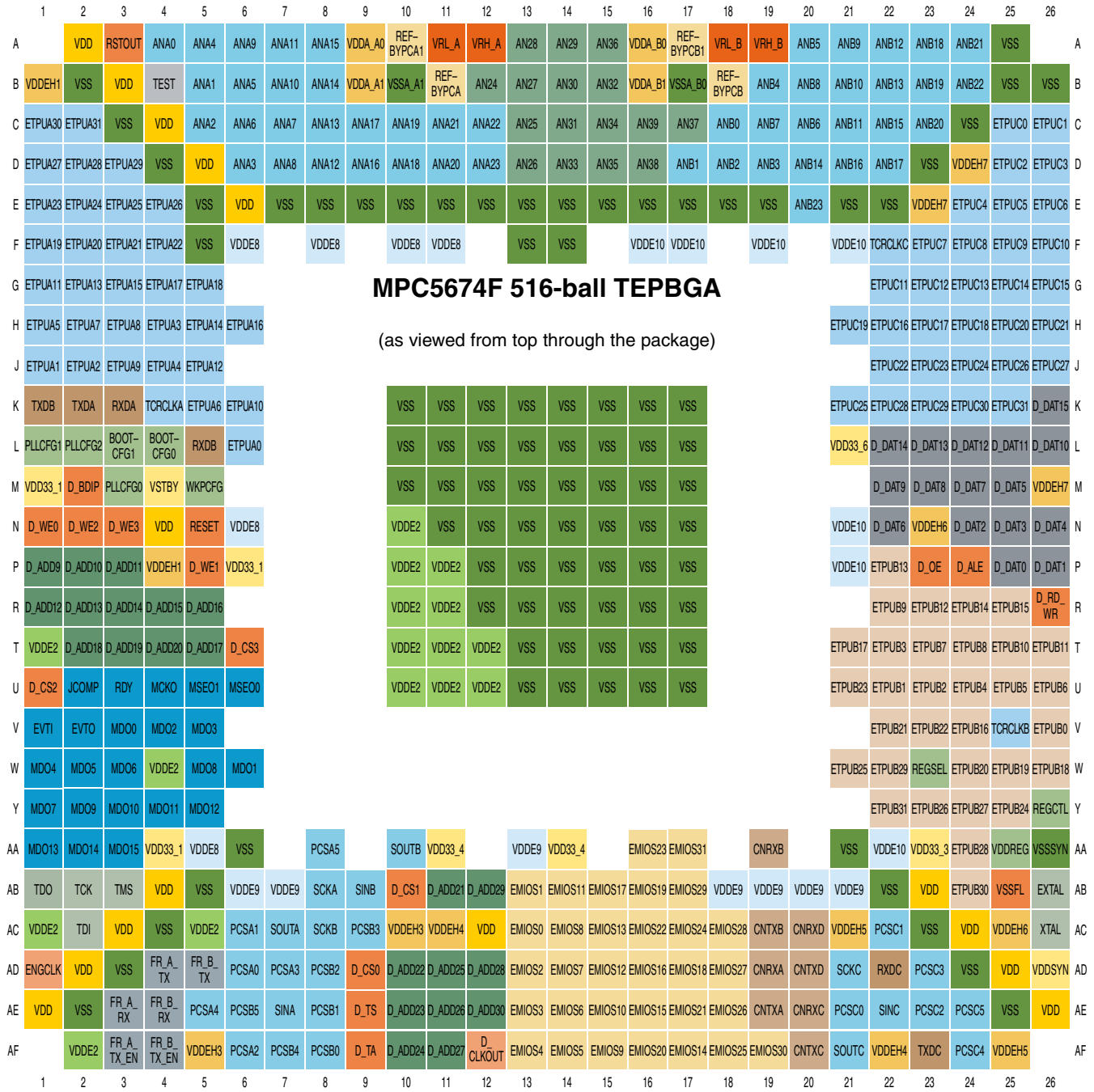
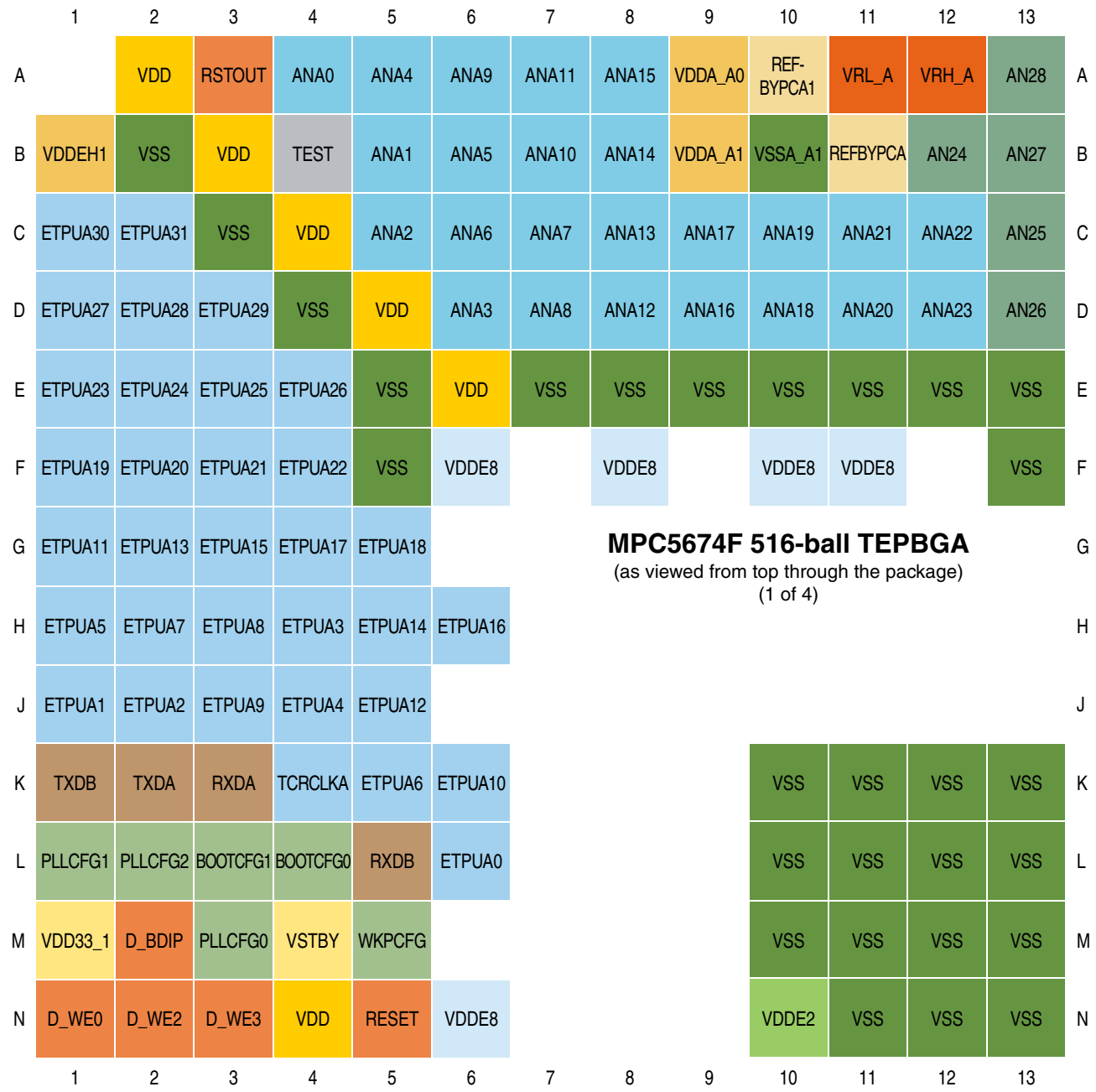
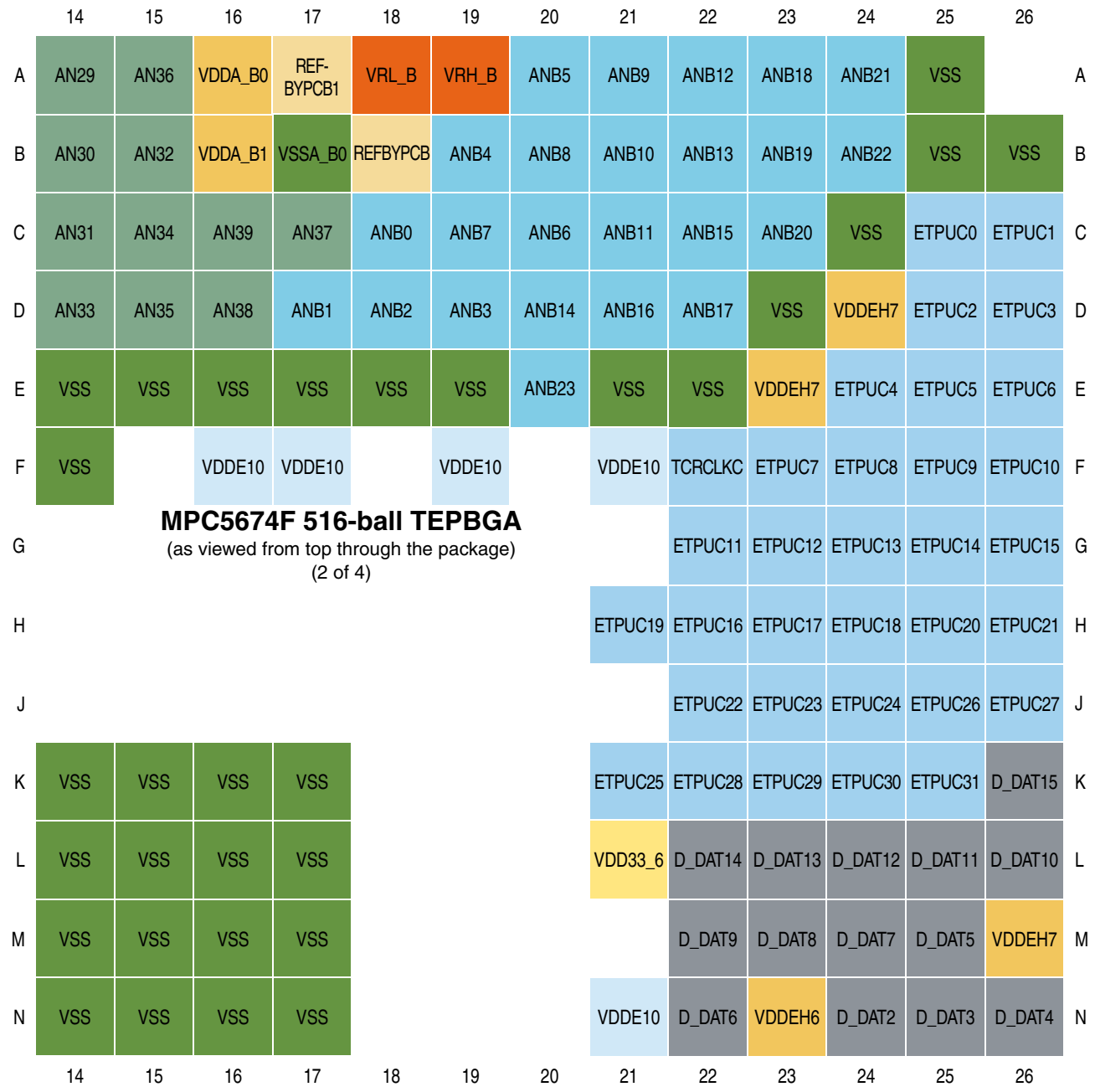


Figure 11. MPC5674F 516-ball TEPBGA (full diagram)



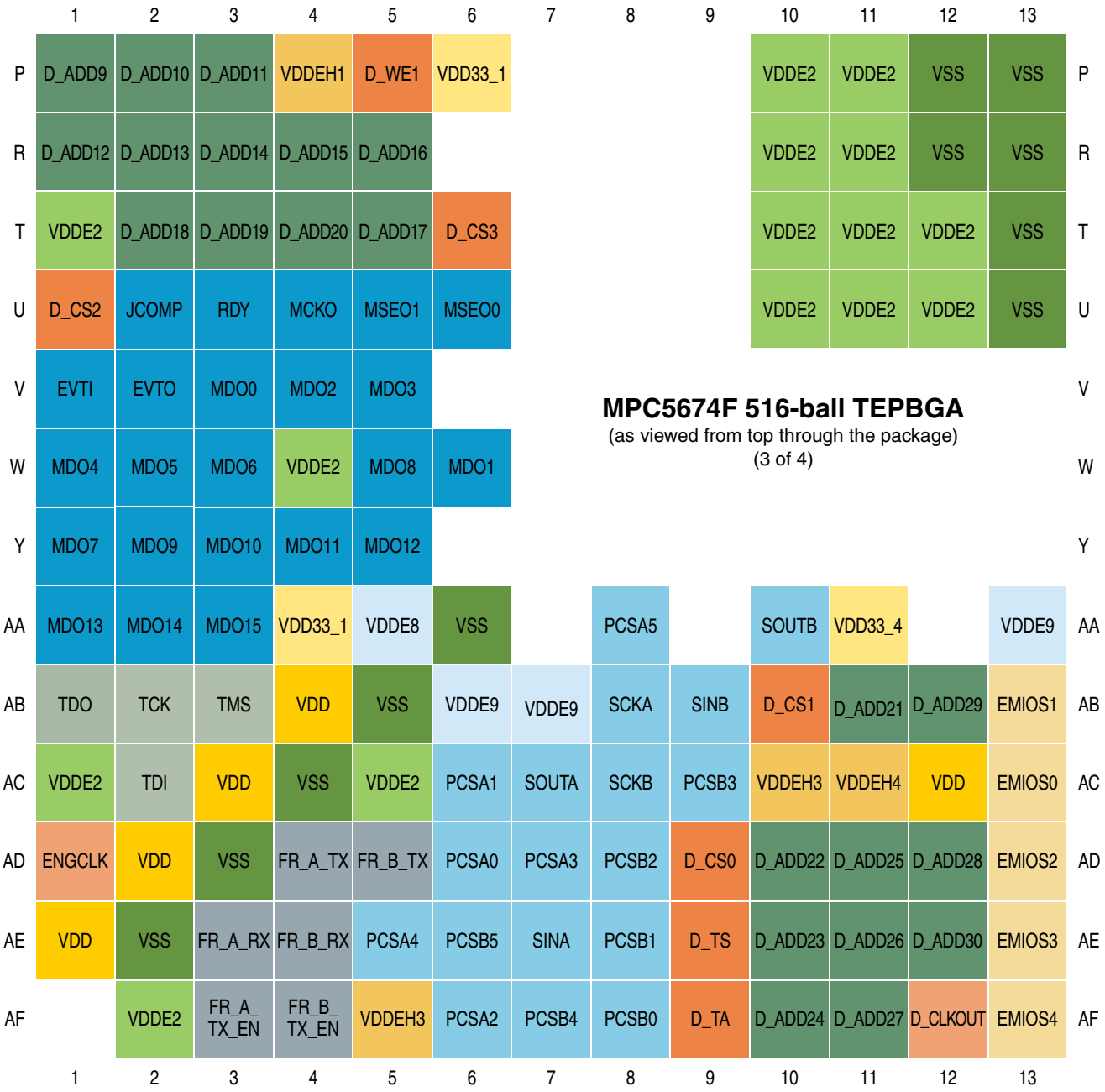
	1	2	3	4	5	6	7	8	9	10	11	12	13	
A		VDD	RSTOUT	ANA0	ANA4	ANA9	ANA11	ANA15	VDDA_A0	REF-BYPCA1	VRL_A	VRH_A	AN28	A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REFBYPCA	AN24	AN27	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA7	ANA13	ANA17	ANA19	ANA21	ANA22	AN25	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA8	ANA12	ANA16	ANA18	ANA20	ANA23	AN26	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18									G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16								H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12									J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	K
L	PLLCFG1	PLLCFG2	BOOTCFG1	BOOTCFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	L
M	VDD33_1	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 12. MPC5674F 516-ball TEPBGA (1 of 4)



	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	AN29	AN36	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	AN30	AN32	VDDA_B1	VSSA_B0	REFBYPCB	ANB4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	AN31	AN34	AN39	AN37	ANB0	ANB7	ANB6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	AN33	AN35	AN38	ANB1	ANB2	ANB3	ANB14	ANB16	ANB17	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G									ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H								ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J									ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	VSS	VSS	VSS	VSS				VDD33_6	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 13. MPC5674F 516-ball TEPBGA (2 of 4)



	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	VDD33_1				VDDE2	VDDE2	VSS	VSS	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	U
V	EVTI	EVTO	MDO0	MDO2	MDO3									V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1								W
Y	MDO7	MDO9	MDO10	MDO11	MDO12									Y
AA	MDO13	MDO14	MDO15	VDD33_1	VDDE8	VSS		PCSA5		SOUTB	VDD33_4		VDDE9	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	AE
AF		VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 14. MPC5674F 516-ball TEPBGA (3 of 4)

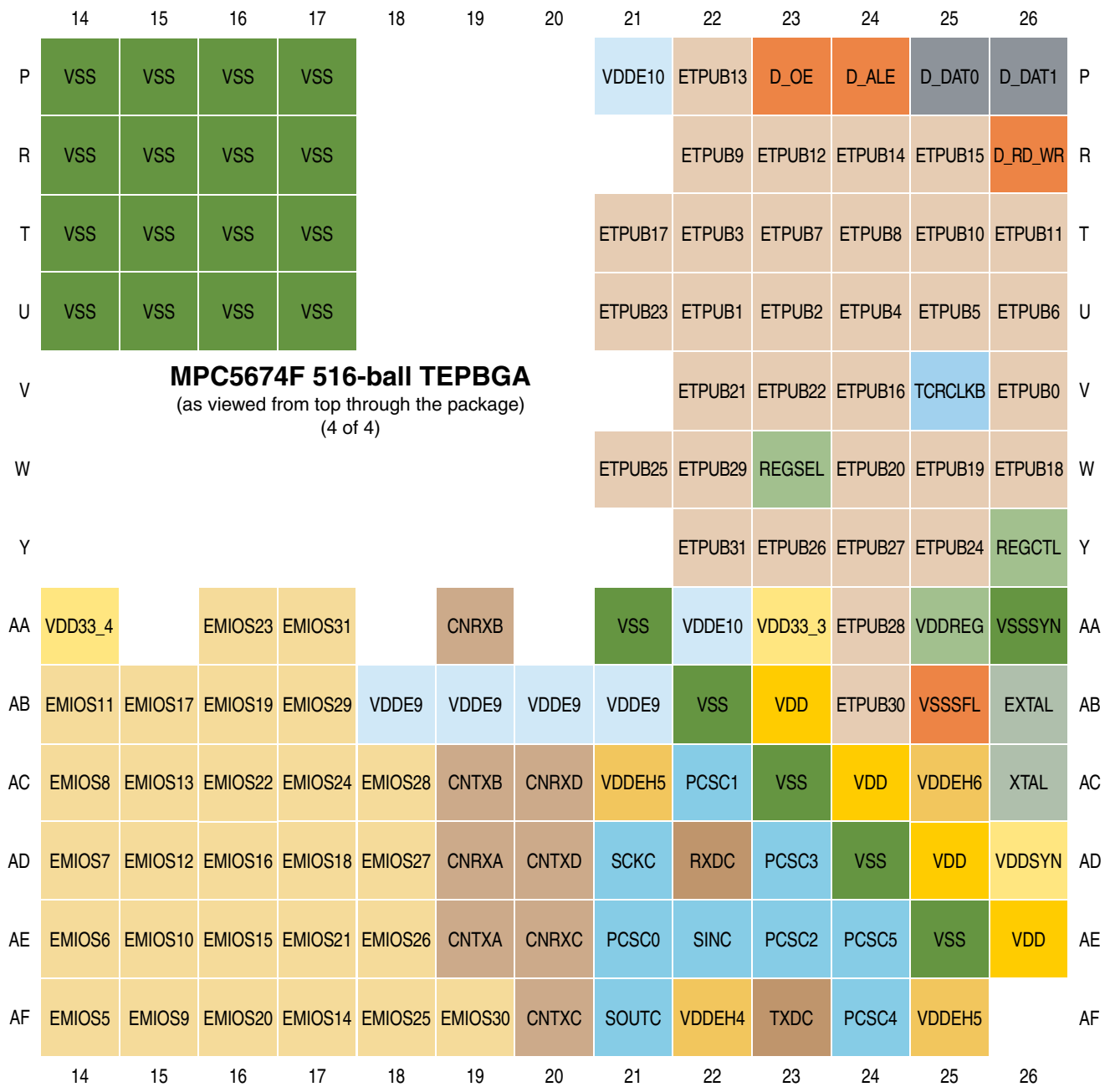


Figure 15. MPC5674F 516-ball TEPBGA (4 of 4)

3.4 Signal Properties and Muxing

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5674F.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	–0.3	2.0 [2]	V
2	SRAM Standby Voltage	V_{STBY}	–0.3	6.4 [3,4]	V
3	Clock Synthesizer Voltage	V_{DDSYN}	–0.3	5.3 [4,5]	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	–0.3	5.3 [4,5]	V
5	Analog Supply Voltage (reference to V_{SSA}[6])	V_{DDA}[7]	–0.3	6.4 [3,4]	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	–0.3	5.3 [4,5]	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	–0.3	6.4 [3,4]	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	–0.3	6.4 [3,4]	V
9	Analog Reference High Voltage (reference to V_{RL}[8])	V_{RH}[9]	–0.3	6.4 [3,4]	V
10	V_{SS} to V_{SSA}[8] Differential Voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	–0.3	6.4 [3,4]	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} – V_{DDSYN}$	–0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
15	Maximum Digital Input Current [10] (per pin, applies to all digital pins)	I_{MAXD}	–3 [11]	3 [11]	mA
16	Maximum Analog Input Current [12] (per pin, applies to all analog pins)	I_{MAXA}	– 3 [7]	3 [7,11]	mA
17	Maximum Operating Temperature Range [13] – Die Junction Temperature	T_J	–40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	–55.0	150.0	°C
19	Maximum Solder Temperature [14] Pb-free package SnPb package	T_{sdr}	 — —	 260.0 245.0	°C
20	Moisture Sensitivity Level [15]	MSL	—	3	—

[1] Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

[2] 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

[3] 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

[4] Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

[5] 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

[6] MPC5674F has two analog power supply pins on the pinout: VDDA_A and VDDA_B.

[7] MPC5674F has two analog ground supply pins on the pinout: VSSA_A and VSSA_B.

[8] MPC5674F has two analog low reference voltage pins on the pinout: VRL_A and VRL_B.

[9] MPC5674F has two analog high reference voltage pins on the pinout: VRH_A and VRH_B.

[10] Total injection current for all pins must not exceed 25 mA at maximum operating voltage.

[11] Injection current of ±5 mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or V_{DDEH} supply when under this stress condition.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Lifetime operation at these specification limits is not guaranteed.

[14] Solder profile per CDF-AEC-Q100.

[15] Moisture sensitivity per JEDEC test method A112.

4.2 Thermal Characteristics

Table 4. Thermal Characteristics, 416-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	19	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	14	°C/W
Junction to Board [5]	$R_{\theta JB}$	9	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

[2] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[3] Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

[4] Per JEDEC JESD51-6 with the board horizontal.

[5] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[6] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 5. Thermal Characteristics, 516-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	25	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	20	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	15	°C/W
Junction to Board [5]	$R_{\theta JB}$	10	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 6. Thermal Characteristics, 324-pin Package[1]

MPC5674F Thermal Characteristic	Symbol	Value	Unit
Junction to ambient [2, 3], natural convection (one-layer board)	$R_{\theta JA}$	29	°C/W
Junction to ambient [1, 4], natural convection (four-layer board 2s2p)	$R_{\theta JA}$	19	°C/W
Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	23	°C/W
Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	16	°C/W
Junction to board [5] (four-layer board 2s2p)	$R_{\theta JB}$	10	°C/W
Junction to case [6]	$R_{\theta JC}$	7	°C/W
Junction to package top [7], natural convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.nxp.com and perform a keyword search for "radiated emissions." The following tables list the values of the device's radiated emissions operating behaviors.

Table 7. EMC Radiated Emissions Operating Behaviors: 416 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	26	dBµV	1
				50–150	30		
				150–500	34		
				500–1000	30		
				IEC and SAE level	I^2	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	24	dBµV	1
				50–150	25		
				150–500	25		
				500–1000	21		
				IEC and SAE level	K[5]	—	1,3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 I = 36 dBµV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 "FM on" = FM depth of ±2%

5 K = 30 dBμV

Table 8. EMC Radiated Emissions Operating Behaviors: 516 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBμV	1
				50–150	48		
				150–500	48		
				500–1000	47		
				IEC and SAE level	G[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 516 BGA EBI on CLK on FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	40	dBμV	1
				50–150	44		
				150–500	41		
				500–1000	36		
				IEC and SAE level	G[2]	—	1, 3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 G = 48 dBμV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 "FM on" = FM depth of ±2%

4.4 ESD Characteristics

Table 9. ESD Ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Note: For ADC internal resource measurements, see Table 21 in Section 4.9.1, "ADC Internal Resource Measurements."

Table 10. PMC Operating conditions

Name	Parameter	Condition	Min	Typ	Max	Unit	Note
V_{DDREG}	Supply voltage VDDREG 5V nominal	LDO5V / SMPS5V mode	4.5	5	5.5	V	1
V_{DDREG}	Supply voltage VDDREG 3V nominal	LDO3V mode	3.0	3.3	3.6	V	1
V_{DD33}	Supply voltage VDDSYN / V_{DD33} 3.3V nominal	LDO3V mode	3.0	3.3	3.6	V	2
V_{DD}	Core supply voltage	—	1.14	1.2	1.32	V	3

1 Voltage should be higher than maximum V_{LVDREG} to avoid LVD event

2 Applies to both V_{DD33} (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V_{LVD33} to avoid LVD event

3 Voltage should be higher than maximum V_{LVD12} to avoid LVD event

NOTE

In the following table, "untrimmed" means "at reset" and "trimmed" means "after reset".

Table 11. PMC Electrical Specifications

ID	Name	Parameter	Min	Typ	Max	Unit
1	V_{BG}	Nominal bandgap reference voltage	0.608	0.620	0.632	V
1a	—	Untrimmed bandgap reference voltage	V_{BG} – 5%	V_{BG}	V_{BG} + 5%	V
2	$V_{DD12OUT}$	Nominal VRC regulated 1.2V output VDD	—	1.27	—	V
2a	—	Untrimmed VRC 1.2V output variation before band gap trim (unloaded) **Note:** Voltage should be higher than maximum V_{LVD12} to avoid LVD event	$V_{DD12OUT}$ – 14%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 10%	V
2b	—	Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max. 1A)[1]	$V_{DD12OUT}$ – 10%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 5%	V
2c	$V_{STEPV12}$	Trimming step $V_{DD12OUT}$	—	10	—	mV
3	V_{PORC}	POR rising VDD 1.2V	—	0.7	—	V
3a	—	POR VDD 1.2V variation	V_{PORC} – 30%	V_{PORC}	V_{PORC} + 30%	
3b	—	POR 1.2V hysteresis	—	75	—	mV
4	V_{LVD12}	Nominal rising LVD 1.2V **Note:** ~$V_{DD12OUT}$ × 0.87	—	1.100	—	V
4a	—	Untrimmed LVD 1.2V variation before band gap trim **Note:** Rising VDD	V_{LVD12} – 6%	V_{LVD12}	V_{LVD12} + 6%	V
4b	—	Trimmed LVD 1.2V variation after band gap trim Rising VDD	V_{LVD12} – 3%	V_{LVD12}	V_{LVD12} + 3%	V

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
4c	—	LVD 1.2V Hysteresis	15	20	25	mV
4d	$V_{LVDSTEP12}$	Trimming step LVD 1.2V	—	10	—	mV
5	I_{REGCTL}	VRC DC current output on REGCTL	—	—	20	mA
6	—	Voltage regulator 1.2V current consumption VDDREG	—	3	—	mA
7	$V_{DD33OUT}$	Nominal V_{REG} 3.3V output	—	3.3	—	V
7a	—	Untrimmed V_{REG} 3.3V output variation before band gap trim (unloaded) **Note:** Rising VDDSYN	$V_{DD33OUT}$ – 6%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	V
7b	—	Trimmed V_{REG} 3.3V output variation after band gap trim (max. load 80mA)	$V_{DD33OUT}$ – 5%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	V
7c	$V_{STEPV33}$	Trimming step VDDSYN	—	30	—	mV
8	V_{LVD33}	Nominal rising LVD 3.3V **Note:** ~$V_{DD33OUT}$ × 0.872	—	2.950	—	V
8a	—	Untrimmed LVD 3.3V variation before band gap trim **Note:** Rising VDDSYN	V_{LVD33} – 5%	V_{LVD33}	V_{LVD33} + 5%	V
8b	—	Trimmed LVD 3.3V variation after bad gap trim **Note:** Rising VDDSYN	V_{LVD33} – 3%	V_{LVD33}	V_{LVD33} + 3%	V
8c	—	LVD 3.3V Hysteresis	—	30	—	mV
8d	$V_{LVDSTEP33}$	Trimming step LVD 3.3V	—	30	—	mV
9	I_{DD33}	V_{REG} = 4.5 V, max DC output current V_{REG} = 4.25 V, max DC output current, crank condition **Note:** Max current supplied by VDDSYN that does not cause it to drop below V_{LVD33}	— —	— —	80 40	mA mA
10	—	Voltage regulator 3.3V current consumption VDDREG **Note:** Except I_{DD33}	—	2	—	mA
11	V_{PORREG}	POR rising on VDDREG	—	2.00	—	V
11a	—	POR VDDREG variation	V_{PORREG} – 30%	V_{PORREG}	V_{PORREG} + 30%	V
11b	—	POR VDDREG hysteresis	—	250	—	mV
12	V_{LVDREG}	Nominal rising LVD VDDREG (LDO3V / LDO5V mode)	—	2.950	—	V
12a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
12b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V

Table 11. PMC Electrical Specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
12c	—	LVD VDDREG Hysteresis (LDO3V / LDO5V mode)	—	30	—	mV
12d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (LDO3V / LDO5V mode)	—	30	—	mV
13	V_{LVDREG}	Nominal rising LVD VDDREG (SMPS5V mode)	—	4.360	—	V
13a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
13b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
13c	—	LVD VDDREG Hysteresis (SMPS5V mode)	—	50	—	mV
13d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (SMPS5V mode)	—	50	—	mV
14	V_{LVDA}	Nominal rising LVD VDDA	—	4.60	—	V
14a	—	Untrimmed LVD VDDA variation before band gap trim	V_{LVDA} – 5%	V_{LVDA}	V_{LVDA} + 5%	V
14b	—	Trimmed LVD VDDA variation after band gap trim	V_{LVDA} – 3%	V_{LVDA}	V_{LVDA} + 3%	V
14c	—	LVD VDDA Hysteresis	—	150	—	mV
14d	$V_{LVDASTEP}$	Trimming step LVD VDDA	—	20	—	mV
15	—	SMPS regulator output resistance **Note:** Pulup to VDDREG when high, pulldown to VSSREG when low.	—	15	25	Ohm
16	—	SMPS regulator clock frequency (after reset)	1.0	1.5	2.4	MHz
17	—	SMPS regulator overshoot at start-up[2]	—	1.32	1.4	V
18	—	SMPS maximum output current	—	1.0	—	A
19	—	Voltage variation on current step[2] (20% to 80% of maximum current with 4 usec constant time)	—	—	0.1	V

1 VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 uA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

2 Parameter cannot be tested; this value is based on simulation and characterization.

4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 12 and Table 13.

Table 12. Power Sequence Pin States for MH and AE pads

VDD	VDD33	VDDE	MH Pad	MH+LVDS Pads[1]	AE/up-down Pads
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled

1 MH+LVDS pads are output-only.

Table 13. Power Sequence Pin States for F and FS pads

VDD	VDD33	VDDE	F and FS pads
low	low	high	Outputs Disabled
low	high	—	Outputs Disabled
high	low	low	Outputs Disabled
high	low	high	Outputs Disabled
high	high	low	Normal operation - except no drive current and input buffer output is unknown.[1]
high	high	high	Normal Operation

1 The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

4.6.1 Power-Up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tristates all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DD} powers up before V_{DDE}/V_{DDEH} must power up.

The rise times on the power supplies are to be no faster than 25 V/millisecond.

4.6.2 Power-Down

If V_{DD} is powered down first, then all drivers are tristated. There is no limit to how long after V_{DD} powers down before V_{DDE}/V_{DDEH} must power down.

If V_{DDE}/V_{DDEH} is powered down first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DDE}/V_{DDEH} powers down before V_{DD} must power down.

There are no limits on the fall times for the power supplies.

4.6.3 Power Sequencing and POR Dependent on V_{DDA}

During power up or down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggers POR (ADC monitors on V_{DDEH1} segment which powers the RESET pin) if the leakage current path created, when V_{DDA} is sufficiently low, causes sufficient voltage drop on V_{DDEH1} node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially V_{DDEH1}) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of (($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KOhms) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V).
- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since $V_{DD} = 1.32$ V max.

4.7 DC Electrical Specifications

Table 14. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage (External Regulation)	V_{DD}	1.14	1.32[1,2]	V
1a	Core Supply Voltage (Internal Regulation)[3]	V_{DD}	1.08	1.32	V
2	I/O Supply Voltage (fast I/O pads)	V_{DDE}	3.0	3.6[1,4]	V
3	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	3.0	5.25[1,5]	V
4	3.3 V I/O Buffer Voltage	V_{DD33}	3.0	3.6[1,4]	V
5	Analog Supply Voltage	V_{DDA}	4.75	5.25[1,5]	V
6a	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_LOW}	0.95[6]	1.2	V
6b	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_HIGH}	2	6	V
7	Voltage Regulator Control Input Voltage[7]	V_{DDREG}	2.7[8]	5.5[1,5]	V

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Clock Synthesizer Operating Voltage[9]	V_{DDSYN}	3.0	3.6[1,4]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 0.65 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE}	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 0.65 × V_{DDEH} 0.55 × V_{DDEH}	V_{DDEH} + 0.3	V
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	V_{SS} – 0.3	 0.35 × V_{DDEH} 0.40 × V_{DDEH}	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 × V_{DDE}	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	0.1 × V_{DDEH}	—	V
15	Analog Input Voltage	V_{INDC}	V_{SSA} – 0.1	V_{DDA} + 0.1	V
16	Fast I/O Output High Voltage[10]	V_{OH_F}	0.8 × V_{DDE}	—	V
17	Medium I/O Output High Voltage[11]	V_{OH_S}	0.8 × V_{DDEH}	—	V
18	Fast I/O Output Low Voltage[10]	V_{OL_F}	—	0.2 × V_{DDE}	V
19	Medium I/O Output Low Voltage[11]	V_{OL_S}	—	0.2 × V_{DDEH}	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 264 MHz V_{DD} @1.32 V V_{STBY}[13] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$	 — — —	 850 0.10 0.15	 mA mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 264 MHz V_{DD33}[14] V_{DDSYN}	 I_{DD33} I_{DDSYN}	 — —	 note[14] 7[15]	 mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[16] 1.0 22	 mA mA mA

Table 14. DC Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
27	Operating Current V_{DDE}/V_{DDEH}[17] Supplies V_{DDE2} V_{DDEH1} V_{DDEH3} V_{DDEH4} V_{DDEH5} V_{DDEH6} V_{DDEH7}	 I_{DD2} I_{DD1} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7}	 — — — — — — —	 note[17]	 mA mA mA mA mA mA mA
28	Fast I/O Weak Pull Up/Down Current[18] 3.0 V–3.6 V	 I_{ACT_F}	 42	 158	 µA
29	Medium I/O Weak Pull Up/Down Current[19] 3.0 V–3.6 V 4.5 V–5.5 V	I_{ACT_S}	 15 35	 95 200	 µA µA
30	I/O Input Leakage Current[20]	I_{INACT_D}	–2.5	2.5	µA
31	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
32	Analog Input Current, Channel Off[21], AN[0:7], AN38, AN39 Analog Input Current, Channel Off, all other analog inputs AN[x]	I_{INACT_A}	–250 –150	250 150	nA nA
33	V_{SS} Differential Voltage	$V_{SS} - V_{SSA}$	–100	100	mV
34	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 100	mV
35	V_{RL} Differential Voltage	$V_{RL} - V_{SSA}$	–100	100	mV
36	Analog Reference High Voltage	V_{RH}	V_{DDA} – 100	V_{DDA}	mV
37	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	4.75	5.25	V
38	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} - V_{SS}$	–100	100	mV
39	Operating Temperature Range—Ambient (Packaged)	T_A (T_L to T_H)	–40.0	125.0	°C
40	Slew rate on power supply pins	—	—	25	V/ms
41	Weak Pull-Up/Down Resistance[22], 200 K Option	$R_{PUPD200K}$	130	280	kΩ
42	Weak Pull-Up/Down Resistance[22], 100 K Option	$R_{PUPD100K}$	65	140	kΩ
43	Weak Pull-Up/Down Resistance[22], 5 K Option	R_{PUPD5K}	1.4	7.5	kΩ
44	Pull-Up/Down Resistance Matching Ratios[23] (100K/200K)	$R_{PUPDMTCH}$	–2.5	+2.5	%

1 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

2 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

3 Assumed with DC load.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 V_{STBY} below 0.95 V the RAM will not retain states, but will be operational. V_{STBY} can be 0 V when bypass standby mode.

7 Regulator is functional with derated performance, with supply voltage down to 4.0 V for system with V_{DDREG} = 4.5 V (min).

8 2.7 V minimum operating voltage allowed during vehicle crank for system with V_{DDREG} = 3.0 V (min). Normal operating voltage should be either V_{DDREG} = 3.0 V (min) or 4.5 V (min) depending on the user regulation voltage system selected.

9 Required to be supplied when 3.3 V regulator is disabled. See Section 4.5, “PMC/POR/LVI Electrical Specifications.”

[10] I_{OH_F} = {16,32,47,77} mA and I_{OL_F} = {24,48,71,115} mA for {00,01,10,11} drive mode with V_{DDE} = 3.0 V. This spec is for characterization only.

[11] I_{OH_S} = {11.6} mA and IOL_S = {17.7} mA for {medium} I/O with V_{DDE} = 4.5 V;
I_{OH_S} = {5.4} mA and IOL_S = {8.1} mA for {medium} I/O with V_{DDE} = 3.0 V. These specs are for characterization only.

[12] Applies to D_CLKOUT, external bus pins, and Nexus pins.

[13] V_{STBY} current specified at 1.0 V at a junction temperature of 85 °C. V_{STBY} current is 700 µA maximum at a junction temperature of 150 °C.

[14] Power requirements for the V_{DD33} supply depend on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See Section 4.7.2, "I/O Pad V_{DD33} Current Specifications," for information on both fast (F, FS) and medium (MH) pads. Also refer to Table 16 for values to calculate power dissipation for specific operation.

[15] This value is a target that is subject to change.

[16] This value allows a 5 V reference to supply ADC + REF.

[17] Power requirements for each I/O segment depend on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Section 4.7.1, "I/O Pad Current Specifications," for information on I/O pad power. Also refer to Table 15 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[18] Absolute value of current, measured at V_{IL} and V_{IH}.

[19] Absolute value of current, measured at V_{IL} and V_{IH}.

[20] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types F and MH.

[21] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to pad types AE and AE/up-down. See Appendix A, Signal Properties and Muxing.

[22] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics

[23] Pull-up and pull-down resistances are both enabled and settings are equal.

4.7.1 I/O Pad Current Specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 15 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 15.

The AC timing of these pads are described in the Section 4.11.2, "Pad AC Specifications."

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{DRV_MH}	50	50	5.25	11	16.0
2			20	50	5.25	01	6.3
3			3.0	50	5.25	00	1.1
4			2.0	200	5.25	00	2.4
5	Fast	I_{DRV_FC}	66	10	3.6	00	7.4
6			66	20	3.6	01	10.5
7			66	30	3.6	10	12.3
8			66	50	3.6	11	35.2

Table 15. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1] (continued)

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
9	Fast w/ Slew Control	I_{DRV_FSR}	66	50	3.6	11	12.7
10			50	50	3.6	10	6.7
11			33.33	50	3.6	01	4.2
12			20	50	3.6	00	2.6
13			20	200	3.6	00	9.1

1 These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

2 All loads are lumped.

4.7.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The V_{DD33} current draw on fast speed pads can be calculated from Table 16 dependent on the voltage, frequency, and load on all F type pins. The V_{DD33} current draw on medium pads can be calculated from Table 16 dependent on voltage and independent on the frequency and load on all MH type pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 16.

The AC timing of these pads are described in the Section 4.11.2, “Pad AC Specifications.”

Table 16. V_{DD33} Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{33_MH}	—	—	3.6	5.5	—	0.0007
2	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.92
3			66	20	3.6	3.6	01	1.14
4			66	30	3.6	3.6	10	1.50
5			66	50	3.6	3.6	11	2.19
6	Fast w/ Slew Control	I_{33_FSR}	66	50	3.6	3.6	11	0.74
7			50	50	3.6	3.6	10	0.52
8			33.33	50	3.6	3.6	00	0.19
9			20	50	3.6	3.6	00	0.19
10			20	200	3.6	3.6	00	0.19

1 These are average IDDE for worst case PVT from simulation. Currents apply to output pins only for the fast pads and to input pins only for the medium pads.

2 All loads are lumped.

4.7.3 LVDS Pad Specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

Table 17. DSPI LVDS pad specification

#	Characteristic	Symbol	Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate							
1	Data Frequency	$f_{LVDSCLK}$	—	—	50	—	MHz
Driver Specs							
2	Differential output voltage	V_{OD}	SRC=0b00 or 0b11	150	—	400	mV
			SRC=0b01	90	—	320	
			SRC=0b10	160	—	480	
3	Common mode voltage (LVDS), VOS	V_{OS}	—	1.06	1.2	1.39	V
4	Rise/Fall time	T_R/T_F	—	—	2	—	ns
5	Propagation delay (Low to High)	T_{PLH}	—	—	4	—	ns
6	Propagation delay (High to Low)	T_{PHL}	—	—	4	—	ns
7	Delay (H/L), sync Mode	t_{PDSYNC}	—	—	4	—	ns
8	Delay, Z to Normal (High/Low)	T_{DZ}	—	—	500	—	ns
9	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	—	—	—	0.5	ns
Termination							
10	Trans. Line (differential Zo)	—	—	95	100	105	ohms
11	Temperature	—	—	–40	—	150	°C

4.8 Oscillator and FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[2] (Normal Mode) Crystal Reference (PLLCFG2 = 0b0) Crystal Reference (PLLCFG2 = 0b1) External Reference (PLLCFG2 = 0b0) External Reference (PLLCFG2 = 0b1)	 $f_{ref_crystal}$ $f_{ref_crystal}$ f_{ref_ext} f_{ref_ext}	 8 16 8 16	 20 40[3] 20 40	MHz
2	Loss of Reference Frequency[4]	f_{LOR}	100	1000	kHz
3	Self Clocked Mode Frequency[5]	f_{SCM}	4	16	MHz
4	PLL Lock Time[6]	t_{LPLL}	—	< 400	µs

Table 18. FMPLL Electrical Specifications[1] (continued)

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
5	Duty Cycle of Reference [7]	t_{DC}	40	60	%
6	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
7	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
8	D_CLKOUT Period Jitter[8, 9] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{clkout}
9	Peak-to-Peak Frequency Modulation Range Limit [10,11] (f_{sys} Max must not be exceeded)	C_{mod}	0	4	%f_{sys}
10	FM Depth Tolerance[12]	C_{mod_err}	–0.25	0.25	%f_{sys}
11	VCO Frequency	f_{VCO}	192	600	MHz
12	Modulation Rate Limits[13]	f_{mod}	0.400	1	MHz
13	Predivider output frequency range[14]	f_{prediv}	4	10	MHz

1 All values given are initial design targets and subject to change.

2 Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

3 Upper tolerance of less than 1% is allowed on 40MHz crystal.

4 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

5 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured at D_CLKOUT. A default RFD value of (0x05) is used in SCM mode, and the programmed MFD and RFD values have no effect

6 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

7 For Flexray operation, duty cycle requirements are higher.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval. D_CLKOUT divider set to divide-by-2.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

10 Modulation depth selected must not result in f_{pll} value greater than the f_{pll} maximum specified value.

11 Maximum and minimum variation from programmed modulation depth is pending characterization. Depth settings available in control register are: 2%, 3%, and 4% peak-to-peak.

12 Depth tolerance is the programmed modulation depth ±0.25% of F_{sys}. Violating the VCO min/max range may prevent the system from exiting reset.

13 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

14 Violating this range will cause the VCO max/min range to be violated with the default MFD settings out of reset.

Table 19. Oscillator Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Crystal Mode Differential Amplitude[2] (Min differential voltage between EXTAL and XTAL)	$V_{crystal_diff_amp}$	$\lvert V_{extal} - V_{xtal} \rvert$ > 0.4 V	—	V
2	Crystal Mode: Internal Differential Amplifier Noise Rejection	$V_{crystal_diff_amp_nr}$	—	$\lvert V_{extal} - V_{xtal} \rvert$ < 0.2 V	V
3	EXTAL Input High Voltage Bypass mode, External Reference	V_{IHEXT}	((V_{DD33}/2) + 0.4 V)	—	V
4	EXTAL Input Low Voltage Bypass mode, External Reference	V_{ILEXT}	—	(V_{DD33}/2) – 0.4 V	V
5	XTAL Current[3]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	($2 \times C_L - C_{S_EXTAL} - C_{PCB_EXTAL}$[4])	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	($2 \times C_L - C_{S_XTAL} - C_{PCB_XTAL}$[4])	pF

1 All values given are initial design targets and subject to change.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criterion has to be met for oscillator's comparator to produce output clock.

3 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

4 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

4.9 eQADC Electrical Characteristics

Table 20. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles Single Ended Conversion Cycles 12 bit resolution Single Ended Conversion Cycles 10 bit resolution Single Ended Conversion Cycles 8 bit resolution **Note:** Differential conversion (min) is one clock cycle less than the single-ended conversion values listed here.	CC	 2 + 14 2 + 12 2 + 10	 128 + 14 128 + 12 128 + 10	ADCLK cycles
3	Stop Mode Recovery Time[1]	T_{SR}	10	—	µs
4	Resolution[2]	—	1.25	—	mV
5	INL: 8 MHz ADC Clock[3]	INL8	–4[4]	4[4]	LSB[5]
6	INL: 16 MHz ADC Clock[3]	INL16	–8[4]	8[4]	LSB
7	DNL: 8 MHz ADC Clock[3]	DNL8	–3[4]	3[4]	LSB
8	DNL: 16 MHz ADC Clock[3]	DNL16	–3[4]	3[4]	LSB

Table 20. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Non-Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–3	3	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	–4[4]	4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	–4[4,6]	4[4,6]	Counts
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	–8	8	Counts
17	Maximum differential voltage[15] (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	 $DIFF_{max}$ $DIFF_{max2}$ $DIFF_{max4}$	 — — —	 $(V_{RH} – V_{RL})/2$ $(V_{RH} – V_{RL})/4$ $(V_{RH} - V_{RL})/8$	 V V V
18	Differential input Common mode voltage[15] (DANx- + DANx+)/2	$DIFF_{cmv}$	$(V_{RH} – V_{RL})/2$ – 5%	$(V_{RH} – V_{RL})/2$ + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

4.9.1 ADC Internal Resource Measurements

Table 21. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	—	0.62	—	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	—	1.22	—	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	—	V_{DD} / 2.045	—	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	—	V_{DD} / 1.774	—	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	—	Vreg3p3 / 5.460	—	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	—	Vreg3p3 / 4.758	—	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	—	 V_{DDREG} / 4.758 V_{DDREG}/7.032	—	V

Table 22. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias 150 mV to 360 mV (30mV Increment @ vref_sel) ADC1 channel 195 Default Value 150 mV (@vref_sel = 1 1 1)	V_{ADC195}	150	—	360	mV
3	Standby Brownout Reference ADC1 channel 195	V_{ADC195}	500	—	850	mV

Table 23. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 24. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 25. Flash Program and Erase Specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

Table 26. Flash EEPROM Module Life

Spec	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of program/erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
2	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	P/E	1,000	100,000	cycles
3	Minimum Data Retention at 85 °C ambient temperature[2] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	Retention	 20 10 5	 — — —	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the NXP definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 27 shows the Platform Flash Configuration Register 1 (PFCPR1) settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 27. PFCPR1 Settings vs. Frequency of Operation[1]

Spec	Clock Mode	Maximum Frequency[2] (MHz)		APC = RWSC	WWSC	DPFEN[3]	IPFEN[3]	PFLIM[4]	BFEN[5]
		Core f_{sys}	Platform f_{platf}						
1	Enhanced	264 MHz[6]	132 MHz[6]	0b011	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
2	Enhanced/ Full	200 MHz	100 MHz	0b010	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
3	Legacy	132 MHz	132 MHz	0b100	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
Default setting after reset:				0b111	0b11	0b00	0b00	0b00	0b0

1 Illegal combinations exist. Use entries from the same row in this table.

2 This is the nominal maximum frequency of operation: platform runs at $f_{sys}/2$ in Enhanced Mode .

3 For maximum flash performance, set to 0b1.

4 For maximum flash performance, set to 0b10.

5 For maximum flash performance, set to 0b1.

6 This is the nominal maximum frequency of operation in Enchanced Mode. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system core clock(f_{sys}) + 2% FM and 132 Mhz platform clock (f_{platf})+ 2% FM.

4.11 AC Specifications

4.11.1 Clocking

The Figure 16 shows the operating frequency domains of various blocks on MPC5674F.

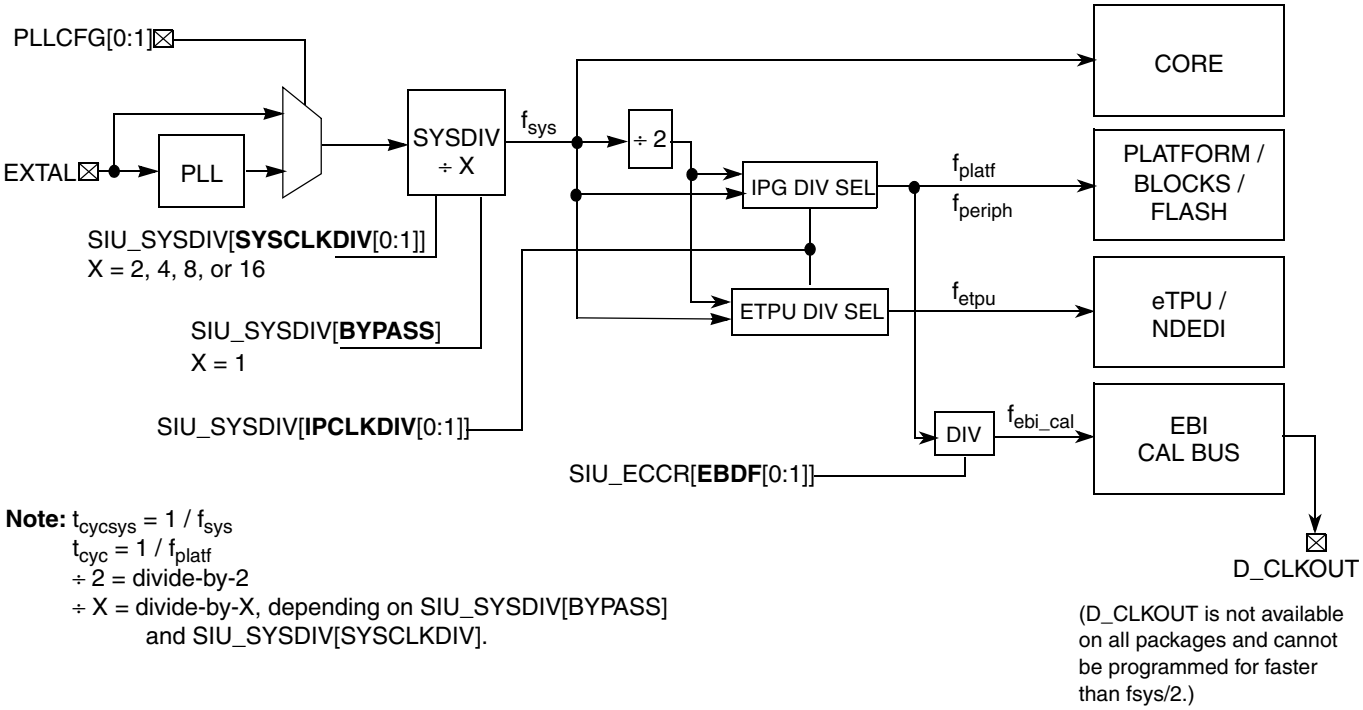


Figure 16. MPC5674F Block Operating Frequency Domain Diagram

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 29 and Table 30 for descriptions of bit settings).

Table 28. MPC5674F Operating Frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

2 Up to the maximum frequency rating of the device (refer to Table 1). The f_{sys} speed is the nominal maximum frequency. 270 Mhz parts allow for 264 Mhz system clock + 2% FM.

3 See the *MPC5674F Reference Manual* for full description as not all bit combinations are valid.

4 EBI/Calibration bus is not available in all packages.

5 The EBI/Calibration Bus operating frequency, f_{ebi_cal} , depends on clock divider settings of block's max allowed frequency of operation. Normally $f_{ebi_cal} = f_{platf}$ /2, but can be limited to < f_{platf} /2 in Full Mode.

Table 29. IPCLKDIV Settings

SIU_SYSDIV [IPCLKDIV[0:1]]	Mode	Description
00	Enhanced	CPU frequency is doubled (Max 264Mhz). Platform, peripheral, and eTPU clocks are 1/2 of CPU frequency
01	Full	CPU and eTPU frequency is doubled (Max 200Mhz). Platform and peripheral clocks are 1/2 of CPU frequency.
10	—	Reserved
11	Legacy	CPU, eTPU, platform, and peripheral's clocks all run at same speed (Max 132Mhz).

Table 30. SYSCLKDIV Settings

SIU_SYSDIV [SYSCLKDIV[0:1]]	Description
00	Divide by 2.
01	Divide by 4.
10	Divide by 8.
11	Divide by 16.

4.11.2 Pad AC Specifications

Table 31. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200
7	Fast[6]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	2.6
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

6 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 32. Derated Pad AC Specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Out delay is shown in Figure 17. Add a maximum of one system clock to the output delay for delay with respect to system clock.

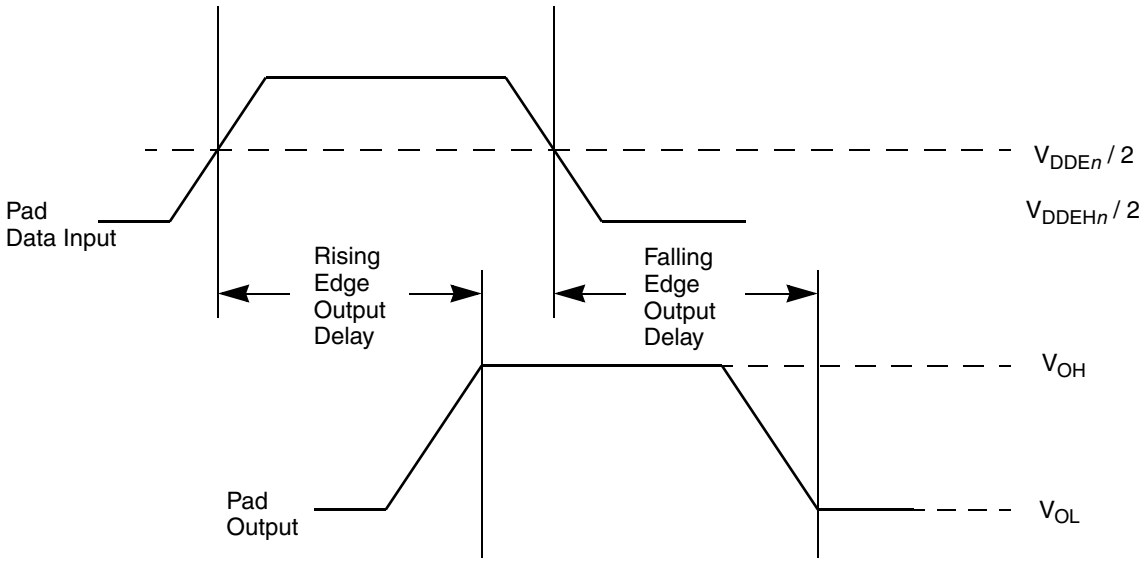


Figure 17. Pad Output Delay

4.12 AC Timing

4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 18 and Figure 19 apply to all I/O pins with pad types F and MH. See Appendix A, Signal Properties and Muxing, for the pad type for each pin.

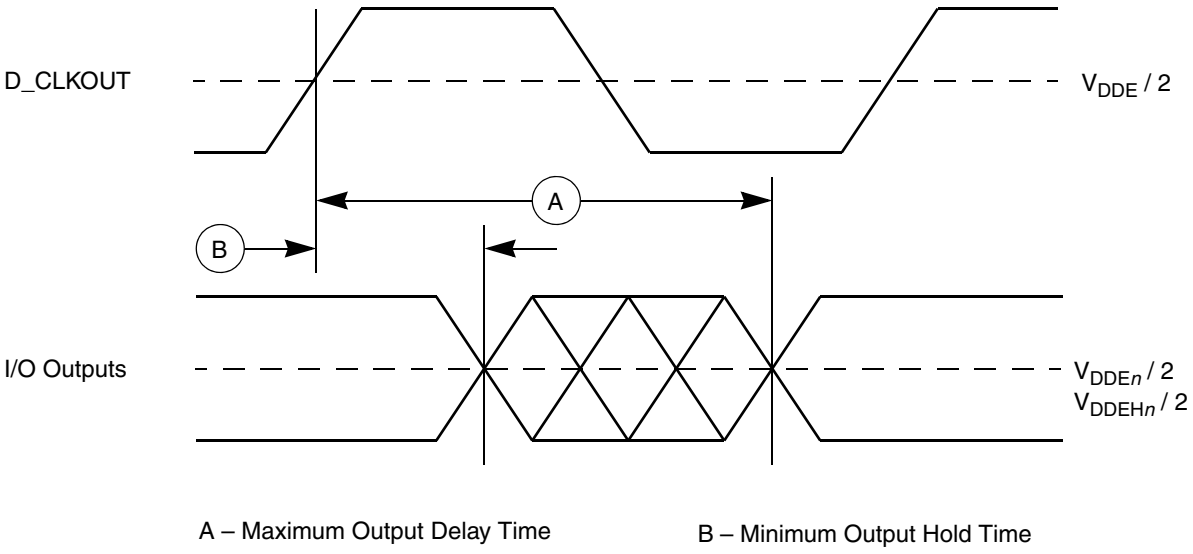


Figure 18. Generic Output Delay/Hold Timing

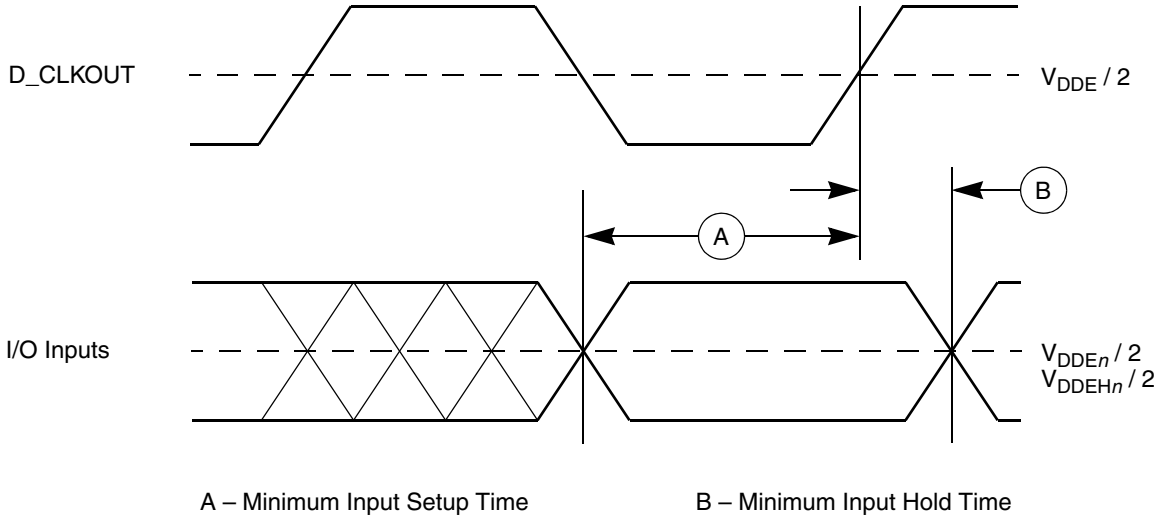


Figure 19. Generic Input Setup/Hold Timing

4.12.2 Reset and Configuration Pin Timing

Table 33. Reset and Configuration Pin Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

[1] Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

[2] See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1, "Clocking."

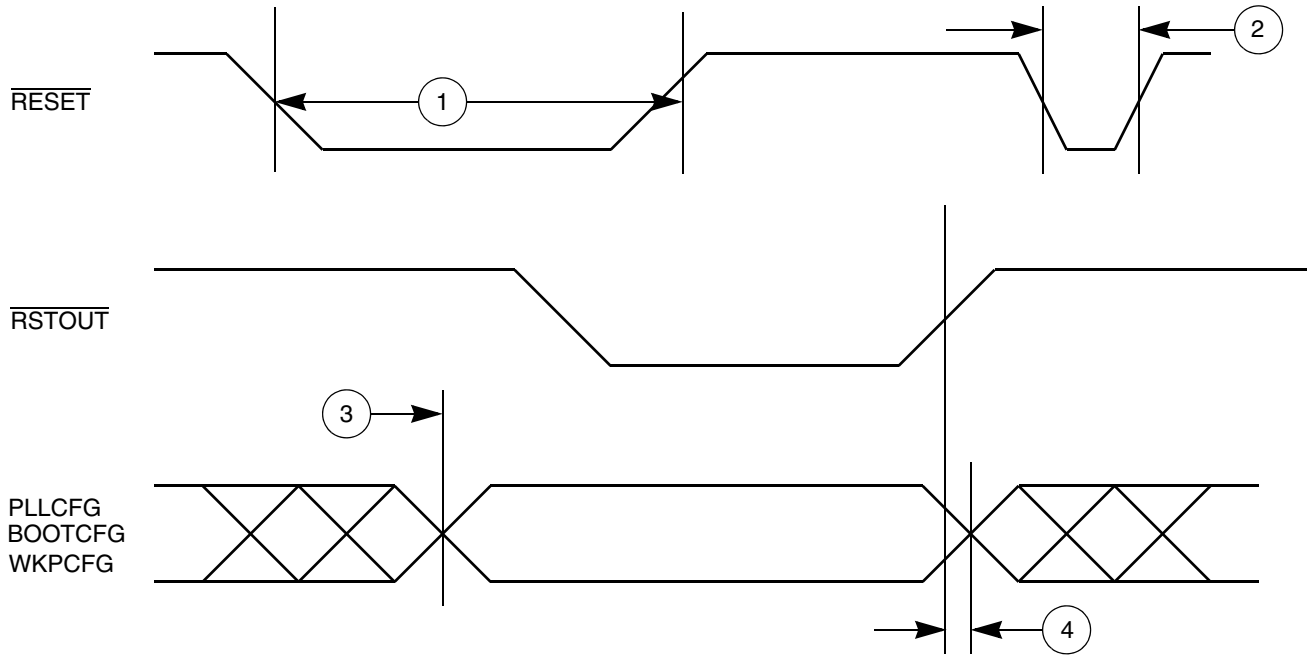


Figure 20. Reset and Configuration Pin Timing

4.12.3 IEEE 1149.1 Interface Timing

Table 34. JTAG Pin AC Electrical Characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] JTAG timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 35 for functional specifications.

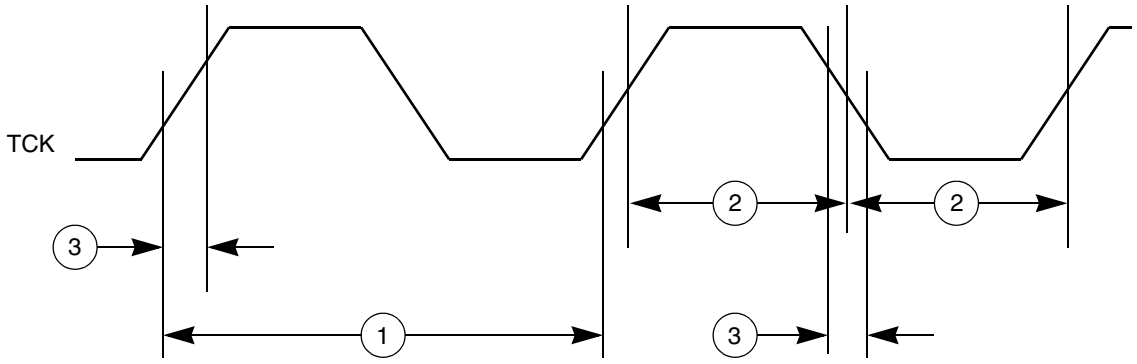


Figure 21. JTAG Test Clock Input Timing

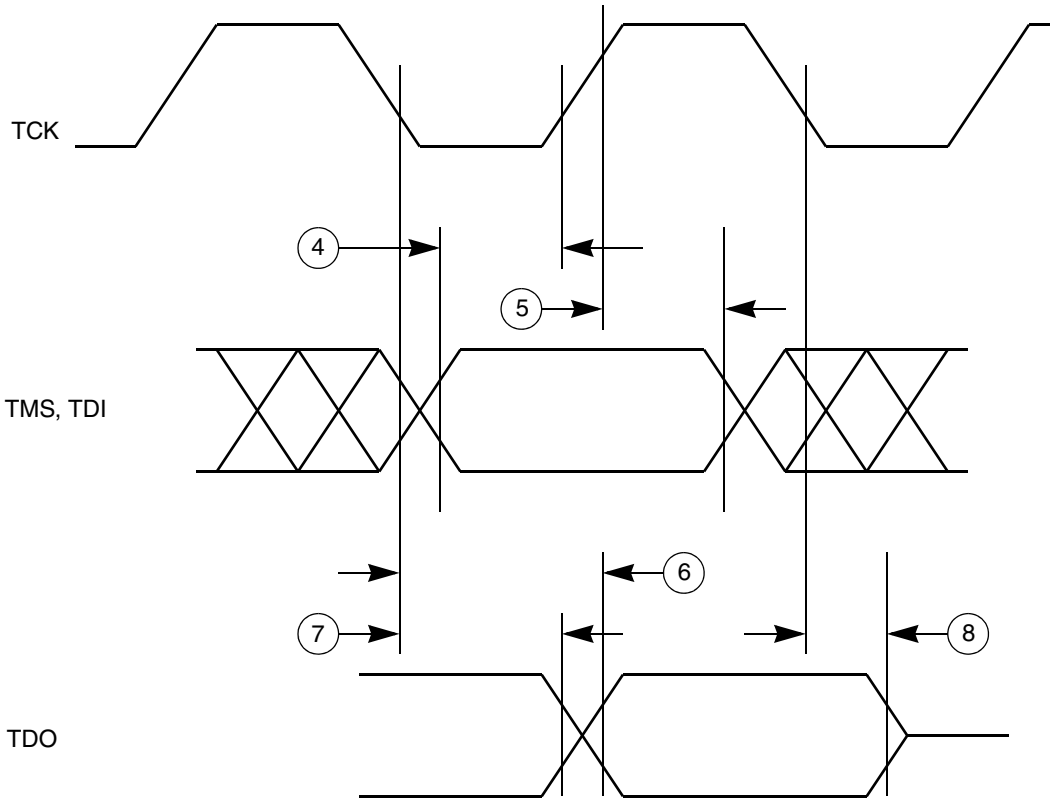


Figure 22. JTAG Test Access Port Timing

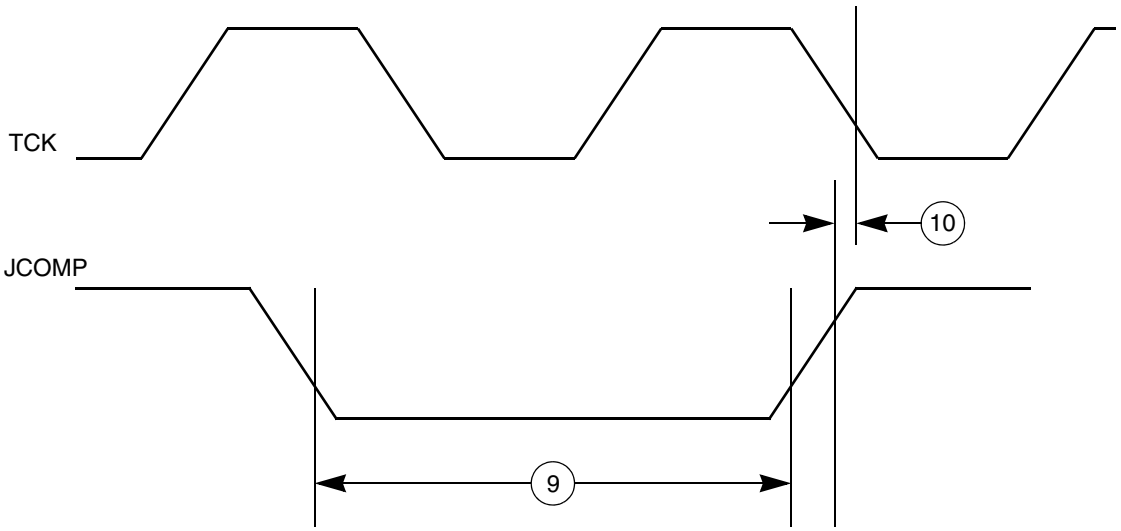


Figure 23. JTAG JCOMP Timing

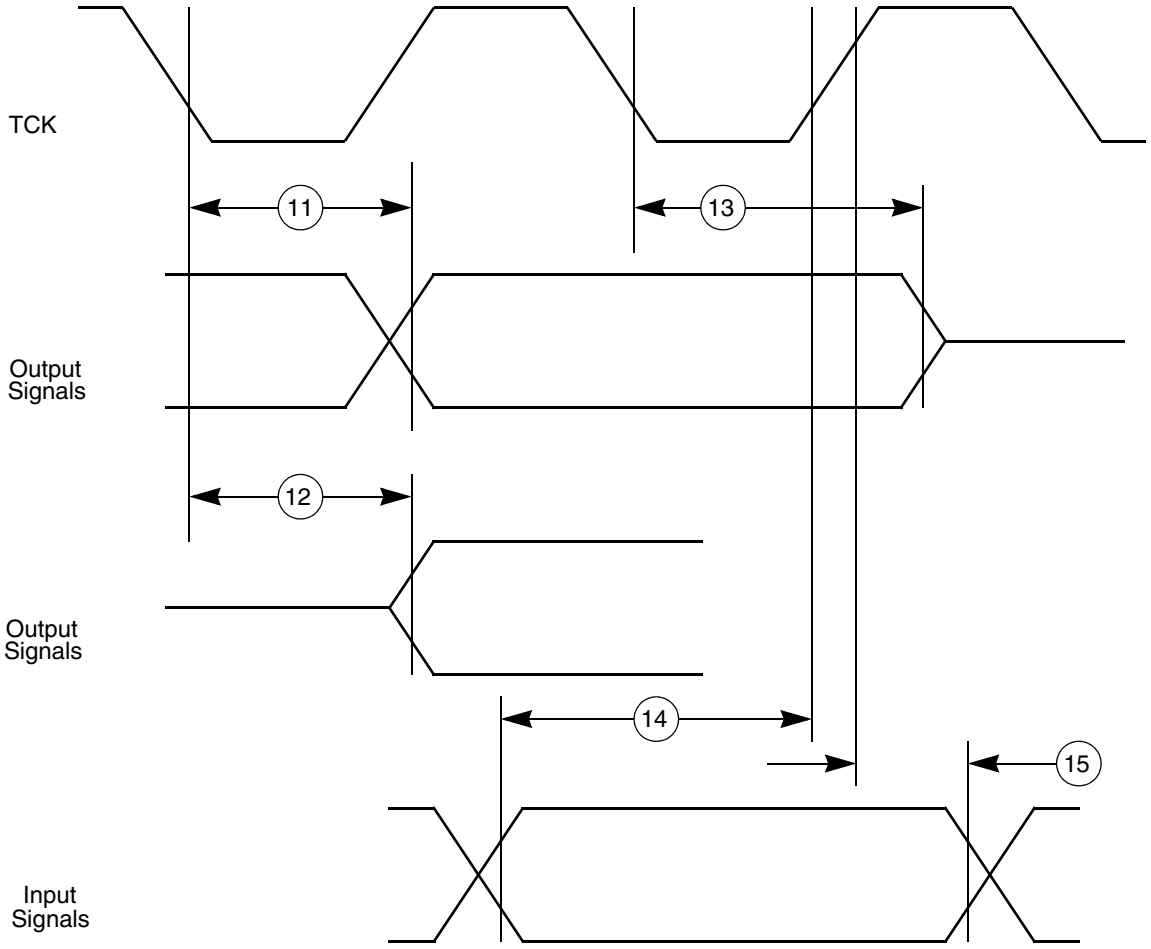


Figure 24. JTAG Boundary Scan Timing

4.12.4 Nexus Timing

Table 35. Nexus Debug Port Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2[2]	8	t_{CYC}[3]
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[4]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[4]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[4]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}[3]
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4[5]	—	t_{CYC}[3]
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{NTDOV}	0	10	ns
13	$\overline{\text{RDY}}$ Valid to MCKO[6]	—	—	—	—

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC_PCR[MKCO_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

3 See Notes on t_{cyc} in Table 28 in Section 4.11.1 Clocking.

4 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

5 Lower frequency is required to be fully compliant to standard.

6 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

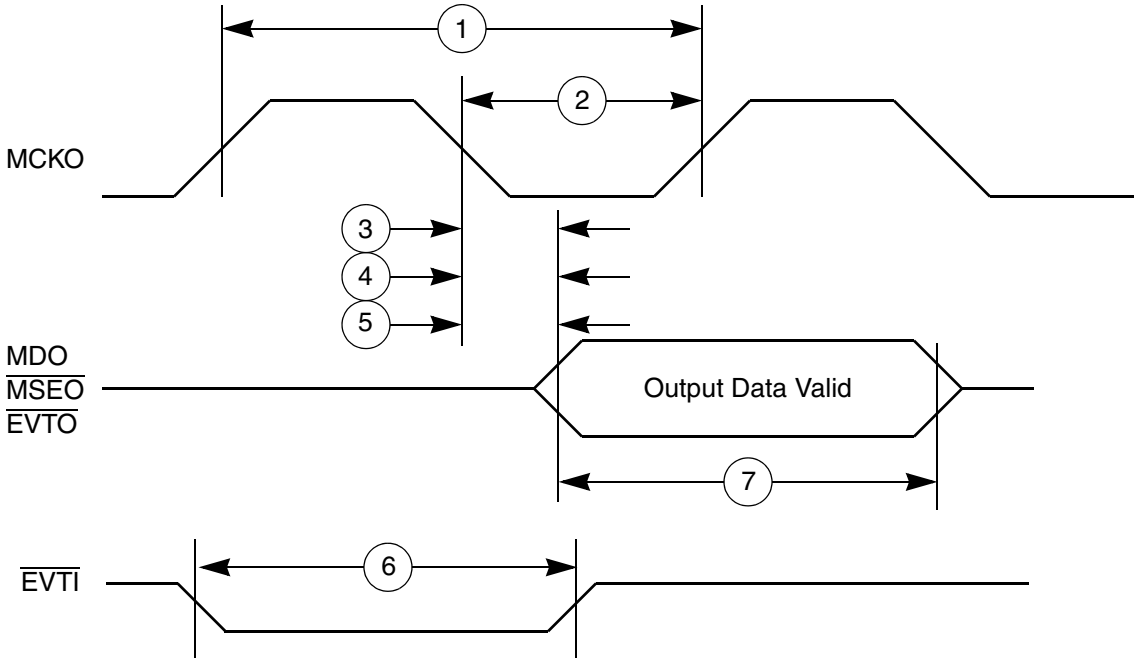


Figure 25. Nexus Timings

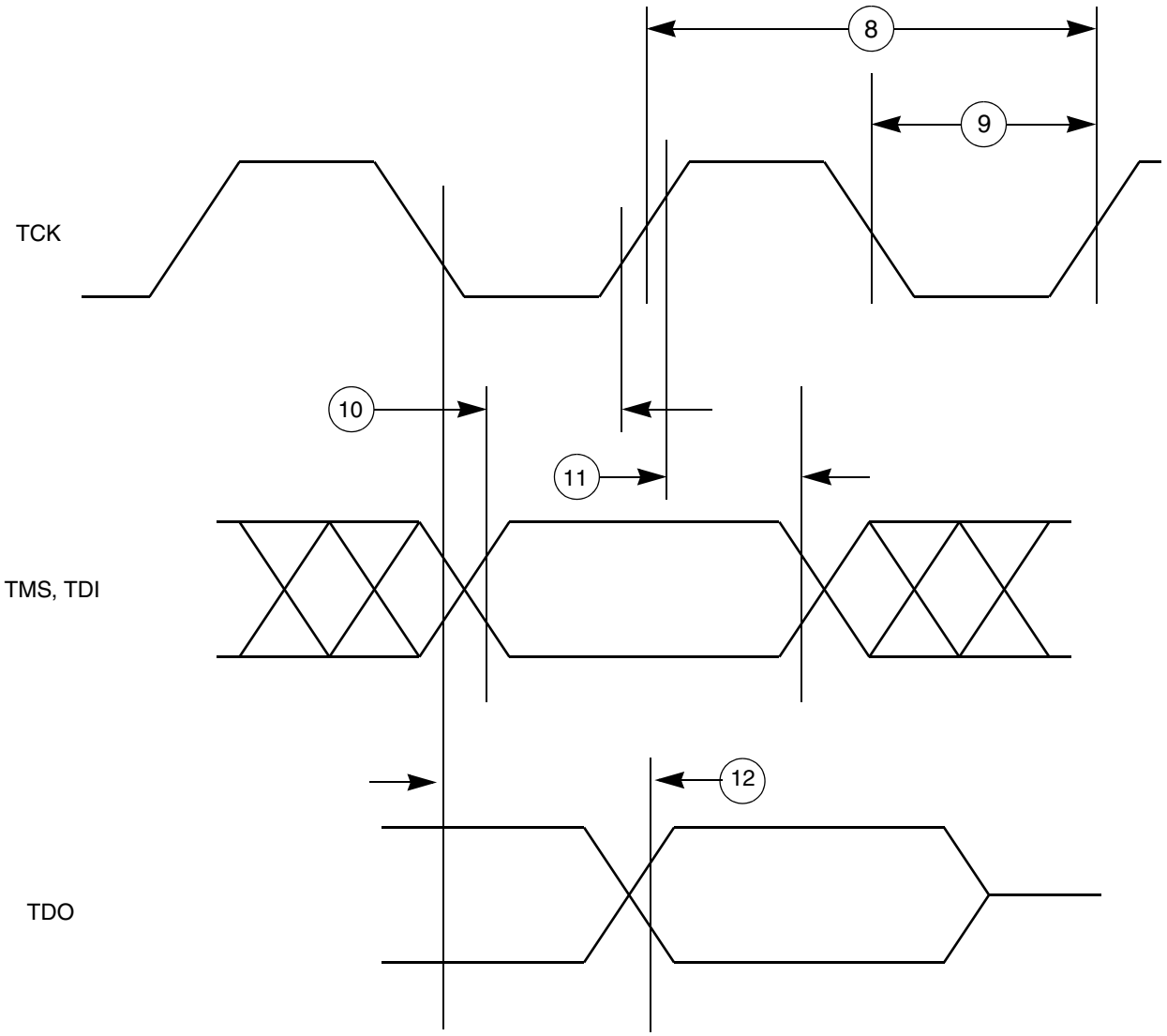


Figure 26. Nexus TCK, TDI, TMS, TDO Timing

4.12.5 External Bus Interface (EBI) Timing

Table 36. Bus Operation Timing [1]

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	7.0/7.5	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 7.0 ns EBTS = 1: 7.5 ns

Table 36. Bus Operation Timing [1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2 3]		Unit	Notes
			Min	Max		
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D_RD_WR}}$ D_TA D_TS	t_{CIS}	5.0/4.5	—	ns	Input setup time selectable via SIU_ECCR[EBTS] bit: EBTS = 0; 5.0ns EBTS = 1; 4.5ns
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D_RD_WR}}$ D_TA D_TS	t_{CIH}	1.0	—	ns	
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 [5]	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

1 EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

3 Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.

4 Refer to Fast pad timing in Table 31 and Table 32.

5 ALE hold time spec is temperature dependant. 1.0 ns spec applies for temperature range -40 to 0 °C. 2.0 ns spec applies to temperatures > 0 °C. This spec has no dependency on SIU_ECCR[EBTS] bit.

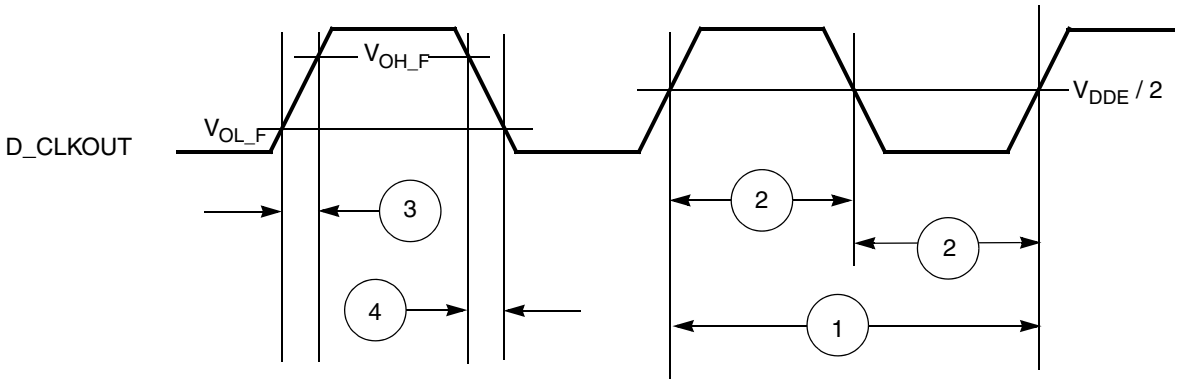


Figure 27. D_CLKOUT Timing

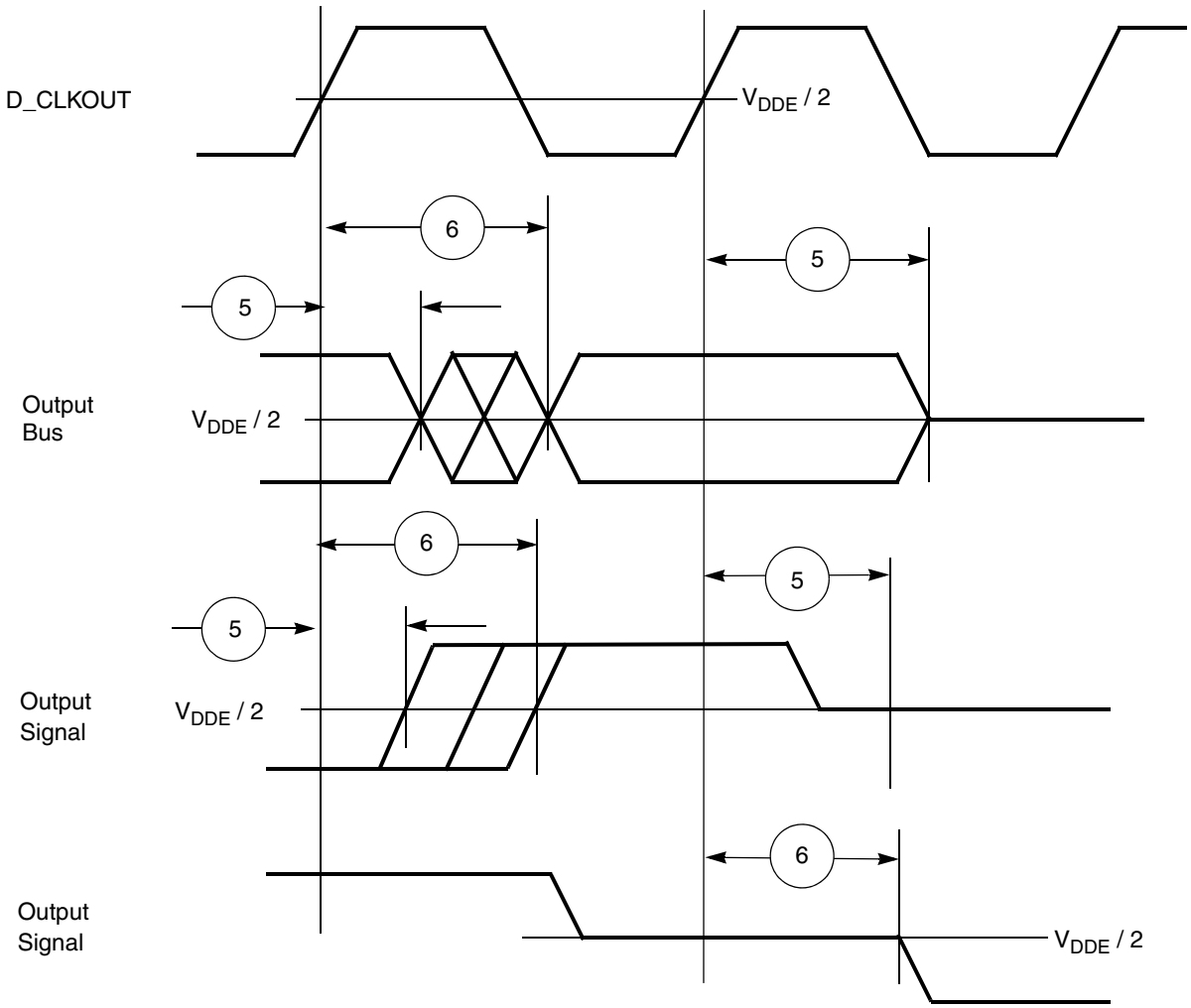


Figure 28. Synchronous Output Timing

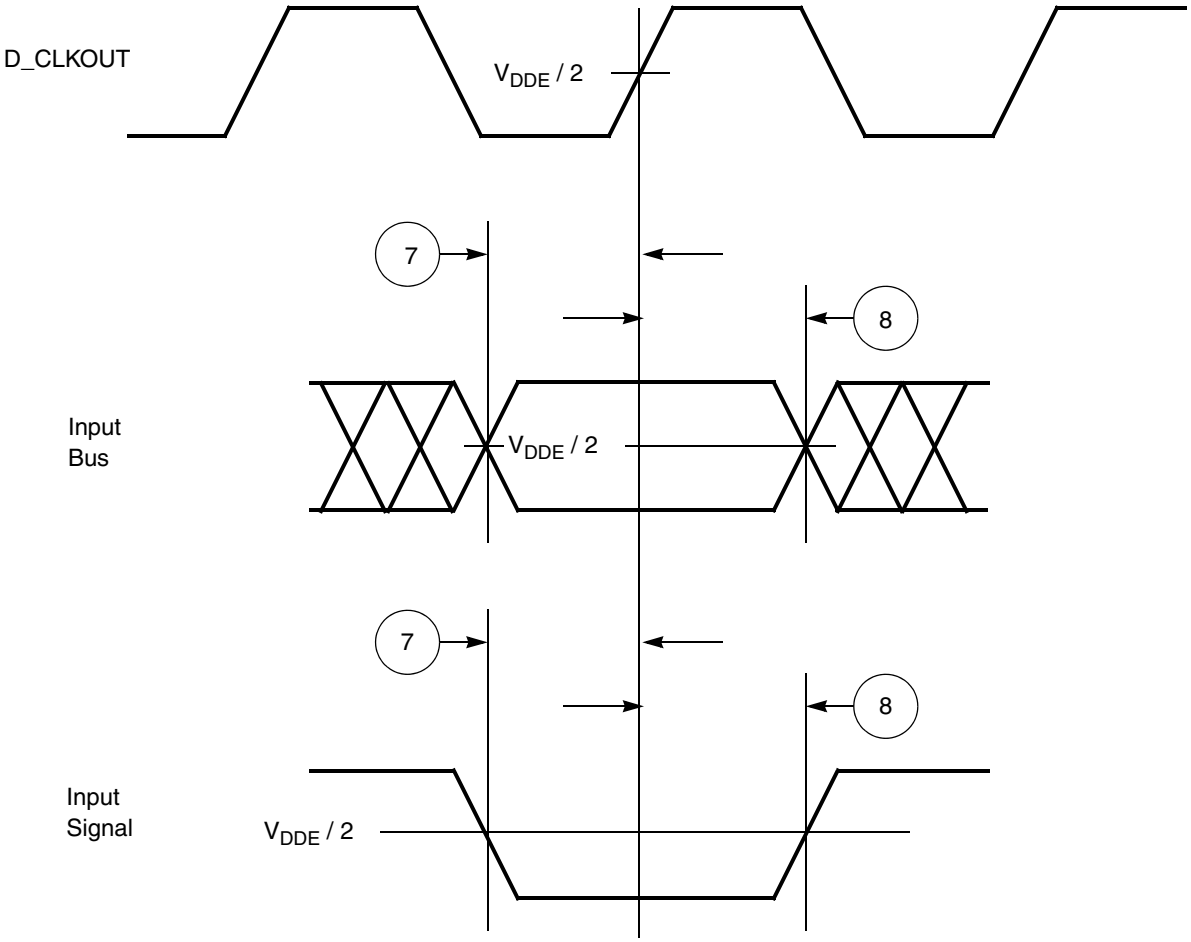


Figure 29. Synchronous Input Timing

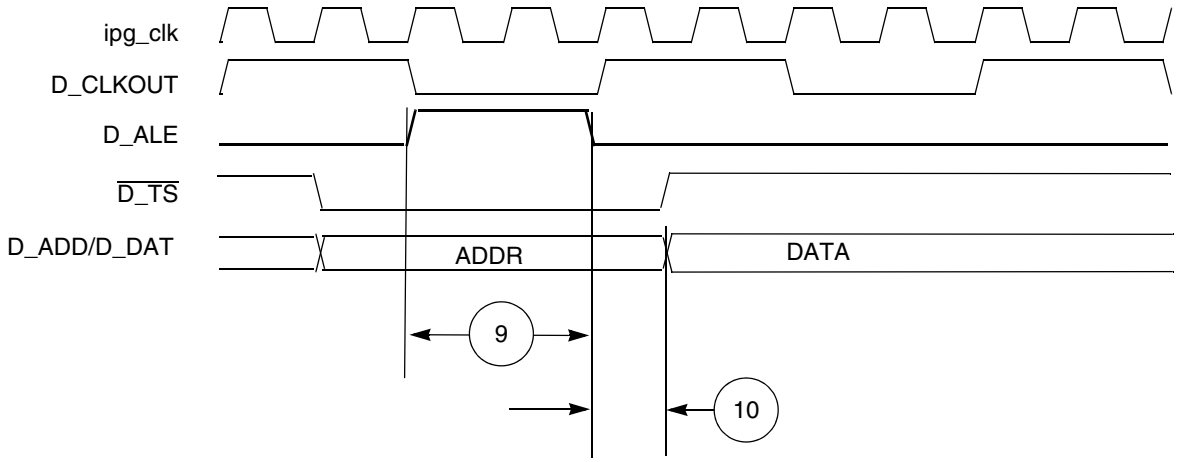


Figure 30. ALE Signal Timing

4.12.6 External Interrupt Timing (IRQ Pin)

Table 37. External Interrupt Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1 IRQ timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

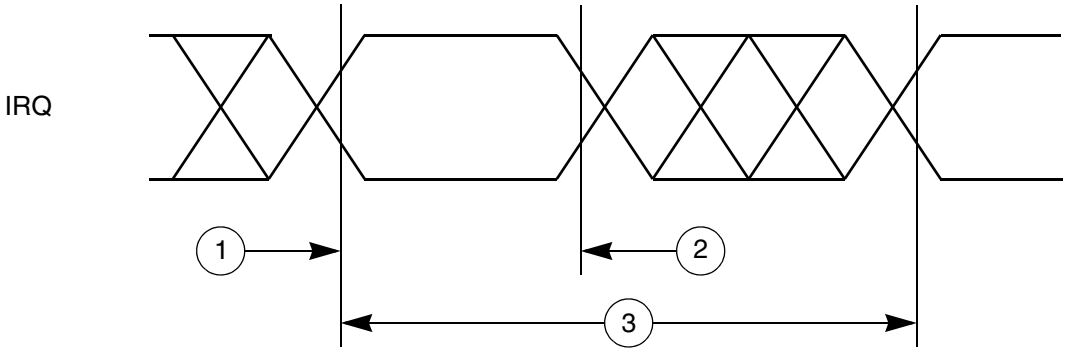


Figure 31. External Interrupt Timing

4.12.7 eTPU Timing

Table 38. eTPU Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{cyc}[2]

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

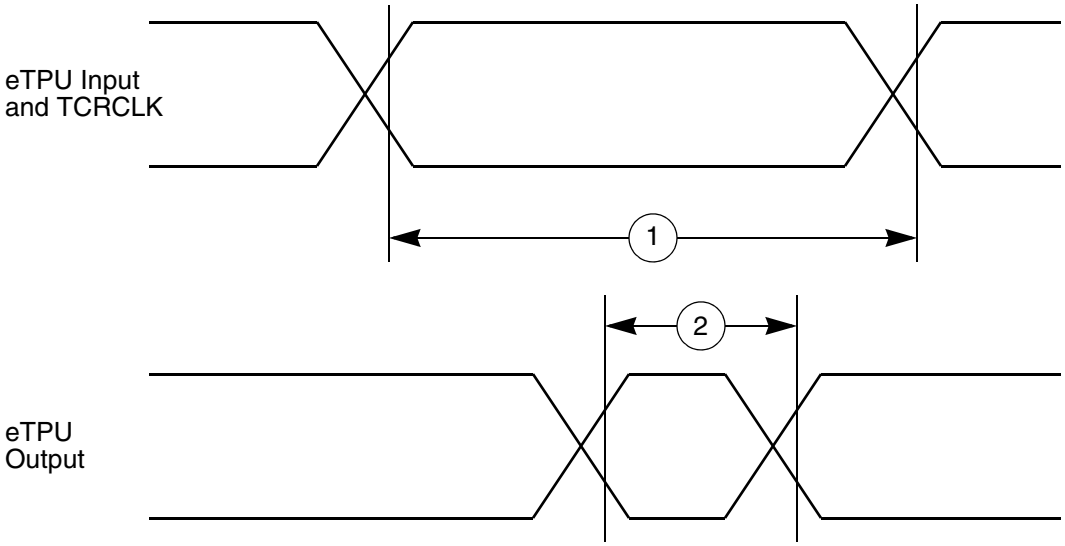


Figure 32. eTPU Timing

4.12.8 eMIOS Timing

Table 39. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 16 and Table 28 in Section 4.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

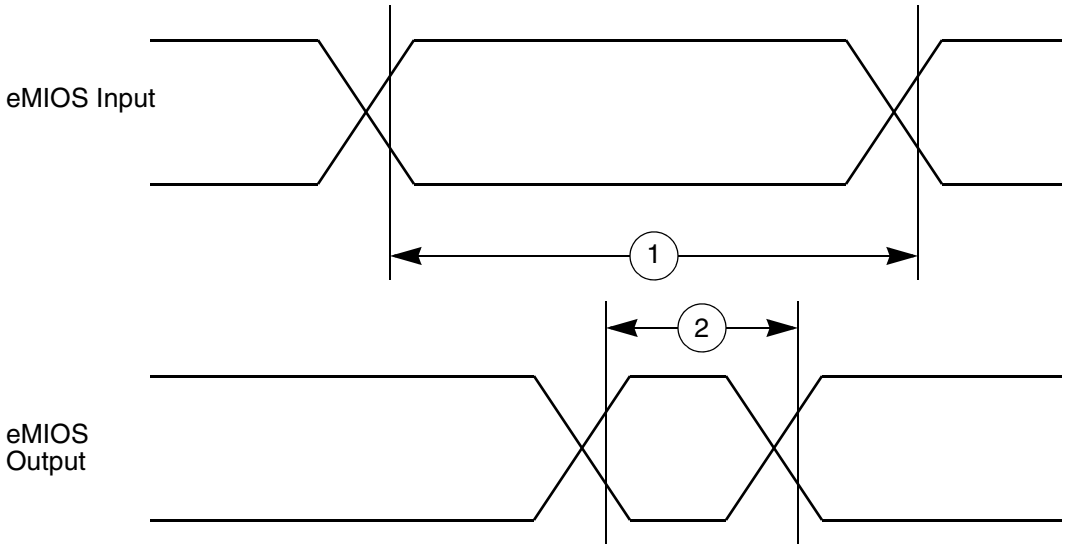


Figure 33. eMIOS Timing

4.12.9 DSPI Timing

Table 40. DSPI Timing[1] [2]

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
1	DSPI Cycle Time[3, 4] Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	t_{SYS} * 2	t_{SYS}*32768*7	ns
2	PCS to SCK Delay[5]	t_{CSC}	12	—	ns
3	After SCK Delay[6] Master mode Slave mode	t_{ASC}	t_{SYS} * 2 t_{SYS} *3 – constraints [7]	—	ns
4	SCK Duty Cycle	t_{SDC}	0.33 * t_{SCK}	0.66 * t_{SCK}	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	t_{SYS} * 2	t_{SYS} * 7	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	t_{SYS} * 2	t_{SYS} * 7	ns

Table 40. DSPI Timing[1] [2] (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[8] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 20 4 6 20	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[8] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –3 7 12 –3	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 5 25 13 5	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –5 2.5 3 –5	 — — — —	 ns ns ns ns

1 DSPI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, and $T_A = T_L$ to T_H

2 Speed is the nominal maximum frequency of platform clock (f_{platf}). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock (f_{sys}) + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

6 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

7 For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

8 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 41. DSPI LVDS Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit
LVDS Clock to Data/Chip Select Outputs	$t_{LVDSDATA}$	–0.25 × t_{SCYC}	+0.25 × t_{SCYC}	ns

1 These are typical values that are estimated from simulation.

2 See DSPI LVDS Pad related data in Table 17.

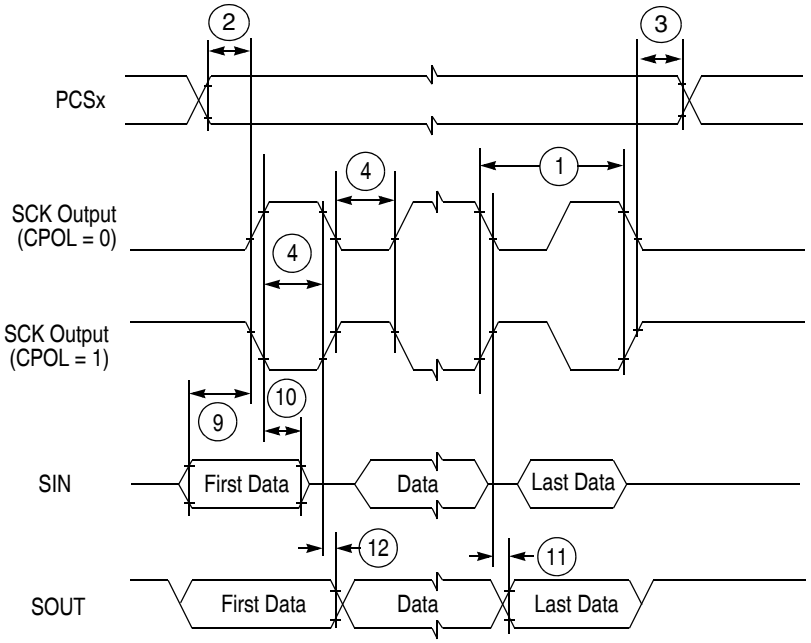


Figure 34. DSPI Classic SPI Timing — Master, CPHA = 0

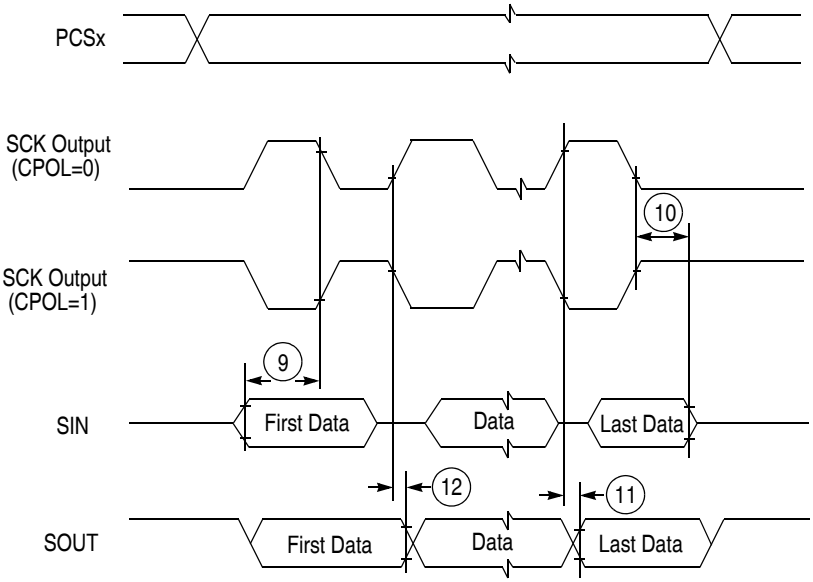


Figure 35. DSPI Classic SPI Timing — Master, CPHA = 1

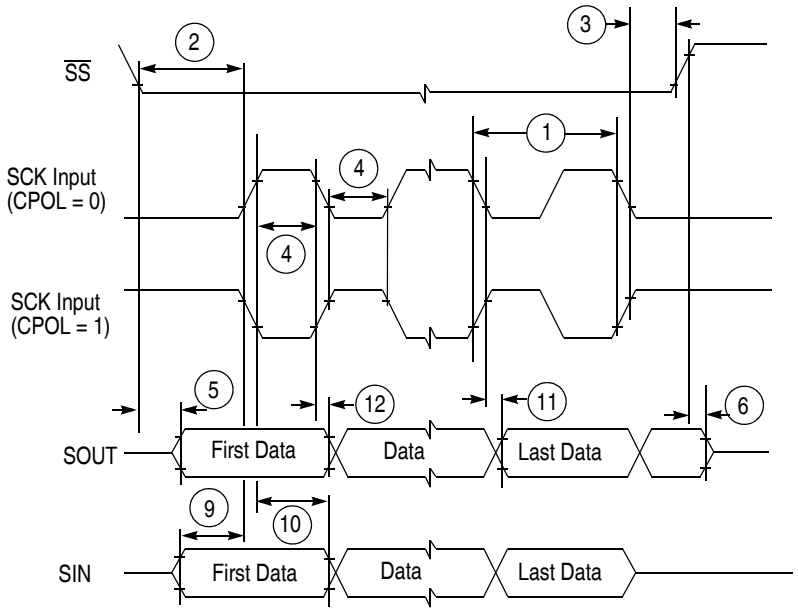


Figure 36. DSPI Classic SPI Timing — Slave, CPHA = 0

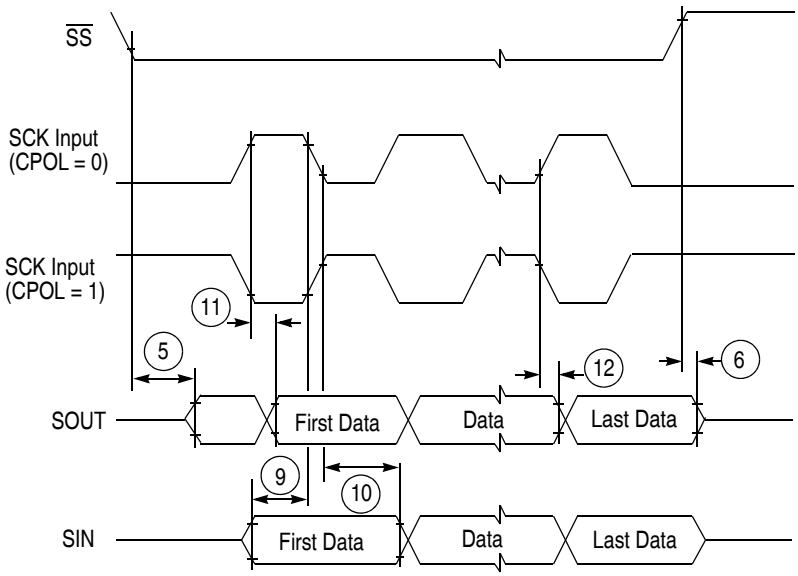


Figure 37. DSPI Classic SPI Timing — Slave, CPHA = 1

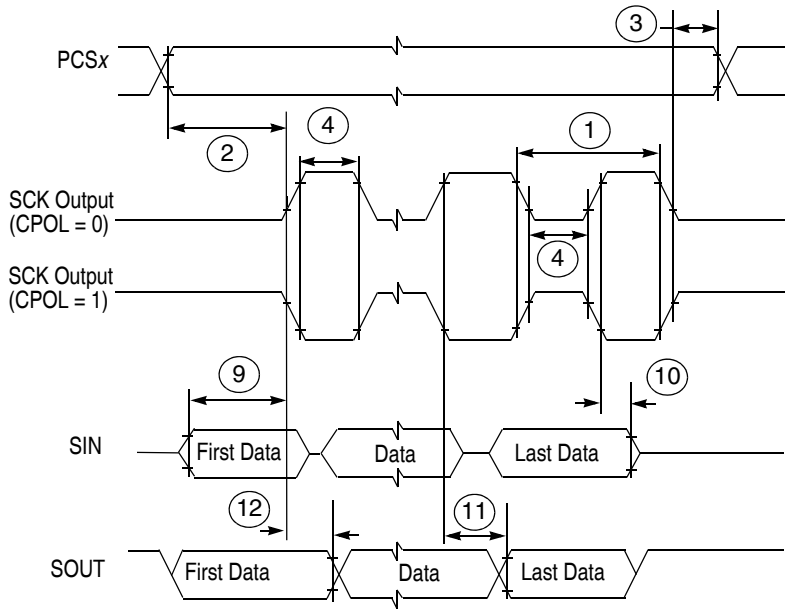


Figure 38. DSPI Modified Transfer Format Timing — Master, CPHA = 0

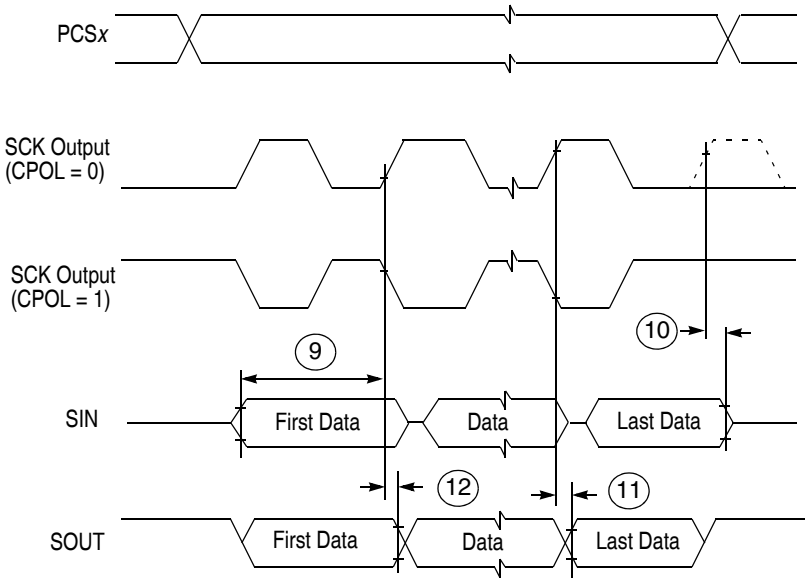


Figure 39. DSPI Modified Transfer Format Timing — Master, CPHA = 1

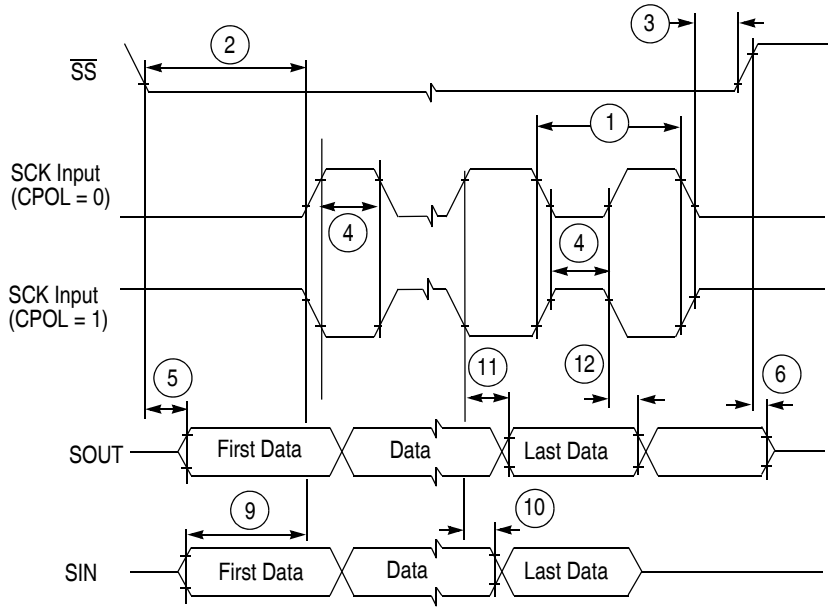


Figure 40. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

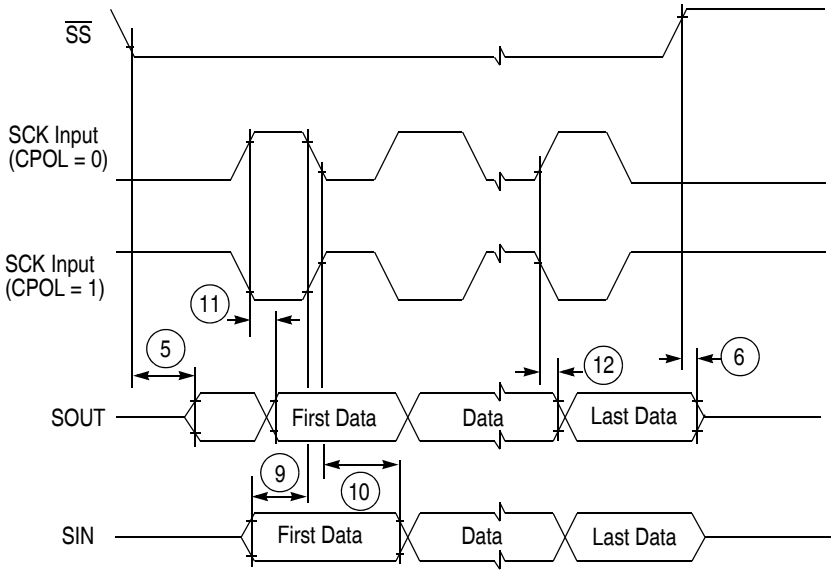


Figure 41. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

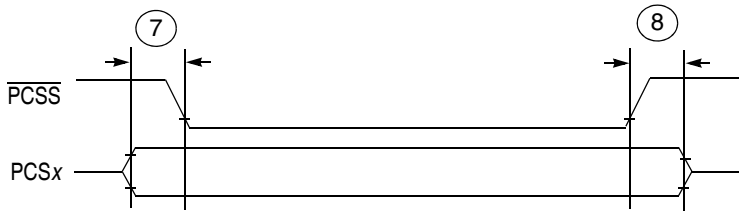


Figure 42. DSPI PCS Strobe (PCSS) Timing

5 Package Information

The latest package outline drawings are available on the product summary pages on our website: http://www.nxp.com/powerarchitecture. The following table lists the package case number. Use these numbers in the webpage's keyword search engine to find the latest package outline drawings.

Table 42. Package Information

Package Type	Case Outline Number
324 TEPBGA	98ASS23840W
416 TEPBGA	98ARE10523D
516 TEPBGA	98ARS10503D

5.1 324-Pin Package

The package drawings of the 324-pin TEPBGA package are shown in Figure 43 and Figure 44.

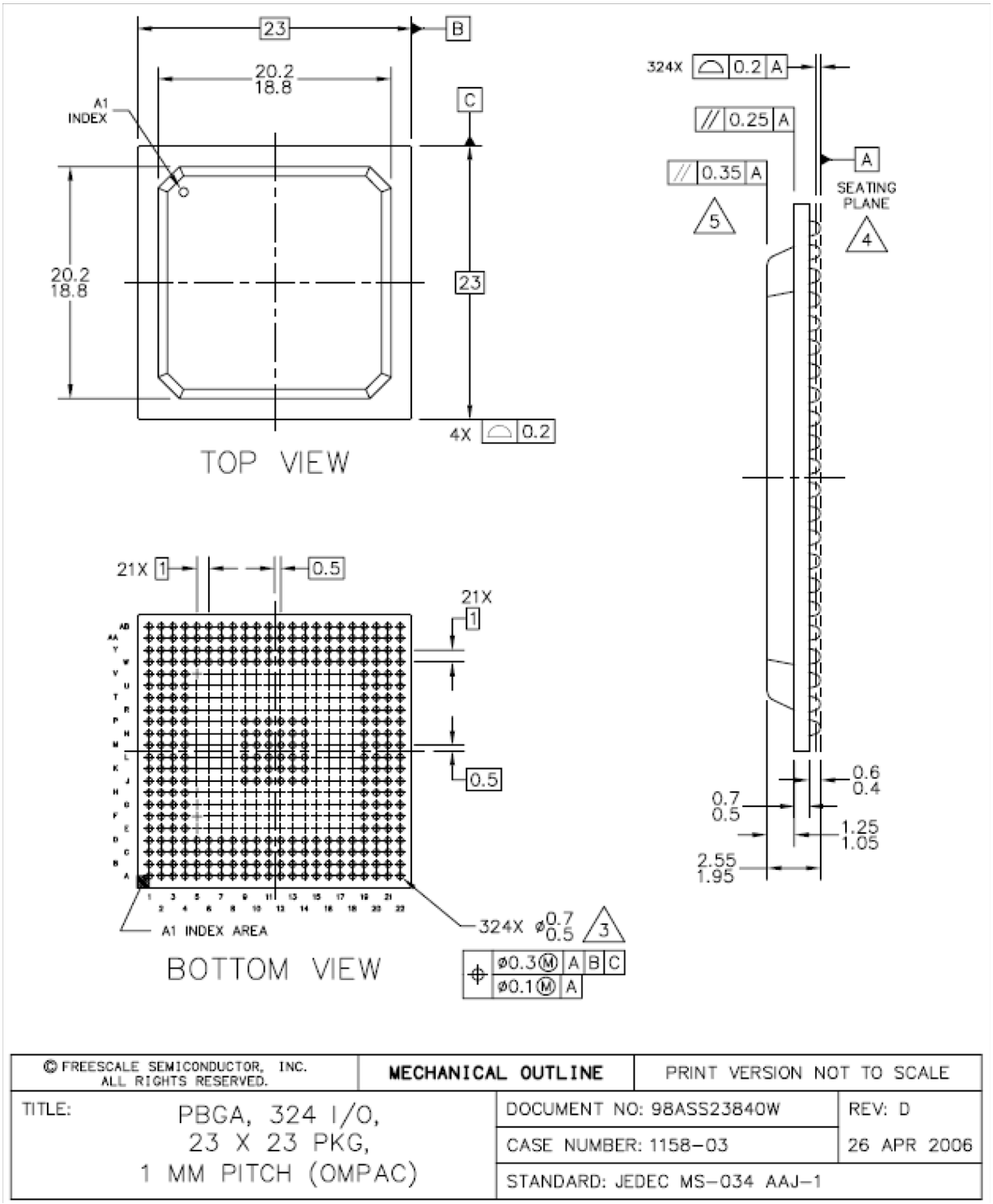


Figure 43. 324 TEPBGA Package (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASS23840W	REV: D
PBGA, 324 I/O, 23 X 23 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1158–03	26 APR 2006
	STANDARD: JEDEC MS–034 AAJ–1	

Figure 44. 324 TEPBGA Package (2 of 2)

5.2 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 45 and Figure 46.

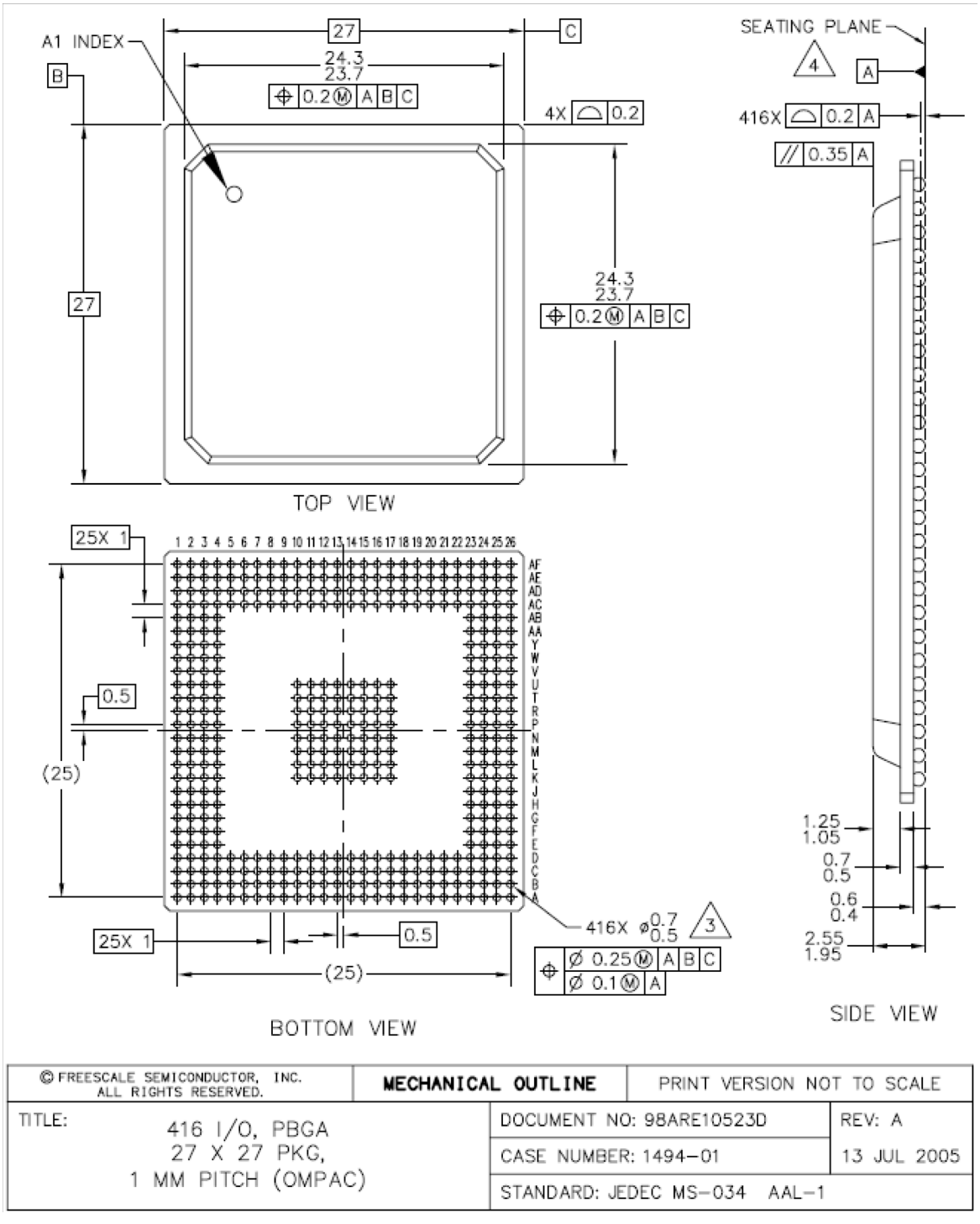

Figure 45. 416 TEPBGA Package (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ARE10523D	REV: A
416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1494–01	13 JUL 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 46. 416 TEPBGA Package (2 of 2)

5.3 516-Pin Package

The package drawings of the 516-pin TEPBGA package are shown in Figure 47 and Figure 48.

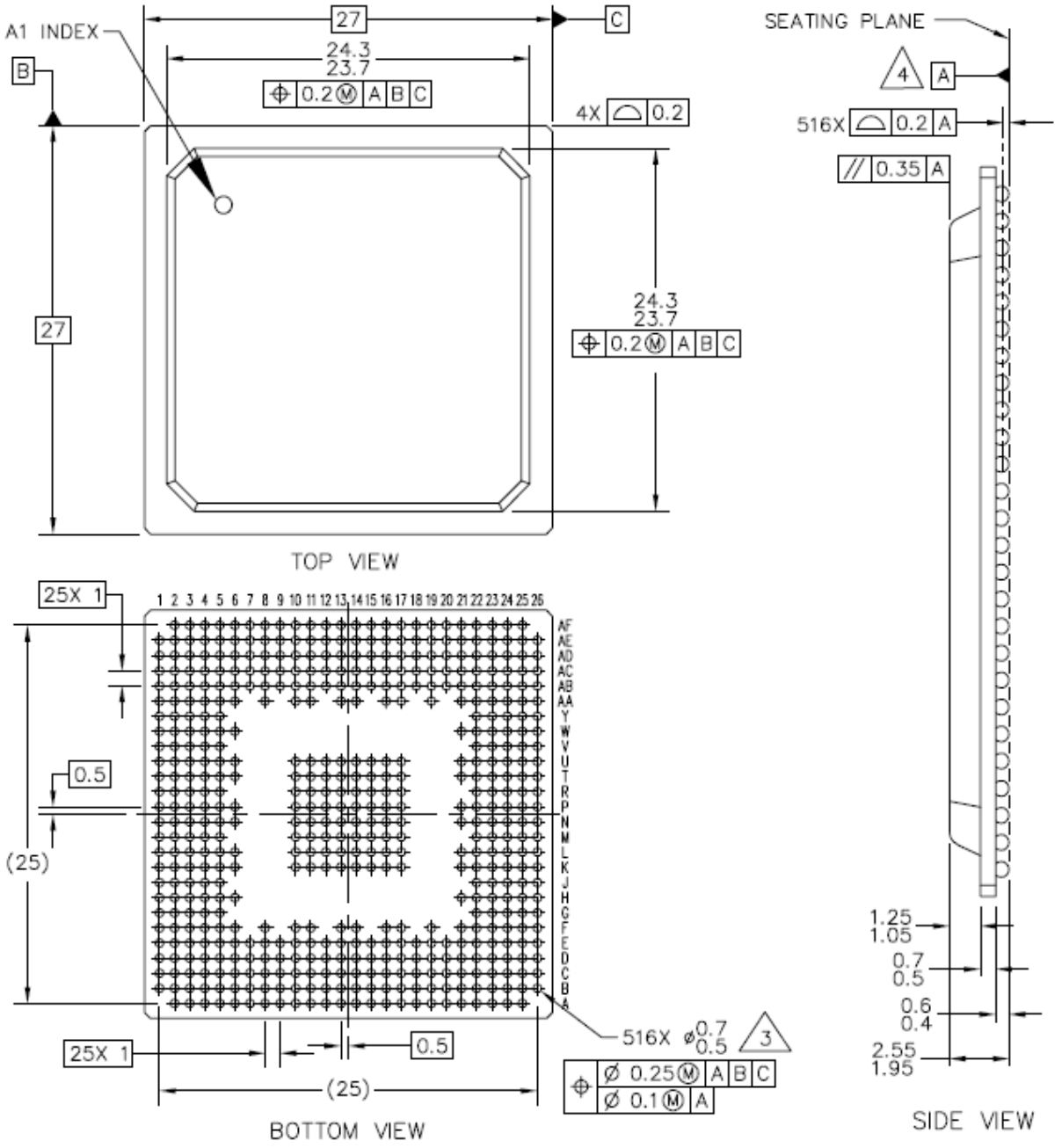

Figure 47. 516 TEPBGA Package (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES: 5193 & 5198.

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ARS10503D	REV: B
516 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1164A–01	09 AUG 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 48. 516 TEPBGA Package (2 of 2)

6 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.nxp.com.

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5674F Microprocessor Reference Manual* (document number MPC5674FRM).

Appendix A Signal Properties and Muxing

The following table shows the signals properties for each pin on the MPC5674F. For each port pin that has an associated SIU_PCR*n* register to control its pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: Primary function (P), Function 2 (F2), Function 3 (F3), and GPIO (G). See Figure 49.

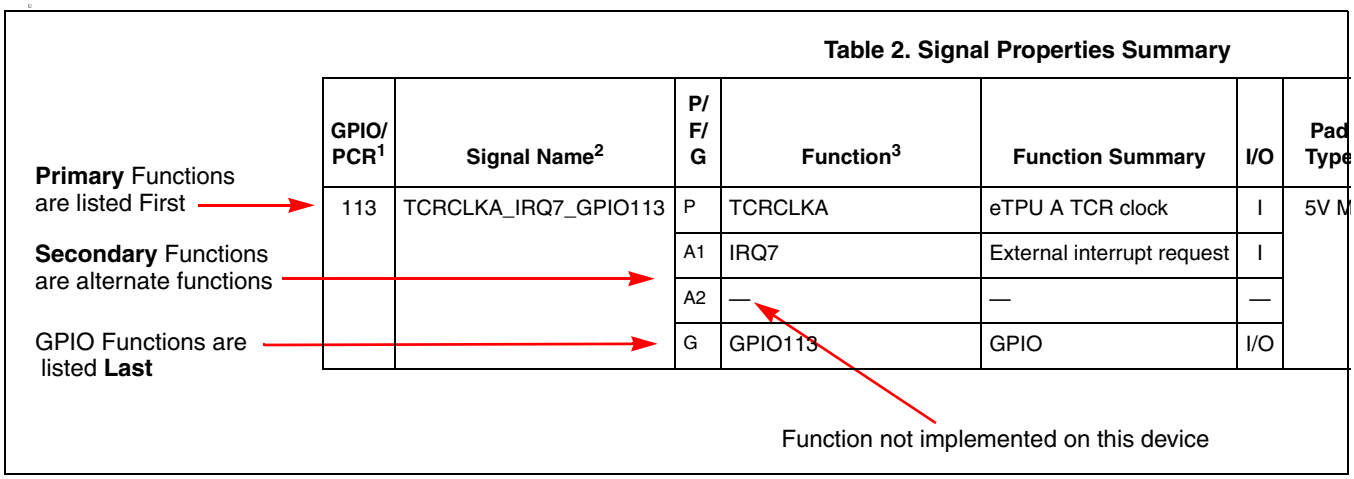

Figure 49. Supported Functions Example

Table 43. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
eTPU_A									
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	
		A1	IRQ7	External interrupt request	I				
		A2	—	—	—				
		G	GPIO113	GPIO	I/O				
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA12	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO114	GPIO	I/O				
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA13	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO115	GPIO	I/O				
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA14	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO116	GPIO	I/O				
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA15	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO117	GPIO	I/O				
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA16	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO118	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA17	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO119	GPIO	I/O				
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA18	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO120	GPIO	I/O				
121	ETPUA7_ETPUA19_ GPIO121	P	ETPUA7	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA19	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO121	GPIO	I/O				
122	ETPUA8_ETPUA20_ GPIO122	P	ETPUA8	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA20	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO122	GPIO	I/O				
123	ETPUA9_ETPUA21_ GPIO123	P	ETPUA9	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA21	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO123	GPIO	I/O				
124	ETPUA10_ETPUA22_ GPIO124	P	ETPUA10	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA22	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO124	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	ETPUA23	eTPU A channel (output only)	O				
		A2	—	—	—				
		G	GPIO125	GPIO	I/O				
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSB1	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO126	GPIO	I/O				
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSB3	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO127	GPIO	I/O				
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSB4	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO128	GPIO	I/O				
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSB5	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO129	GPIO	I/O				
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSD1	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO130	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSD2	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO131	GPIO	I/O				
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSD3	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO132	GPIO	I/O				
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSD4	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO133	GPIO	I/O				
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ8	External interrupt request	I				
		A2	—	—	—				
		G	GPIO134	GPIO	I/O				
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ9	External interrupt request	I				
		A2	—	—	—				
		G	GPIO135	GPIO	I/O				
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ10	External interrupt request	I				
		A2	—	—	—				
		G	GPIO136	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ11	External interrupt request	I				
		A2	—	—	—				
		G	GPIO137	GPIO	I/O				
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ12	External interrupt request	I				
		A2	—	—	—				
		G	GPIO138	GPIO	I/O				
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ13	External interrupt request	I				
		A2	—	—	—				
		G	GPIO139	GPIO	I/O				
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ14	External interrupt request	I				
		A2	—	—	—				
		G	GPIO140	GPIO	I/O				
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	IRQ15	External interrupt request	I				
		A2	—	—	—				
		G	GPIO141	GPIO	I/O				
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSC1	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO142	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
143	ETPUA29_PCSC2_ GPIO143	P	ETPUA29	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSC2	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO143	GPIO	I/O				
144	ETPUA30_PCSC3_ GPIO144	P	ETPUA30	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSC3	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO144	GPIO	I/O				
145	ETPUA31_PCSC4_ GPIO145	P	ETPUA31	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—
		A1	PCSC4	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO145	GPIO	I/O				
eTPU_B									
146	TCRCLKB_IRQ6_ GPIO146	P	TCRCLKB	eTPU B TCR clock	I	MH	V_{DDEH6}	—/Up	
		A1	IRQ6	External interrupt request	I				
		A2	—	—	—				
		G	GPIO146	GPIO	I/O				
147	ETPUB0_ETPUB16_ GPIO147	P	ETPUB0	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB16	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO147	GPIO	I/O				
148	ETPUB1_ETPUB17_ GPIO148	P	ETPUB1	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB17	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO148	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
149	ETPUB2_ETPUB18_ GPIO149	P	ETPUB2	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB18	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO149	GPIO	I/O				
150	ETPUB3_ETPUB19_ GPIO150	P	ETPUB3	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB19	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO150	GPIO	I/O				
151	ETPUB4_ETPUB20_ GPIO151	P	ETPUB4	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB20	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO151	GPIO	I/O				
152	ETPUB5_ETPUB21_ GPIO152	P	ETPUB5	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB21	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO152	GPIO	I/O				
153	ETPUB6_ETPUB22_ GPIO153	P	ETPUB6	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB22	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO153	GPIO	I/O				
154	ETPUB7_ETPUB23_ GPIO154	P	ETPUB7	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB23	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO154	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
155	ETPUB8_ETPUB24_ GPIO155	P	ETPUB8	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB24	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO155	GPIO	I/O				
156	ETPUB9_ETPUB25_ GPIO156	P	ETPUB9	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB25	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO156	GPIO	I/O				
157	ETPUB10_ETPUB26_ GPIO157	P	ETPUB10	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB26	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO157	GPIO	I/O				
158	ETPUB11_ETPUB27_ GPIO158	P	ETPUB11	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB27	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO158	GPIO	I/O				
159	ETPUB12_ETPUB28_ GPIO159	P	ETPUB12	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB28	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO159	GPIO	I/O				
160	ETPUB13_ETPUB29_ GPIO160	P	ETPUB13	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB29	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO160	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
161	ETPUB14_ETPUB30_ GPIO161	P	ETPUB14	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB30	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO161	GPIO	I/O				
162	ETPUB15_ETPUB31_ GPIO162	P	ETPUB15	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	ETPUB31	eTPU B channel (output only)	O				
		A2	—	—	—				
		G	GPIO162	GPIO	I/O				
163	ETPUB16_PCSA1_ GPIO163	P	ETPUB16	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	PCSA1	DSPI A peripheral chip select	O				
		A2	—	—	—				
		G	GPIO163	GPIO	I/O				
164	ETPUB17_PCSA2_ GPIO164	P	ETPUB17	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	PCSA2	DSPI A peripheral chip select	O				
		A2	—	—	—				
		G	GPIO164	GPIO	I/O				
165	ETPUB18_PCSA3_ GPIO165	P	ETPUB18	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	PCSA3	DSPI A peripheral chip select	O				
		A2	—	—	—				
		G	GPIO165	GPIO	I/O				
166	ETPUB19_PCSA4_ GPIO166	P	ETPUB19	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	PCSA4	DSPI A peripheral chip select	O				
		A2	—	—	—				
		G	GPIO166	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
167	ETPUB20_ GPIO167	P	ETPUB20	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO167	GPIO	I/O				
168	ETPUB21_ GPIO168	P	ETPUB21	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO168	GPIO	I/O				
169	ETPUB22_ GPIO169	P	ETPUB22	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO169	GPIO	I/O				
170	ETPUB23_ GPIO170	P	ETPUB23	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO170	GPIO	I/O				
171	ETPUB24_ GPIO171	P	ETPUB24	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO171	GPIO	I/O				
172	ETPUB25_ GPIO172	P	ETPUB25	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO172	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
173	ETPUB26_ GPIO173	P	ETPUB26	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO173	GPIO	I/O				
174	ETPUB27_ GPIO174	P	ETPUB27	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO174	GPIO	I/O				
175	ETPUB28_ GPIO175	P	ETPUB28	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO175	GPIO	I/O				
176	ETPUB29_ GPIO176	P	ETPUB29	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO176	GPIO	I/O				
177	ETPUB30_ GPIO177	P	ETPUB30	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO177	GPIO	I/O				
178	ETPUB31_ GPIO178	P	ETPUB31	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO178	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
GPIO, IRQ, FlexRay									
440	TCRCLKC_ GPIO440[9]	P	—	—	—	MH	V_{DDEH7}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO440	GPIO	I/O				
441	ETPUC0_ GPIO441[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO441	GPIO	I/O				
442	ETPUC1_ GPIO442[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO442	GPIO	I/O				
443	ETPUC2_ GPIO443[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO443	GPIO	I/O				
444	ETPUC3_ GPIO444[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO444	GPIO	I/O				
445	ETPUC4_ GPIO445[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO445	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
446	ETPUC5_ GPIO446[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO446	GPIO	I/O				
447	ETPUC6_ GPIO447[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO447	GPIO	I/O				
448	ETPUC7_ GPIO448[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO448	GPIO	I/O				
449	ETPUC8_ GPIO449[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO449	GPIO	I/O				
450	ETPUC9_IRQ0_ GPIO450[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	IRQ0	External interrupt request	I				
		A2	—	—	—				
		G	GPIO450	GPIO	I/O				
451	ETPUC10__IRQ1_ GPIO451[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	IRQ1	External interrupt request	I				
		A2	—	—	—				
		G	GPIO451	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	IRQ2	External interrupt request	I				
		A2	—	—	—				
		G	GPIO452	GPIO	I/O				
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	IRQ3	External interrupt request	I				
		A2	—	—	—				
		G	GPIO453	GPIO	I/O				
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	IRQ4	External interrupt request	I				
		A2	—	—	—				
		G	GPIO454	GPIO	I/O				
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	IRQ5	External interrupt request	I				
		A2	—	—	—				
		G	GPIO455	GPIO	I/O				
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO456	GPIO	I/O				
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	FR_A_TX	FlexRay A transfer	O				
		A2	—	—	—				
		G	GPIO457	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
458	ETPUC17_FR_A_RX_ GPIO458[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	FR_A_RX	FlexRay A receive	I				
		A2	—	—	—				
		G	GPIO458	GPIO	I/O				
459	ETPUC18_FR_A_TX_EN_ GPIO459[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	FR_A_TX_EN	FlexRay A transfer enable	O				
		A2	—	—	—				
		G	GPIO459	GPIO	I/O				
460	ETPUC19_TXDA_ GPIO460[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	TXDA	eSCI A transmit	O				
		A2	—	—	—				
		G	GPIO460	GPIO	I/O				
461	ETPUC20_RXDA _ GPIO461[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	RXDA	eSCI A receive	I				
		A2	—	—	—				
		G	GPIO461	GPIO	I/O				
462	ETPUC21_TXDB_ GPIO462[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	TXDB	eSCI B transmit	O				
		A2	—	—	—				
		G	GPIO462	GPIO	I/O				
463	ETPUC22_RXDB_ GPIO463[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	RXDB	eSCI B receive	I				
		A2	—	—	—				
		G	GPIO463	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
464	ETPUC23_PCSD5_ GPIO464[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	PCSD5	DSPI D peripheral chip select	O				
		A2	MAA0	ADC A Mux Address 0	O				
		A3	MAB0	ADC B Mux Address 0	O				
		G	GPIO464	GPIO	I/O				
465	ETPUC24_PCSD4_ GPIO465[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	PCSD4	DSPI D peripheral chip select	O				
		A2	MAA1	ADC A Mux Address 1	O				
		A4	MAB1	ADC B Mux Address 1	O				
		G	GPIO465	GPIO	I/O				
466	ETPUC25_PCSD3_ GPIO466[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	PCSD3	DSPI D peripheral chip select	O				
		A2	MAA2	ADC A Mux Address 2	O				
		A3	MAB2	ADC B Mux Address 2	O				
		G	GPIO466	GPIO	I/O				
467	ETPUC26_PCSD2_ GPIO467[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	PCSD2	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO467	GPIO	I/O				
468	ETPUC27_PCSD1_ GPIO468[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	PCSD1	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO468	GPIO	I/O				
469	ETPUC28_PCSD0_ GPIO469[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	PCSD0	DSPI D peripheral chip select	I/O				
		A2	—	—	—				
		G	GPIO469	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	SCKD	DSPI D clock	I/O				
		A2	—	—	—				
		G	GPIO470	GPIO	I/O				
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	SOUTD	DSPI D data output	O				
		A2	—	—	—				
		G	GPIO471	GPIO	I/O				
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG	—
		A1	SIND	DSPI D data input	I				
		A2	—	—	—				
		G	GPIO472	GPIO	I/O				
eMIOS									
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA0	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO179	GPIO	I/O				
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA1	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO180	GPIO	I/O				
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA2	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO181	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA3	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO182	GPIO	I/O				
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA4	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO183	GPIO	I/O				
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA5	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO184	GPIO	I/O				
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA6	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO185	GPIO	I/O				
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA7	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO186	GPIO	I/O				
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA8	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO187	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
188	EMIOS9_ETPUA9_ GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUA9	eTPU A channel	O				
		A2	—	—	—				
		G	GPIO188	GPIO	I/O				
189	EMIOS10_SCKD_ GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	SCKD	DSPI D clock	O				
		A2	—	—	—				
		G	GPIO189	GPIO	I/O				
190	EMIOS11_SIND_ GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	SIND	DSPI D data input	I				
		A2	—	—	—				
		G	GPIO190	GPIO	I/O				
191	EMIOS12_SOUTC_ GPIO191	P	EMIOS12	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	SOUTC	DSPI C data output	O				
		A2	—	—	—				
		G	GPIO191	GPIO	I/O				
192	EMIOS13_SOUTD_ GPIO192	P	EMIOS13	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	SOUTD	DSPI D data output	O				
		A2	—	—	—				
		G	GPIO192	GPIO	I/O				
193	EMIOS14_IRQ0_ GPIO193	P	EMIOS14	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	IRQ0	External interrupt request	I				
		A2	CNTXD	FlexCAN D transmit	O				
		G	GPIO193	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
194	EMIOS15_IRQ1_ GPIO194	P	EMIOS15	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	IRQ1	External interrupt request	I				
		A2	CNRXD	FlexCAN D receive	I				
		G	GPIO194	GPIO	I/O				
195	EMIOS16_ETPUB0_ GPIO195	P	EMIOS16	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB0	eTPU B channel	O				
		A2	FR_DBG[3]	FlexRay debug	O				
		G	GPIO195	GPIO	I/O				
196	EMIOS17_ETPUB1_ GPIO196	P	EMIOS17	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB1	eTPU B channel	O				
		A2	FR_DBG[2]	FlexRay debug	O				
		G	GPIO196	GPIO	I/O				
197	EMIOS18_ETPUB2_ GPIO197	P	EMIOS18	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB2	eTPU B channel	O				
		A2	FR_DBG[1]	FlexRay debug	O				
		G	GPIO197	GPIO	I/O				
198	EMIOS19_ETPUB3_ GPIO198	P	EMIOS19	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB3	eTPU B channel	O				
		A2	FR_DBG[0]	FlexRay debug	O				
		G	GPIO198	GPIO	I/O				
199	EMIOS20_ETPUB4_ GPIO199	P	EMIOS20	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB4	eTPU B channel	O				
		A2	—	—	—				
		G	GPIO199	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB5	eTPU B channel	O				
		A2	—	—	—				
		G	GPIO200	GPIO	I/O				
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB6	eTPU B channel	O				
		A2	—	—	—				
		G	GPIO201	GPIO	I/O				
202	EMIOS23_ETPUB7_ GPIO202	P	EMIOS23	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	ETPUB7	eTPU B channel	O				
		A2	—	—	—				
		G	GPIO202	GPIO	I/O				
203	EMIOS24_PCSB0_ GPIO203	P	EMIOS24	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSB0	DSPI B peripheral chip select	I/O				
		A2	—	—	—				
		G	GPIO203	GPIO	I/O				
204	EMIOS25_PCSB1_ GPIO204	P	EMIOS25	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSB1	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO204	GPIO	I/O				
432	EMIOS26_PCSB2_ GPIO432	P	EMIOS26	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSB2	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO432	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSB3	DSPI B peripheral chip select	O				
		A2	—	—	—				
		G	GPIO433	GPIO	I/O				
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSC0	DSPI C peripheral chip select	I/O				
		A2	—	—	—				
		G	GPIO434	GPIO	I/O				
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSC1	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO435	GPIO	I/O				
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSC2	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO436	GPIO	I/O				
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—
		A1	PCSC5	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO437	GPIO	I/O				
eQADC									
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0	
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1	
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2	

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
—	ANA3	P	ANA3[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA3	
—	ANA4	P	ANA4[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA4	
—	ANA5	P	ANA5[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA5	
—	ANA6	P	ANA6[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA6	
—	ANA7	P	ANA7[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA7	
—	ANA8	P	ANA8	eQADC A analog input	I	AE	V_{DDA_A1}	ANA8	
—	ANA9	P	ANA9	eQADC A analog input	I	AE	V_{DDA_A1}	ANA9	
—	ANA10	P	ANA10	eQADC A analog input	I	AE	V_{DDA_A1}	ANA10	
—	ANA11	P	ANA11	eQADC A analog input	I	AE	V_{DDA_A1}	ANA11	
—	ANA12	P	ANA12	eQADC A analog input	I	AE	V_{DDA_A1}	ANA12	
—	ANA13	P	ANA13	eQADC A analog input	I	AE	V_{DDA_A1}	ANA13	
—	ANA14	P	ANA14	eQADC A analog input	I	AE	V_{DDA_A1}	ANA14	
—	ANA15	P	ANA15	eQADC A analog input	I	AE	V_{DDA_A1}	ANA15	
—	ANA16	P	ANA16	eQADC A analog input	I	AE	V_{DDA_A1}	ANA16	
—	ANA17	P	ANA17	eQADC A analog input	I	AE	V_{DDA_A1}	ANA17	
—	ANA18	P	ANA18	eQADC A analog input	I	AE	V_{DDA_A1}	ANA18	
—	ANA19	P	ANA19	eQADC A analog input	I	AE	V_{DDA_A1}	ANA19	
—	ANA20	P	ANA20	eQADC A analog input	I	AE	V_{DDA_A1}	ANA20	
—	ANA21	P	ANA21	eQADC A analog input	I	AE	V_{DDA_A1}	ANA21	
—	ANA22	P	ANA22	eQADC A analog input	I	AE	V_{DDA_A1}	ANA22	
—	ANA23	P	ANA23	eQADC A analog input	I	AE	V_{DDA_A1}	ANA23	
—	AN24	P	AN24	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN24	
—	AN25	P	AN25	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN25	
—	AN26	P	AN26	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN26	

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN27	
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN28	
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN29	
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN30	
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN31	
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN32	
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN33	
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN34	
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN35	
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN36	
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN37	
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN38	
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN39	
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB0	
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB1	
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB2	
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB3	
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB4	
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB5	
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB6	
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB7	
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8	

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9	
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10	
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11	
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12	
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13	
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14	
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15	
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16	
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17	
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18	
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19	
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20	
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21	
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22	
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23	
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A	
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A	
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B	
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B	
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB	R
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA	R
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0	V
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1	V
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1	RE
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1	V
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0	V
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1	V

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
—	VSSA_B0	P	VSSA_B	Ground	I	VSSE	V_{SSA_B0}	VSSA_B0	V
—	REFBYPCB1	P	REFBYPCB1	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB1	RE
FlexRay									
248	FR_A_TX_ GPIO248	P	FR_A_TX	FlexRay A transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	(–/– th
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO248	GPIO	I/O				
249	FR_A_RX_ GPIO249	P	FR_A_RX	FlexRay A receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	(–/– th
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO249	GPIO	I/O				
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	(–/– th
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO250	GPIO	I/O				
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	(–/– th
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO251	GPIO	I/O				
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	(–/– th
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO252	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	(–/– th
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO253	GPIO	I/O				
FlexCAN									
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V_{DDEH4}	—/Up	
		A1	TXDA	eSCI A transmit	O				
		A2	—	—	—				
		G	GPIO83	GPIO	I/O				
84	CNRXA_RXDA_ GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V_{DDEH4}	—/Up	
		A1	RXDA	eSCI A receive	I				
		A2	—	—	—				
		G	GPIO84	GPIO	I/O				
85	CNTXB_PCSC3_ GPIO85	P	CNTXB	FlexCAN B transmit	O	MH	V_{DDEH4}	—/Up	
		A1	PCSC3	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO85	GPIO	I/O				
86	CNRXB_PCSC4_ GPIO86	P	CNRXB	FlexCAN B receive	I	MH	V_{DDEH4}	—/Up	
		A1	PCSC4	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO86	GPIO	I/O				
87	CNTXC_PCSD3_ GPIO87	P	CNTXC	FlexCAN C transmit	O	MH	V_{DDEH4}	—/Up	
		A1	PCSD3	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO87	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
88	CNRXC_PCSD4_ GPIO88	P	CNRXC	FlexCAN C receive	I	MH	V_{DDEH4}	—/Up	
		A1	PCSD4	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO88	GPIO	I/O				
246	CNTXD_ GPIO246	P	CNTXD	FlexCAN D transmit	O	MH	V_{DDEH4}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO246	GPIO	I/O				
247	CNRXD_ GPIO247	P	CNRXD	FlexCAN D receive	I	MH	V_{DDEH4}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO247	GPIO	I/O				
eSCI									
89	TXDA_ GPIO89	P	TXDA	eSCI A transmit	O	MH	V_{DDEH1}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO89	GPIO	I/O				
90	RXDA _ GPIO90	P	RXDA	eSCI A receive	I	MH	V_{DDEH1}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO90	GPIO	I				
91	TXDB_PCSD1_ GPIO91	P	TXDB	eSCI B transmit	O	MH	V_{DDEH1}	—/Up	
		A1	PCSD1	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO91	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V_{DDEH1}	—/Up	
		A1	PCSD5	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO92	GPIO	I/O				
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V_{DDEH4}	—/Up	
		A1	ETRIG0	eQADC trigger input	I				
		A2	—	—	—				
		G	GPIO244	GPIO	I/O				
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V_{DDEH5}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO245	GPIO	I/O				
DSPI									
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V_{DDEH3}	—/Up	
		A1	PCSC1	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO93	GPIO	I/O				
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V_{DDEH3}	—/Up	
		A1	PCSC2	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO94	GPIO	I/O				
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V_{DDEH3}	—/Up	
		A1	PCSC5	DSPI C peripheral chip select	O				
		A2	—	—	—				
		G	GPIO95	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
96	PCSA0_PCSD2_ GPIO96	P	PCSA0	DSPI A peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	
		A1	PCSD2	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO96	GPIO	I/O				
97	PCSA1_ GPIO97	P	PCSA1	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO97	GPIO	I/O				
98	PCSA2_ GPIO98	P	PCSA2	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO98	GPIO	I/O				
99	PCSA3_ GPIO99	P	PCSA3	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO99	GPIO	I/O				
100	PCSA4_ GPIO100	P	PCSA4	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO100	GPIO	I/O				
101	PCSA5_ETRIG1_ GPIO101	P	PCSA5	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	ETRIG1	eQADC trigger input	I				
		A2	—	—	—				
		G	GPIO101	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
102	SCKB_ GPIO102	P	SCKB	DSPI B clock	I/O	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO102	GPIO	I/O				
103	SINB_ GPIO103	P	SINB	DSPI B data input	I	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO103	GPIO	I/O				
104	SOUTB_ GPIO104	P	SOUTB	DSPI B data output	O	MH	V_{DDEH3}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO104	GPIO	I/O				
105	PCSB0_PCSD2_ GPIO105	P	PCSB0	DSPI B peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	
		A1	PCSD2	DSPI D peripheral chip select	O				
		A2	—	—	—				
		G	GPIO105	GPIO	I/O				
106	PCSB1_PCSD0_ GPIO106	P	PCSB1	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	PCSD0	DSPI D peripheral chip select	I/O				
		A2	—	—	—				
		G	GPIO106	GPIO	I/O				
107	PCSB2_SOUTC_ GPIO107	P	PCSB2	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	SOUTC	DSPI C data output	O				
		A2	—	—	—				
		G	GPIO107	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
108	PCSB3_SINC_ GPIO108	P	PCSB3	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	SINC	DSPI C data input	I				
		A2	—	—	—				
		G	GPIO108	GPIO	I/O				
109	PCSB4_SCKC_ GPIO109	P	PCSB4	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	SCKC	DSPI C clock	I/O				
		A2	—	—	—				
		G	GPIO109	GPIO	I/O				
110	PCSB5_PCSC0_ GPIO110	P	PCSB5	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	
		A1	PCSC0	DSPI C peripheral chip select	I/O				
		A2	—	—	—				
		G	GPIO110	GPIO	I/O				
235	SCKC_SCK_C_LVDSP_ GPIO235	P	SCKC	DSPI C clock	I/O	MH+ LVDS	V_{DDEH4}	—/Up	
		A1	SCK_C_LVDSP	LVDS+ downstream signal positive output clock	O				
		A2	—	—	—				
		G	GPIO235	GPIO	I/O				
236	SINC_SCK_C_LVDSM_ GPIO236	P	SINC	DSPI C data input	I	MH+ LVDS	V_{DDEH4}	—/Up	
		A1	SCK_C_LVDSM	LVDS– downstream signal negative output clock	O				
		A2	—	—	—				
		G	GPIO236	GPIO	I/O				
237	SOUTC_SOUT_C_LVDSP_ GPIO237	P	SOUTC	DSPI C data output	O	MH+ LVDS	V_{DDEH4}	—/Up	
		A1	SOUT_C_LVDSP	LVDS+ downstream signal positive output data	O				
		A2	—	—	—				
		G	GPIO237	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
238	PCSC0_SOUT_C_LVDSM_ GPIO238	P	PCSC0	DSPI C peripheral chip select	I/O	MH+ LVDS	V_{DDEH4}	—/Up	
		A1	SOUT_C_LVDSM	LVDS– downstream signal negative output data	O				
		A2	—	—	—				
		G	GPIO238	GPIO	I/O				
239	PCSC1_ GPIO239	P	PCSC1	DSPI C peripheral chip select	O	MH	V_{DDEH4}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO239	GPIO	I/O				
240	PCSC2_GPIO240	P	PCSC2	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO240	GPIO	I/O				
241	PCSC3_GPIO241	P	PCSC3	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO241	GPIO	I/O				
242	PCSC4_GPIO242	P	PCSC4	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO242	GPIO	I/O				
243	PCSC5_GPIO243	P	PCSC5	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO243	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
EBI									
256	D_CS0_ GPIO256	P	D_CS0	EBI chip select 0	O	F	V_{DDE9}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO256	GPIO	I/O				
257	D_CS2_D_ADD_DAT31_ GPIO257	P	D_CS2	EBI chip select 2	O	F	V_{DDE8}	—/Up	
		A1	D_ADD_DAT31	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO257	GPIO	I/O				
258	D_CS3_D_TEA_ GPIO258	P	D_CS3	EBI chip select 3	O	F	V_{DDE8}	—/Up	
		A1	D_TEA	EBI transfer error acknowledge	I				
		A2	—	—	—				
		G	GPIO258	GPIO	I/O				
259	D_ADD12_ GPIO259	P	D_ADD12	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO259	GPIO	I/O				
260	D_ADD13_ GPIO260	P	D_ADD13	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO260	GPIO	I/O				
261	D_ADD14_ GPIO261	P	D_ADD14	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO261	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
262	D_ADD15_ GPIO262	P	D_ADD15	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO262	GPIO	I/O				
263	D_ADD16_D_ADD_DAT16_ GPIO263	P	D_ADD16	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	D_ADD_DAT16	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO263	GPIO	I/O				
264	D_ADD17_D_ADD_DAT17_ GPIO264	P	D_ADD17	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	D_ADD_DAT17	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO264	GPIO	I/O				
265	D_ADD18_D_ADD_DAT18_ GPIO265	P	D_ADD18	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	D_ADD_DAT18	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO265	GPIO	I/O				
266	D_ADD19_D_ADD_DAT19_ GPIO266	P	D_ADD19	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	D_ADD_DAT19	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO266	GPIO	I/O				
267	D_ADD20_D_ADD_DAT20_ GPIO267	P	D_ADD20	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	D_ADD_DAT20	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO267	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
268	D_ADD21_D_ADD_DAT21_ GPIO268	P	D_ADD21	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT21	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO268	GPIO	I/O				
269	D_ADD22_D_ADD_DAT22_ GPIO269	P	D_ADD22	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT22	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO269	GPIO	I/O				
270	D_ADD23_D_ADD_DAT23_ GPIO270	P	D_ADD23	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT23	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO270	GPIO	I/O				
271	D_ADD24_D_ADD_DAT24_ GPIO271	P	D_ADD24	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT24	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO271	GPIO	I/O				
272	D_ADD25_D_ADD_DAT25_ GPIO272	P	D_ADD25	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT25	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO272	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
273	D_ADD26_D_ADD_DAT26_ GPIO273	P	D_ADD26	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT26	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO273	GPIO	I/O				
274	D_ADD27_D_ADD_DAT27_ GPIO274	P	D_ADD27	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT27	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO274	GPIO	I/O				
275	D_ADD28_D_ADD_DAT28_ GPIO275	P	D_ADD28	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT28	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO275	GPIO	I/O				
276	D_ADD29_D_ADD_DAT29_ GPIO276	P	D_ADD29	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT29	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO276	GPIO	I/O				
277	D_ADD30_D_ADD_DAT30_ GPIO277	P	D_ADD30	EBI address bus	I/O	F	V_{DDE9}	—/Up	
		A1	D_ADD_DAT30	EBI data only in non-mux mode. Address and data in mux mode.	I/O				
		A2	—	—	—				
		G	GPIO277	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO278	GPIO	I/O				
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO279	GPIO	I/O				
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO280	GPIO	I/O				
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO281	GPIO	I/O				
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO282	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO283	GPIO	I/O				
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO284	GPIO	I/O				
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO285	GPIO	I/O				
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO286	GPIO	I/O				
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO287	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO288	GPIO	I/O				
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO289	GPIO	I/O				
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO290	GPIO	I/O				
291	D_ADD_DAT13 _GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO291	GPIO	I/O				
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO292	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
293	D_ADD_DAT15_GPIO293	P	D_ADD_DAT15	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO293	GPIO	I/O				
294	D_RD_WR_GPIO294	P	D_RD_WR	EBI read/write	O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO294	GPIO	I/O				
295	D_WE0_GPIO295	P	D_WE0	EBI write enable	O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO295	GPIO	I/O				
296	D_WE1_GPIO296	P	D_WE1	EBI write enable	O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO296	GPIO	I/O				
297	D_OE_GPIO297	P	D_OE	EBI output enable	O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO297	GPIO	I/O				
298	D_TS_GPIO298	P	D_TS	EBI transfer start	O	F	V_{DDE9}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO298	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
299	D_ALE_GPIO299	P	D_ALE	EBI Address Latch Enable	O	F	V_{DDE10}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO299	GPIO	I/O				
300	D_TA_GPIO300	P	D_TA	EBI transfer acknowledge	I/O	F	V_{DDE9}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO300	GPIO	I/O				
301	D_CS1_GPIO301	P	D_CS1	EBI chip select	O	F	V_{DDE9}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO301	GPIO	I/O				
302	D_BDIP_GPIO302	P	D_BDIP	EBI burst data in progress	O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO302	GPIO	I/O				
303	D_WE2_GPIO303	P	D_WE2	EBI write enable	O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO303	GPIO	I/O				
304	D_WE3_GPIO304	P	D_WE3	EBI write enable	O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO304	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
305	D_ADD9_GPIO305	P	D_ADD9	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO305	GPIO	I/O				
306	D_ADD10_GPIO306	P	D_ADD10	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO306	GPIO	I/O				
307	D_ADD11_GPIO307	P	D_ADD11	EBI address bus	I/O	F	V_{DDE8}	—/Up	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO307	GPIO	I/O				
Reset and Clocks									
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up	F
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low	F
211	BOOTCFG0_IRQ2_ GPIO211	P	BOOTCFG0	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	B
		A1	IRQ2		I				
		A2	—	—	—				
		G	GPIO211	GPIO	I/O				
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	In
		A1	IRQ3	External interrupt request	I				
		A2	—	—	—				
		G	GPIO212	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
213	WKPCFG_NMI_ GPIO213	P	WKPCFG	Weak pull configuration input	I	MH	V_{DDEH1}	WKPCFG/Up	
		A1	NMI	Critical interrupt to core[11]	I				
		A2	—	—	—				
		G	GPIO213	GPIO	I				
208	PLLCFG0_IRQ4_ GPIO208	P	PLLCFG0	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up	
		A1	IRQ4	External interrupt request	I				
		A2	—	—	—				
		G	GPIO208	GPIO	I/O				
209	PLLCFG1_IRQ5_ GPIO209	P	PLLCFG1	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up	(for dev
		A1	IRQ5	External interrupt request	I				
		A2	SOUTD	DSPI D data output	O				
		G	GPIO209	GPIO	I/O				
—	PLLCFG2	P	PLLCFG2	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/ Down	
—	XTAL	P	XTAL	Crystal oscillator output	O	AE	V_{DD33}	XTAL	
—	EXTAL	P	EXTAL	Crystal oscillator input	I	AE	V_{DD33}	EXTAL	
229	D_CLKOUT	P	D_CLKOUT	EBI system clock output	O	F	V_{DDE9}	CLKOUT/ Enabled	
214	ENGCLK	P	ENGCLK	EBI engineering clock output Note: EXTCLK (External clock input) selected through SIU register)	O	F	V_{DDE2}	ENGCLK/ Enabled	
JTAG and Nexus (see footnote[12] about resets)									
—	$\overline{\text{EVTI}}$	–[13]	EVTI	Nexus event in	I	F	V_{DDE2}	—/Up	
227	$\overline{\text{EVTO}}$ (the BAM uses this pin to select if auto baud rate is on or off)	–[13]	EVTO	Nexus event out	O	F	V_{DDE2}	ABS/Up	
219	MCKO	–[13]	MCKO	Nexus message clock out	O	F	V_{DDE2}	O/Low	

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
220	MDO0_GPIO220 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO0[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	M
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO220	GPIO	I/O				
221	MDO1_GPIO221 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO1[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO221	GPIO	I/O				
222	MDO2_GPIO222 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO2[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO222	GPIO	I/O				
223	MDO3_GPIO223 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO3[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO223	GPIO	I/O				
75	MDO4_GPIO75 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO4[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO75	GPIO	I/O				
76	MDO5_GPIO76 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO5[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO76	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
77	MDO6_GPIO77 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO6[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO77	GPIO	I/O				
78	MDO7_GPIO78 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO7[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO78	GPIO	I/O				
79	MDO8_GPIO79 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO8[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO79	GPIO	I/O				
80	MDO9_GPIO80 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO9[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO80	GPIO	I/O				
81	MDO10_GPIO81 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO10[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO81	GPIO	I/O				
82	MDO11_GPIO82 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO11[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO82	GPIO	I/O				

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
231	MDO12_GPIO231	–[13]	MDO12[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO231	GPIO	I/O				
232	MDO13_GPIO232	–[13]	MDO13[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO232	GPIO	I/O				
233	MDO14_GPIO233	–[13]	MDO14[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO233	GPIO	I/O				
234	MDO15_GPIO234	–[13]	MDO15[15]	Nexus message data out	O	F	V_{DDE2}	O/Low	
		A1	—	—	—				
		A2	—	—	—				
		G	GPIO234	GPIO	I/O				
224	$\overline{\text{MSEO0}}$	–[13]	MSEO0[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	I
225	$\overline{\text{MSEO1}}$	–[13]	MSEO1[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	I
226	RDY	–[13]	RDY	Nexus ready output	O	F	V_{DDE2}	O/Low	
—	TCK	–[13]	TCK	JTAG test clock input	I	F	V_{DDE2}	TCK/Down	T
—	TDI	–[13]	TDI	JTAG test data input	I	F	V_{DDE2}	TDI/Up	
228	TDO	–[13]	TDO	JTAG test data output	O	F	V_{DDE2}	TDO/Up	
—	TMS	–[13]	TMS	JTAG test mode select input	I	F	V_{DDE2}	TMS/Up	
—	JCOMP	–[13]	JCOMP	JTAG TAP controller enable	I	F	V_{DDE2}	JCOMP/Down	JC
—	TEST	—	TEST	Test mode select (not for customer use)	I	F	V_{DDEH1}	TEST/Down	TI
—	VDDSYN	—	VDDSYN	Clock synthesizer power input	I	VDDE	V_{DDSYN}	VDDSYN	V

Table 43. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	aft
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN	
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY	
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL	
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL	
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL	
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG	

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is n indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO . This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alterna

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, c designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, A Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input a off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

9 This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that have

10 During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resisto clock propagates through the device.

11 NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.

[12] Nexus reset is different than system reset; MDO 1-11 are enabled when trace (RPM or FPM) is enabled, and MDO 12-15 when FPM tra
are also dependent on trace (RPM or FPM) being enabled.

[13] The Nexus pins don't have a "primary" function as they are not configured by the SIU. The pins are selected by asserting JCOMP and
have no effect on the function of these pins once enabled.

[14] MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC_PCR register).

[15] Do not connect pin directly to a power supply or ground.

Table 45 lists the pin locations of the power and ground signals on the 324 TEPBGA package.

Table 44. 324-pin Power Supply Locations

VDD

A2	B3	C4	D5	K3	V19	W5	W9	W20	Y4	Y21	AA3	AA22	AB2

VDD33

W21	V4

VDDE2

AB4	M9	N1	N10	N9	P10	P9	T4	W6	V2

VDDEH1

B1	L4

VDDEH4

AB20	W8

VDDEH6

N20	T21

VDDEH7

C22	H19	L22

VSS

A1	A22	AA2	AA21	AB1	AB22	B2	B21	C20	C3	D19	D4	J10	J11	J12	J13
K10	K11	K12	K13	K14	K9	L10	L11	L12	L13	L14	L9	M10	M11	M12	M13
N12	N13	N14	P11	P12	P13	P14	W19	W4	Y20	Y3					

Table 45 lists the pin locations of the power and ground signals on the 416 TEPBGA package.

Table 45. 416-pin Power Supply Locations

VDD

A2	B3	C4	D5	N4	AB4	AB23	AC3	AC12	AC24	AD2	AD25	AE1	AE26

VDD33

M1	AA4	AA23

VDDE2

N10	P10	P11	R10	R11	T1	T10	T11	T12	U10	U11	U12	W4	AC1	AC5	AF

VDDEH1

B1	P4

VDDEH3

AC10	AF5

VDDEH4

AC11	AF22

VDDEH5

AC21	AF25

VDDEH6

N23	AC25

VDDEH7

D24	E23	M26

VSS

A1	A26	B2	B25	C3	C24	D4	D23	K10	K11	K12	K13	K14	K15	K16	K17
L12	L13	L14	L15	L16	L17	M10	M11	M12	M13	M14	M15	M16	M17	N11	N12
N15	N16	N17	P12	P13	P14	P15	P16	P17	R12	R13	R14	R15	R16	R17	T13
T16	T17	U13	U14	U15	U16	U17	AC4	AC23	AD3	AD24	AE2	AE25	AF1	AF26	

Table 46 lists the pin locations of the power and ground signals on the 516 TEPBGA package.

Table 46. 516-pin Power Supply Locations

VDD

A2	B3	C4	D5	E6	N4	AB4	AB23	AC3	AC12	AC24	AD2	AD25	AE1	AE26

VDD33

M1	P6	L21	AA4	AA11	AA14	AA23

VDDE10

F16	F17	F19	F21	N21	P21	AA22

VDDE2

N10	P10	P11	R10	R11	T1	T10	T11	T12	U10	U11	U12	W4	AC1	AC5	AF2

VDDE8

F6	F8	F10	F11	N6	AA5

VDDE9

AA13	AB6	AB7	AB18	AB19	AB20	AB21

VDDEH1

B1	P4

VDDEH3

AC10	AF5

VDDEH4

AC11	AF22

VDDEH5

AC21	AF25

VDDEH6

N23	AC25

VDDEH7

D24	E23	M26

VSS

A25	B2	B25	B26	C3	C24	D4	D23	E5	E7	E8	E9	E10	E11	E12	E13
E16	E17	E18	E19	E21	E22	F5	F13	F14	K10	K11	K12	K13	K14	K15	K16
L11	L12	L13	L14	L15	L16	L17	M10	M11	M12	M13	M14	M15	M16	M17	N11
N14	N15	N16	N17	P12	P13	P14	P15	P16	P17	R12	R13	R14	R15	R16	R17
T15	T16	T17	U13	U14	U15	U16	U17	AA6	AA21	AB5	AB22	AC4	AC23	AD3	AD24

Appendix B Revision History

Table 47 describes the changes made to this document between revisions.

Table 47. Revision History

Revision (Date)	Description of changes
2 (Sept 2008)	Initial release, NDA Required.
3 (Nov 2009)	**Changes between Rev.2 and Rev. 3:**
	Added 516-pin package figures.
	Signals table: Updates throughout entire table.
	Updated Section 4.6, “Power Up/Down Sequencing”
	Updated features list. Updated flash PFCPR1 settings table. Fixed JTAG Test Clock Input Timing figure so the spec #’s in table matched figure.
	Updated Orderable Part numbers table.
	Moved signals table to be an appendix.
	Added 324-pin package thermals. Updated part numbers in orderable parts table (missing F: MPC5674F).
	FMPLL Electrical Spec table: Spec #1 changed min values of 4 to 8 Removed last sentence of footnote 2 Added note "Upper tolerance of less than 1% is allowed on 40MHz crystal."
	Oscillator Electrical Spec table: Moved predivider op. frequency spec from this table to the FMPLL Electrical Spec table Removed footnote #3 (since VDDE9 is an external supply and has no relation to the oscillator, PMC, or PLL).
	Added maximum solder temperature to Absolute Max Ratings table.
	PMC Operating Conditions table: Removed JTemp row. Changed VDDR to VDDREG (naming consistency) Changed VDD12 to VDD (naming consistency)
	PMC Electrical Spec table: Added VDDREG to this parameter “Trimmed bandgap reference voltage / voltage dependence (V_{DDREG})” Changed VDDSTEP to LVDSTEP12 (naming consistency)
	Added two conditons to the opening statements of Section 4.6, “Power Up/Down Sequencing.”
	DC Electrical Specifications table: spec #9 (Fast I/O Input High Voltage) spec #10 (Fast I/O Input Low Voltage) spec #24 (Operating Current 1.2 V Supplies; IDD) spec #25 (Operating Current 3.3 V Supplies; IDDSYN) spec #32 (Analog Input Current, Channel Off; IINACT_A) footnote #12 ("IOH_S = {11.6} mA...")

Table 47. Revision History (continued)

Revision (Date)	Description of changes
3 (cont.)	eQADC Conversion Specifications table: Spec #7, 8: both +/-3, no dependency on frequency Spec #15, 16: added "(with calibration)" to both
	Flash Program and Erase Specifications table: Added footnote 4 to spec #2. Updated all initial max value times.
	Updated entire AC Specifications: Clocking section.
	Pad AC Specifications table: updated Medium pad specs Derated Pad AC Specifications table: updated all specs
	Updated entire Section 4.6, “Power Up/Down Sequencing.”
	Updated Absolute Maximum Ratings (AMR) specs 1–11, 15, 16.
	Changed name of IDDC to IREGCTL since it is the REGCTL max drive current.
	Added two EMC Radiated Emissions Operating Behaviors tables and removed “EMI Testing Specifications” table.
	PMC Electrical Specifications table: 1b: Changed 1% to 2% 1c: Changed 150 to 300 ppm/C 2b: added footnote 2c: Changed from "Trimming step VDD" to "Trimming step VDD12OUT"
	DC Electrical Specifications table: 6: Updated min value and added keep-out range
	Standby RAM Regulator Electrical Specifications table: Added brownout spec
	PMC electrical spec table, added new specs: SMPS regulator output resistance, SPMS regulator clock frequency, SMPS regulator overshoot at start-up, SMPS max output current, and voltage variation on current step.
	Added LVD VDDA specs to the PMC electrical spec table.
	Removed specs for VDDF and VFLASH since those supplies are shorted with others in the package.
4 (Aug 2010)	**Changes between Rev.3 and Rev.4:**
	Table “Derated Pad AC Specifications”, Spec #1: Changed 20ns to 200ns.
	Added “324-ball TEPBGA Pin Assignments” section and mechanical drawings.
	Appendix A (Signals): Added “(the BAM uses this pin to select if auto baud rate is on or off)” to the EVTO pin description. Added 324 pinout column. Changed footnote from “NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU DIRER register.“ to “NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers.” Updated eQADC signals to show that eQADC A and B each have dedicated channels (ANx0-23) and shared channels (AN24-39).

Table 47. Revision History (continued)

Revision (Date)	Description of changes
4 (cont)	"Temperature Sensor Electrical Specifications" table: Changed spec #2 to have one temperature range (-40 - 150 C) and changed spec value from ±1.0 to ±10.0 C.
	"eQADC Conversion Specifications (Operating)" table: Changed spec #13 (non-disruptive injection current) values from ±1 to ±3.
	"IPCLKDIV Settings" table, removed footnote "eMIOS and DMA are not considered peripherals here."
5 (Feb-2011)	Note 4 in Maximum Ratings updated from 2.0 V to 1.65 V. Changed I/O Supply Voltage spec in DC Electrical specs, Spec 2, from 1.62 V min to 3.0 V min. Changed the APC=RWSC value in line 1 of PFCPR1 Settings vs. Frequency of Operation table from 0b011 to 0b100 Changed note 1 for Pad AC Specifications table from Vdde = 1.62 V to 1.98 V to read Vdde = 3.0 V to 3.6 V Changed note 6 for Signal Properties and Muxing Summary table by removing the voltage range 1.8 V - 3.3 V to have 3.3 V instead of the range. Spec 2 in Table 9 "ESD Ratings" the spec for "ESD for Charged Device Model (CDM)" changed to 250 V (other) from 500 V (other) Removed voltage ranges 1.62-1.98 V and 2.25-2.75 V from spec 28 in Table 14
6 (Feb-2011)	Same content as for Rev. 5
7 (Mar-2011)	Added entry for Rev. 6 and Rev. 7 to this table to fix a revision-numbering issue.
8 (Jun-2011)	Added the following footnotes to the "Signal Properties and Muxing Summary" table: • Footnote 10, for the ANA[0:7] signals, "During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device." • Footnote 15, for MDO[0:15] and MSEO[0:1] signals, "Do not connect pin directly to a power supply or ground."
	Changed min and max values of ID 1 "Nominal bandgap reference voltage" in Table 11 (PMC Electrical Specifications) to 0.608 V min and 0.632 V max. Changed min and max values of Spec 2 "ADC Bandgap" in Table 23 (ADC Band Gap Reference/LVI Electrical Specifications) to 1.171 V min and 1.269 V max. Changed Spec 3 of Table 26 (Flash EEPROM Module Life) from 'Minimum Data Retention at 25 °C ambient temperature' to 'Minimum Data Retention at 85 °C ambient temperature'
	Added Spec 41, 42, 43 and 44 to the "DC Electrical Specifications" table Added Note 25 to the "DC Electrical Specifications" table for Spec 41, 42 and 43 Added Note 26 to the "DC Electrical Specifications" for Spec 44 Added Spec 17 to the "eQADC Conversion Specifications (Operating)" table. Added Spec 18 to the "eQADC Conversion Specifications (Operating)" table. Added Note 15 to the "eQADC Conversion Specifications (Operating)" table for Spec 17 and 18.

Table 47. Revision History (continued)

Revision (Date)	Description of changes
8 (Jun-2011)	Removed spec 3 from Table 27 “PFCPR1 Settings vs Frequency of Operation” Updated spec 2a (Untrimmed VRC 1.2V) in Table 11 “PMC Electrical Specifications“ to a max value of VDD12OUT + 17%. Updated item 26 (Operating Current VDDA Supply) in table 14 “Electrical Specifications” from 30 mA to 40 mA. Updated Note 11 for Table 14 (Electrical Specifications) to read IOH_F = {16,32,47,77} mA and IOL_F = {24,48,71,115} mA for {00,01,10,11} drive mode with VDDE = 3.0 V. Updated ID 9 in Table 11 (PMC Electrical Specifications) to V_{REG} = 4.5 V, max DC output current with a max of 80 mA V_{REG} = 4.25 V, max DC output current, crank condition with a max of 40 mA Updated Table 17 (DSPI LVDS Pad Specification) with the following: • Spec 1 typical value updated from 40 MHz to 50 MHz • Spec 2 added SRC conditions and associated values: – SRC=0b00 or SRC=0b11 Min 150 mV Max 400 mV – SRC=0b01 Min 90 mV Max 320 mV – SRC=0b10 Min 160 mV Max 480 mV • Spec 3 - Min value from 1.075 V to 1.06 V - Max value from 1.325 V to 1.39 V • Added Spec 5, 6 and 7
	Updated table 17 "DSPI LVDS pad specification" to include Temperature with a min value of -40 C and max of 150 C Updated Spec 5 of Table 18, "FMPLL Electrical Specifications" to < 400 us as the Max vaule. Added the sentence "Violating the VCO min/max range may prevent the system from exiting reset." to the end of Footnote 16 of Table 18, "FMPLL Electrical Specifications" Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", Crystal Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Updated Spec 1 of Table 18, "FMPLL Electrical Specifications", External Reference (PLLCFG2 = 0b1) minimum value from 40 MHz to 16 MHz. Removed Note 9, 'Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1', from Table 18, "FMPLL Electrical Specifications". Updated ID 16 in Table 11, “PMC Electrical Specifications”, SMPS regulator clock frequency (after reset) 2.4MHz Max
	Updated Table 16 “Flash EEPROM Module Life”, spec 3, ‘Blocks with 10,001–100,000 P/E cycles’ to 5 Years. Added Typ column to Table 25, “Flash Program and Erase Specifications”
	Updated Table 3, “Absolute Maximum Ratings” with the following: - Spec 1, ‘1.2 V Core Supply Voltage’, to a Max of 2.0 V - Spec 3, ‘Clock Synthesizer Voltage’, to a Max of 5.3 V - Spec 4, ‘I/O Supply Voltage’ to a Max of 5.3 V - Spec 5, ‘Analog Supply Voltage’ to a Max of 5.3 V - Note 2 to read, “2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining.“ - Note 3, “... 5.0 V + 10% ...” to “... 5.25 V + 10 % ...” - Note 5, “... 3.3 V + 10% ...” to “... 3.60 V + 10 % ...” Updated Spec 2 (ESD for Charged Device Model (CDM)) of Table 9, “ESD Ratings”, to 500 V Updated Table 27, “PFCPR1 Settings vs. Frequency of Operation“, Spec 3, APC = RWSC column to 0b100. Updated Spec 26, “Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz“ for I_{DDA} to 50 mA, in Table 14, “DC electrical specifications”.

Table 47. Revision History (continued)

Revision (Date)	Description of changes
9	Updated Table 1.,"Orderable Part Numbers" with actual available parts. Added new part number SPC5673FF3MVY2 ,Package description 516 PBGA, w/EBI, Pb-free.Speed is 200 MHz nom and max.—Removed note attached to “Orderable Part Numbers” and “Freescale Part Number”. Updated footnotes of Table 3.,"Absolute Maximum Ratings" to: • 2.0 V for 10 hours cumulative time, 1.2V +10% for time remaining. • 6.4 V for 10 hours cumulative time, 5.0V +10% for time remaining. • 5.3 V for 10 hours cumulative time, 3.3V +10% for time remaining. Updated Table 6.,"Thermal Characteristics, 324-pin Package" to show MPC5674F thermal characteristics. In Table 10.,"PMC Operating conditions", updated the parameter “Supply voltage VDD 1.2V nominal" to “Core supply voltage". In Table 11.,"PMC Electrical Specifications", updated the following rows: • Parameter “Nominal VRC regulated 1.2V output VDD” updated column “Typ” to 1.27 V. • The minimum and maximum value of “Untrimmed VRC 1.2V output variation before band gap trim (unloaded)” updated to “-14%” and “+10%”, respectively. • The minimum and maximum value of “Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max 1A)” updated to “-10%” and “+5%”, respectively. In Table 12.,"Power Sequence Pin States for MH and AE pads", updated the row (VDD33 = low, VDDE = high), parameter “MH+LVDS Pads” to “Outputs disabled”. In Table 13.,"Power Sequence Pin States for F and FS pads", updated the rows (VDD = low, VDD33 = low, VDDE = high) and (VDD = high, VDD33 = low, VDDE = high), parameter “F and FS pad” to “Outputs Disabled”. In Table 14.,"DC Electrical Specifications", updated the spec 'Operating Current 1.2 V Supplies @ f_{SYS} = 264 MHz' with 'V_{DD} @ 1.32 V' Max value to 850 mA from 1.0 A, and deleted corresponding footnote stating that the previous information was preliminary. Updated current (mA) values in Table 15.,"V_{DDE}/V_{DDEH} I/O Pad Average DC Current" from Spec 5 to 13: • Spec 5 Current (mA) from 6.5 to 7.4 • Spec 6 Current (mA) from 9.4 to 10.5 • Spec 7 Current (mA) from 10.8 to 12.3 • Spec 8 Current (mA) from 33.3 to 35.2 • Spec 9 Current (mA) from 12.0 to 12.7 • Spec 10 Current (mA) from 6.2 to 6.7 • Spec 11 Current (mA) from 4.0 to 4.2 • Spec 12 Current (mA) from 2.4 to 2.6 • Spec 13 Current (mA) from8.9 to 9. In Table 35.,"Nexus Debug Port Timing", updated the footnote of parameter “tCYC” to “See Notes on tcyc in Table27”. Removed references to “Section I/O Pad VDD33 Current Specifications” .
10	Updated Figure 1.,"MPC5674F Orderable Part Number Description" with changes in “Revision of Silicon” and “Fab Revision ID”. Updated Table 1.,"Orderable Part Numbers" with changes in Part numbers and Package Description.

Table 47. Revision History (continued)

Revision (Date)	Description of changes
10.1	In Figure 1.,"MPC5674F Orderable Part Number Description", replaced “Revision of Silicon for TSMC is 0 for now. In future, it will be revision 1” with “0 = Rev 0 (TSMC14)”.
11	In Figure 1.,"MPC5674F Orderable Part Number Description", updated Fab and Masking Information. In Table 1, added information about the available parts.

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