



**THE DATASHEET OF  
LMP7718MME/NOPB**



## 88 MHz, Precision, Low Noise, 1.8V CMOS Input, Decompensated Operational Amplifier

Check for Samples: [LMP7717](#), [LMP7718](#)

### FEATURES

- (Typical 5V Supply, Unless Otherwise Noted)
- Input Offset Voltage:  $\pm 150 \mu\text{V}$  (max)
- Input Referred Voltage Noise:  $5.8 \text{ nV}/\sqrt{\text{Hz}}$
- Input Bias Current: 100 fA
- Gain Bandwidth Product: 88 MHz
- Supply Voltage Range: 1.8V to 5.5V
- Supply Current Per Channel
  - LMP7717: 1.15 mA
  - LMP7718: 1.30 mA
- Rail-to-Rail Output Swing
  - @ 10 k $\Omega$  Load: 25 mV from Rail
  - @ 2 k $\Omega$  Load: 45 mV from Rail
- Ensured 2.5V and 5.0V Performance
- Total Harmonic Distortion: 0.04% @ 1 kHz, 600 $\Omega$
- Temperature Range:  $-40^\circ\text{C}$  to  $125^\circ\text{C}$

### APPLICATIONS

- ADC Interface
- Photodiode Amplifiers
- Active Filters and Buffers
- Low Noise Signal Processing
- Medical Instrumentation
- Sensor Interface Applications

### DESCRIPTION

The LMP7717 (single) and the LMP7718 (dual) low noise, CMOS input operational amplifiers offer a low input voltage noise density of  $5.8 \text{ nV}/\sqrt{\text{Hz}}$  while consuming only 1.15 mA (LMP7717) of quiescent current. The LMP7717/LMP7718 are stable at a gain of 10 and have a gain bandwidth (GBW) product of 88 MHz. The LMP7717/LMP7718 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMP7717/LMP7718 each feature a rail-to-rail output stage. Both amplifiers are part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

The LMP7717 family provides optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femto-Amperes, and an input common mode voltage range, which includes ground, make the LMP7717/LMP7718 ideal for low power sensor applications where high speeds are needed.

The LMP7717/LMP7718 are manufactured using TI's advanced VIP50 process. The LMP7717 is offered in either a 5-Pin SOT-23 or an 8-Pin SOIC package. The LMP7718 is offered in either the 8-Pin SOIC or the 8-Pin VSSOP.



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Typical Application

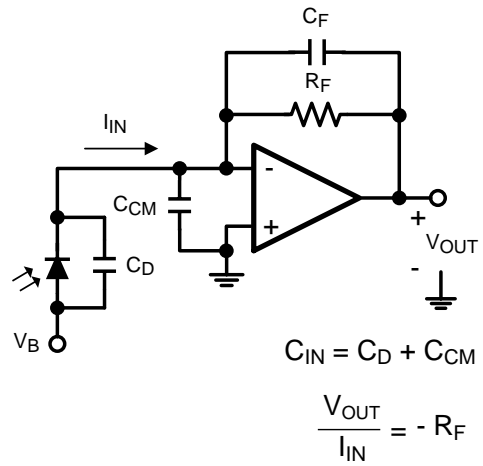


Figure 1. Photodiode Transimpedance Amplifier

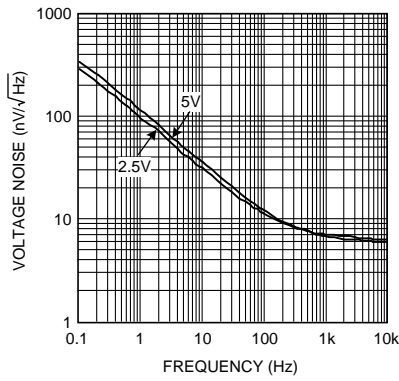


Figure 2. Input Referred Voltage Noise vs. Frequency



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	
Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
V <sub>IN</sub> Differential	±0.3V
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )	6.0V
Input/Output Pin Voltage	V <sup>+</sup> +0.3V, V <sup>-</sup> -0.3V
Storage Temperature Range	-65°C to 150°C
Junction Temperature <sup>(4)</sup>	+150°C
For soldering specifications: see product folder at <a href="http://www.ti.com/">www.ti.com/</a> and <a href="http://www.ti.com/lit/SNOA549">http://www.ti.com/lit/SNOA549</a>	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see [5V Electrical Characteristics](#)<sup>(1)</sup>.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

### Operating Ratings<sup>(1)</sup>

Temperature Range <sup>(2)</sup>	-40°C to 125°C
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> ) -40°C ≤ T <sub>A</sub> ≤ 125°C	2.0V to 5.5V
0°C ≤ T <sub>A</sub> ≤ 125°C	1.8V to 5.5V
Package Thermal Resistance (θ <sub>JA</sub> ) <sup>(2)</sup>	
5-Pin SOT-23	180°C/W
8-Pin SOIC	190°C/W
8-Pin VSSOP	236°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see [5V Electrical Characteristics](#)<sup>(1)</sup>.
- (2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

## 2.5V Electrical Characteristics<sup>(1)</sup>

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage			$\pm 20$	$\pm 180$ <b><math>\pm 480</math></b>	$\mu\text{V}$
$\text{TC } V_{\text{OS}}$	Input Offset Voltage Temperature Drift <sup>(4)</sup> <sup>(5)</sup>	LMP7717		-1.0	$\pm 4$	$\mu\text{V}/^\circ\text{C}$
		LMP7718		-1.8		
$I_{\text{B}}$	Input Bias Current	$V_{\text{CM}} = 1.0\text{V}$ See <sup>(6)</sup> and <sup>(5)</sup>	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.05	1 <b>25</b>	pA
			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	0.05	1 <b>100</b>	
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 1.0\text{V}$ See <sup>(5)</sup>		.006	0.5 <b>50</b>	pA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 1.4\text{V}$	83 <b>80</b>	94		dB
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85 <b>80</b>	100		dB
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	98		
CMVR	Common Mode Voltage Range	CMRR $\geq 60$ dB CMRR $\geq 55$ dB	-0.3 <b>-0.3</b>		1.5 <b>1.5</b>	V
$A_{\text{VOL}}$	Open Loop Voltage Gain	$V_{\text{OUT}} = 0.15\text{V}$ to $2.2\text{V}$ , $R_{\text{L}} = 2\text{ k}\Omega$ to $V^+/2$	LMP7717	88 <b>82</b>	98	dB
			LMP7718	84 <b>80</b>	92	
		$V_{\text{OUT}} = 0.15\text{V}$ to $2.2\text{V}$ , $R_{\text{L}} = 10\text{ k}\Omega$ to $V^+/2$	LMP7717	92 <b>88</b>	110	
			LMP7718	90 <b>86</b>	95	
$V_{\text{OUT}}$	Output Voltage Swing High	$R_{\text{L}} = 2\text{ k}\Omega$ to $V^+/2$		25	70 <b>77</b>	mV from either rail
		$R_{\text{L}} = 10\text{ k}\Omega$ to $V^+/2$		20	60 <b>66</b>	
	Output Voltage Swing Low	$R_{\text{L}} = 2\text{ k}\Omega$ to $V^+/2$		30	70 <b>73</b>	
		$R_{\text{L}} = 10\text{ k}\Omega$ to $V^+/2$		15	60 <b>62</b>	
$I_{\text{OUT}}$	Output Current	Sourcing to $V^-$ $V_{\text{IN}} = 200\text{ mV}$ See <sup>(7)</sup>	36 <b>30</b>	47		mA
		Sinking to $V^+$ $V_{\text{IN}} = -200\text{ mV}$ See <sup>(7)</sup>	7.5 <b>5</b>	15		
$I_{\text{S}}$	Supply Current per Amplifier	LMP7717		0.95	1.30 <b>1.65</b>	mA
		LMP7718 per channel		1.1	1.5 <b>1.85</b>	

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_{\text{J}} = T_{\text{A}}$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_{\text{J}} > T_{\text{A}}$ .
- (2) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (4) Offset voltage average drift is determined by dividing the change in  $V_{\text{OS}}$  by temperature change.
- (5) Parameter is specified by design and/or characterization and is not test in production.
- (6) Positive current corresponds to current flowing into the device.
- (7) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

## 2.5V Electrical Characteristics<sup>(1)</sup> (continued)

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
SR	Slew Rate	$A_V = +10$ , Rising (10% to 90%)		32		V/ $\mu\text{s}$
		$A_V = +10$ , Falling (90% to 10%)		24		
GBW	Gain Bandwidth	$A_V = +10$ , $R_L = 10\text{ k}\Omega$		88		MHz
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$		6.2		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 600\Omega$		0.01		%

## 5V Electrical Characteristics<sup>(1)</sup>

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units	
$V_{\text{OS}}$	Input Offset Voltage			$\pm 10$	$\pm 150$ <b><math>\pm 450</math></b>	$\mu\text{V}$	
$\text{TC } V_{\text{OS}}$	Input Offset Voltage Temperature Drift <sup>(4) (5)</sup>	LMP7717		-1.0	$\pm 4$	$\mu\text{V}/^\circ\text{C}$	
		LMP7718		-1.8			
$I_B$	Input Bias Current	$V_{\text{CM}} = 2.0\text{V}$ See <sup>(6)</sup> and <sup>(5)</sup>	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		0.1	1 <b>25</b>	$\text{pA}$
			$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1	1 <b>100</b>	
$I_{\text{OS}}$	Input Offset Current	$V_{\text{CM}} = 2.0\text{V}$ See <sup>(5)</sup>		.01	0.5 <b>50</b>	$\text{pA}$	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 3.7\text{V}$	85 <b>80</b>	100		$\text{dB}$	
PSRR	Power Supply Rejection Ratio	$2.0\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85 <b>80</b>	100		$\text{dB}$	
		$1.8\text{V} \leq V^+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	98			
CMVR	Common Mode Voltage Range	CMRR $\geq 60\text{ dB}$ CMRR $\geq 55\text{ dB}$	-0.3 <b>-0.3</b>		4 <b>4</b>	$\text{V}$	
$A_{\text{VOL}}$	Open Loop Voltage Gain	$V_{\text{OUT}} = 0.3\text{V}$ to $4.7\text{V}$ , $R_L = 2\text{ k}\Omega$ to $V^+/2$	LMP7717	88 <b>82</b>	107	$\text{dB}$	
			LMP7718	84 <b>80</b>	90		
		$V_{\text{OUT}} = 0.3\text{V}$ to $4.7\text{V}$ , $R_L = 10\text{ k}\Omega$ to $V^+/2$	LMP7717	92 <b>88</b>	110		
			LMP7718	90 <b>86</b>	95		
$V_{\text{OUT}}$	Output Voltage Swing High	$R_L = 2\text{ k}\Omega$ to $V^+/2$	LMP7717		35	70 <b>77</b>	$\text{mV}$ from either rail
			LMP7718		45	80 <b>83</b>	
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		25	60 <b>66</b>		
	Output Voltage Swing Low	$R_L = 2\text{ k}\Omega$ to $V^+/2$	LMP7717		42	70 <b>73</b>	
			LMP7718		45	80 <b>83</b>	
		$R_L = 10\text{ k}\Omega$ to $V^+/2$		25	60 <b>66</b>		
$I_{\text{OUT}}$	Output Short Circuit Current	Sourcing to $V^-$ $V_{\text{IN}} = 200\text{ mV}$ See <sup>(7)</sup>	46 <b>38</b>	60		$\text{mA}$	
		Sinking to $V^+$ $V_{\text{IN}} = -200\text{ mV}$ See <sup>(7)</sup>	10.5 <b>6.5</b>	21			

- Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .
- Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
- Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- Offset voltage average drift is determined by dividing the change in  $V_{\text{OS}}$  by temperature change.
- Parameter is specified by design and/or characterization and is not test in production.
- Positive current corresponds to current flowing into the device.
- The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

### 5V Electrical Characteristics<sup>(1)</sup> (continued)

Unless otherwise specified, all limits are ensured for  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2 = V_O$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$I_S$	Supply Current per Amplifier	LMP7717		1.15	1.40 <b>1.75</b>	mA
		LMP7718 per channel		1.30	1.70 <b>2.05</b>	
SR	Slew Rate	$A_V = +10$ , Rising (10% to 90%)		35		V/ $\mu\text{s}$
		$A_V = +10$ , Falling (90% to 10%)		28		
GBW	Gain Bandwidth	$A_V = +10$ , $R_L = 10\text{ k}\Omega$		88		MHz
$e_n$	Input Referred Voltage Noise Density	$f = 1\text{ kHz}$		5.8		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise Density	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{ kHz}$ , $A_V = 1$ , $R_L = 600\Omega$		0.01		%

### CONNECTION DIAGRAMS

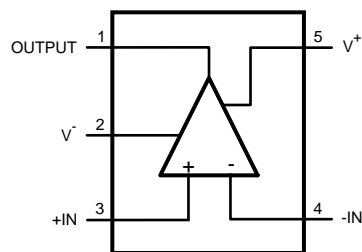


Figure 3. 5-Pin SOT-23 (LMP7717)  
Top View

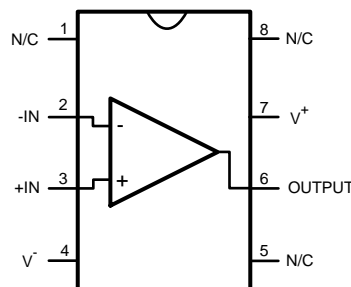


Figure 4. 8-Pin SOIC (LMP7717)  
Top View

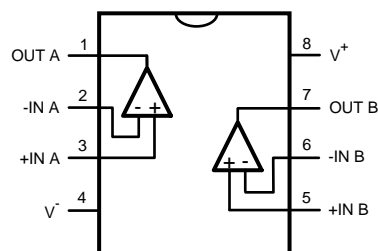


Figure 5. 8-Pin SOIC/VSSOP (LMP7718)

### TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

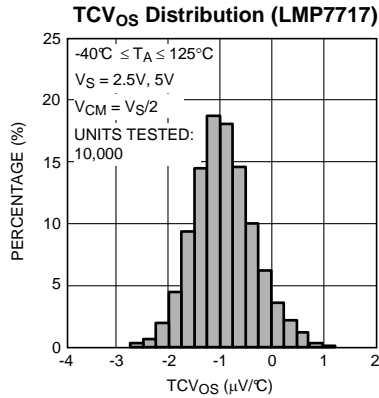


Figure 6.

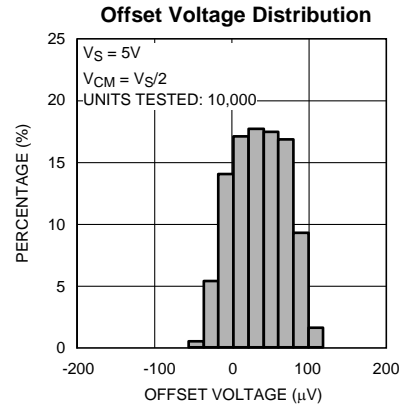


Figure 7.

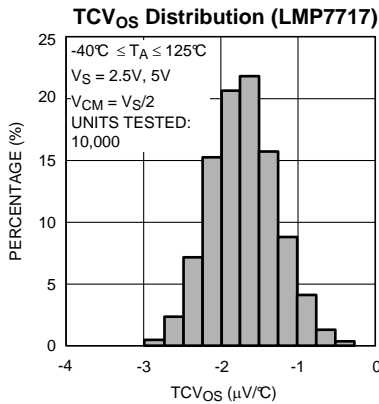


Figure 8.

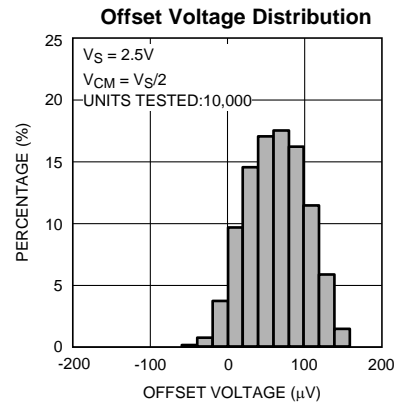


Figure 9.

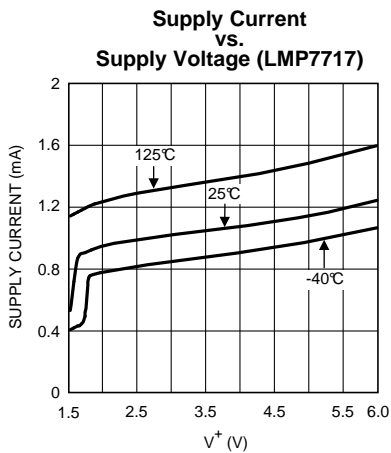


Figure 10.

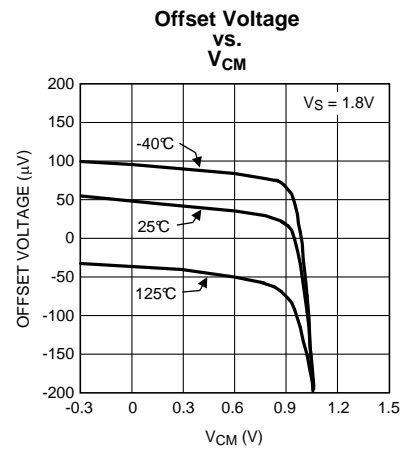


Figure 11.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

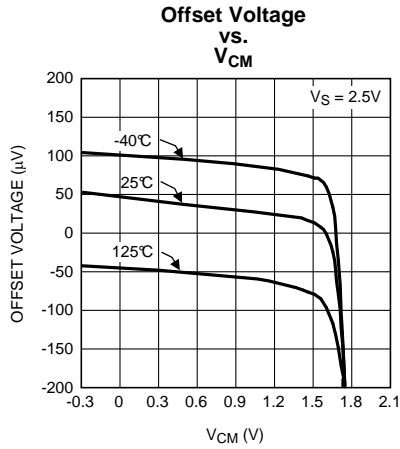


Figure 12.

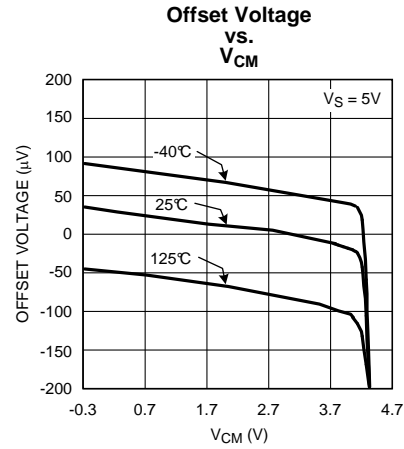


Figure 13.

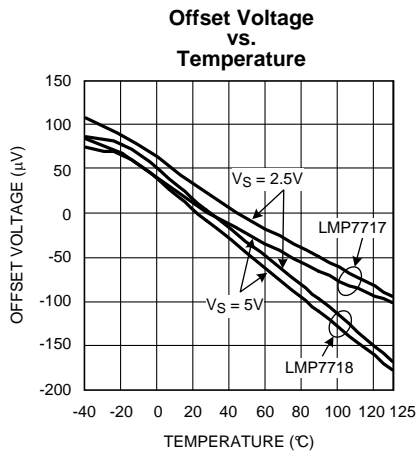


Figure 14.

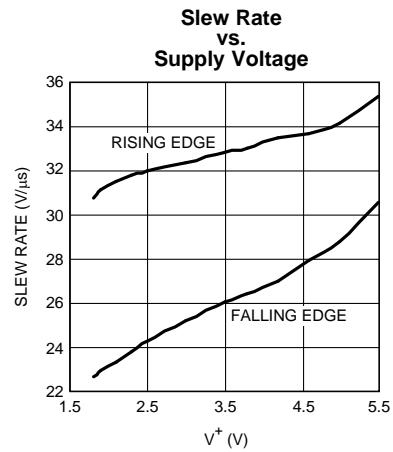


Figure 15.

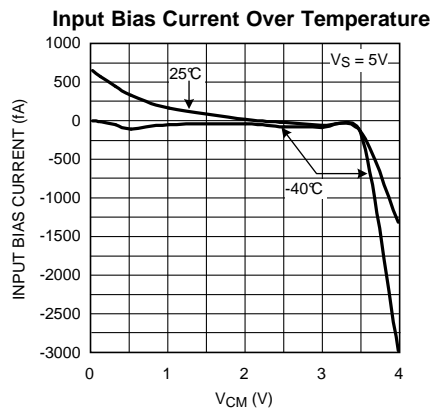


Figure 16.

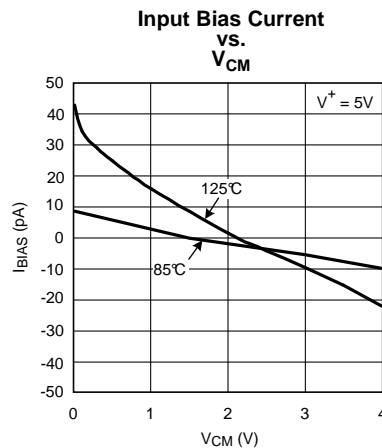


Figure 17.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

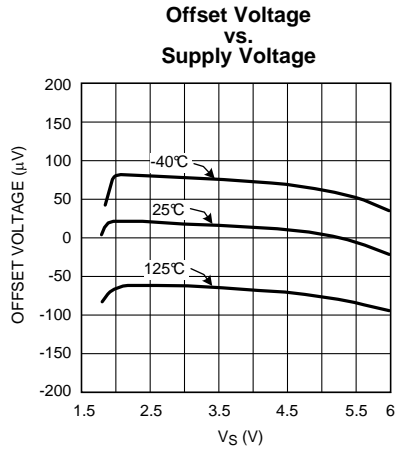


Figure 18.

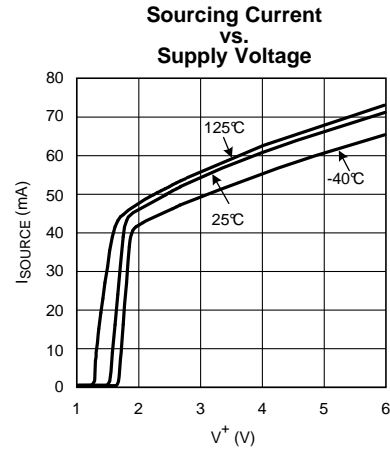


Figure 19.

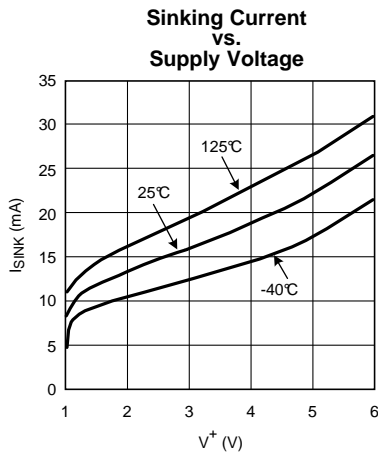


Figure 20.

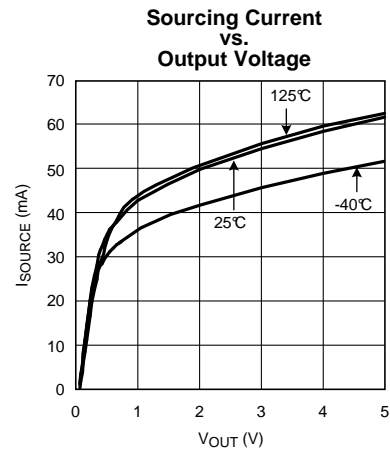


Figure 21.

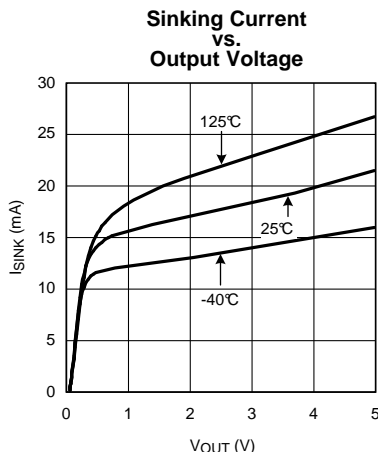


Figure 22.

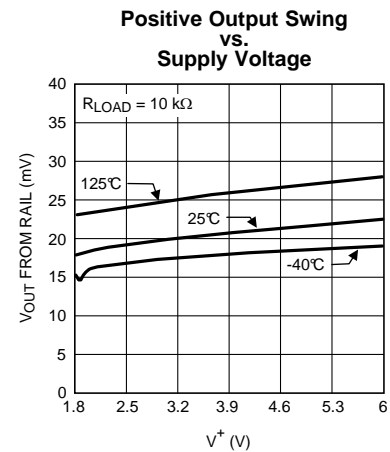


Figure 23.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

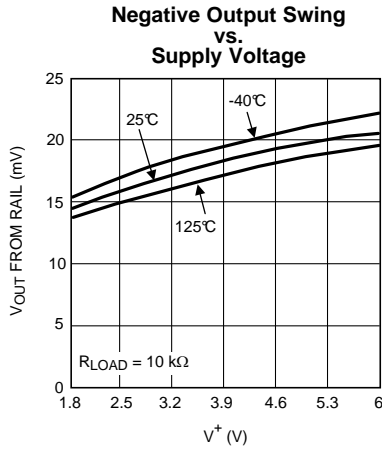


Figure 24.

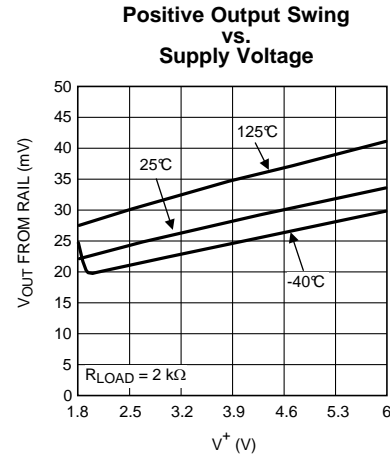


Figure 25.

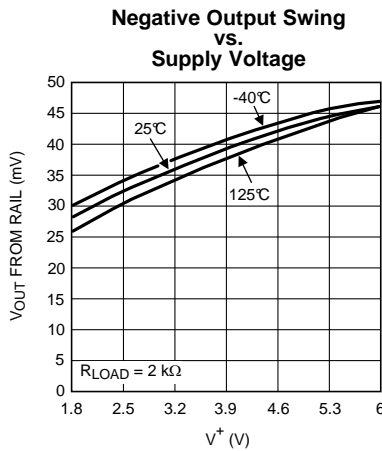


Figure 26.

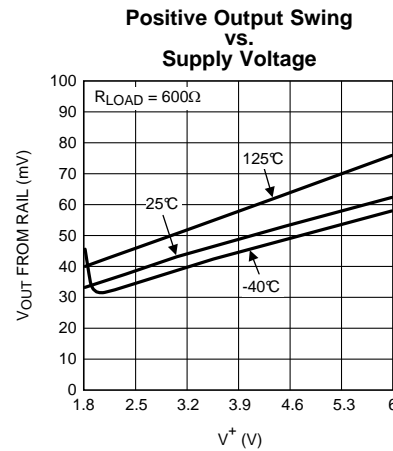


Figure 27.

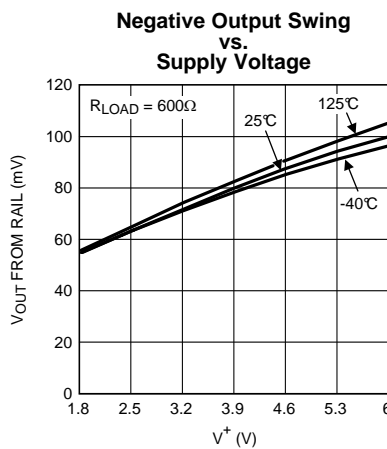


Figure 28.

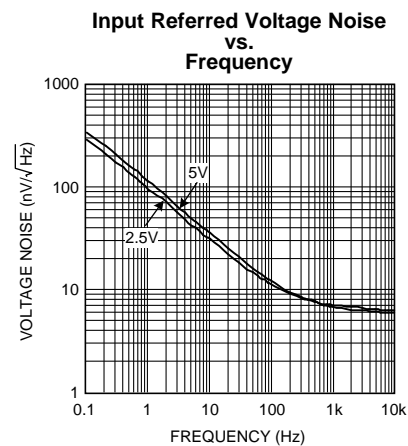


Figure 29.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

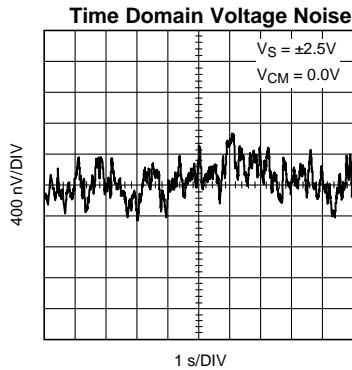


Figure 30.

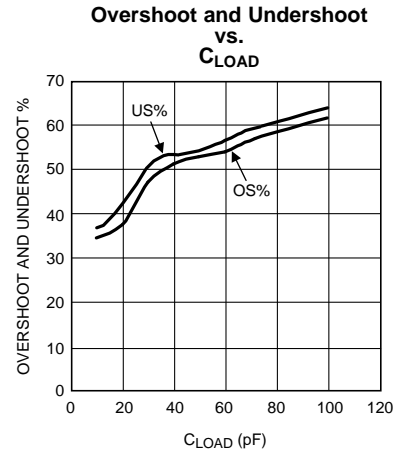


Figure 31.

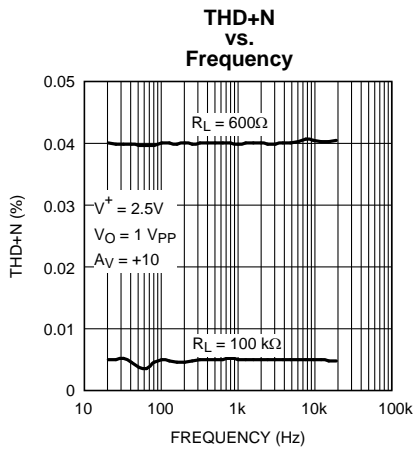


Figure 32.

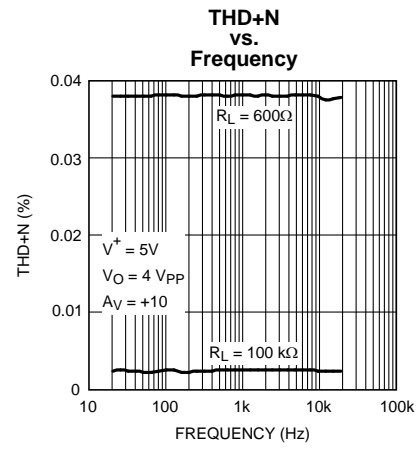


Figure 33.

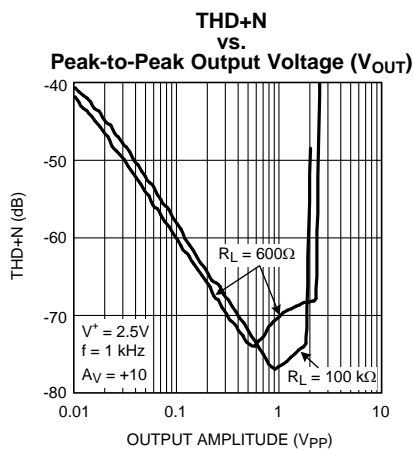


Figure 34.

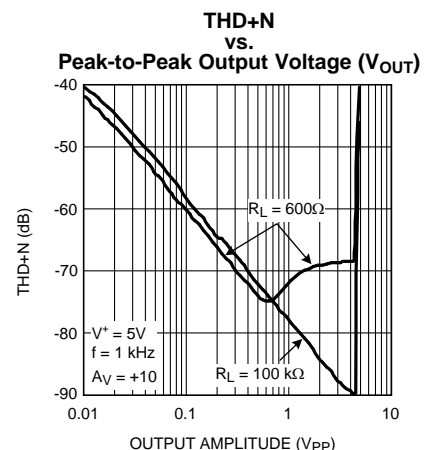


Figure 35.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

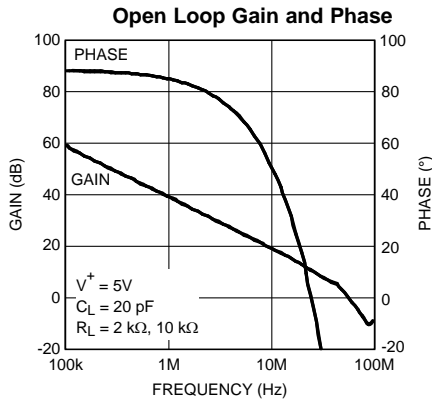


Figure 36.

**Closed Loop Output Impedance vs. Frequency**

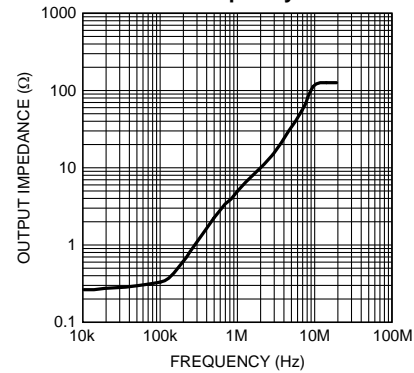


Figure 37.

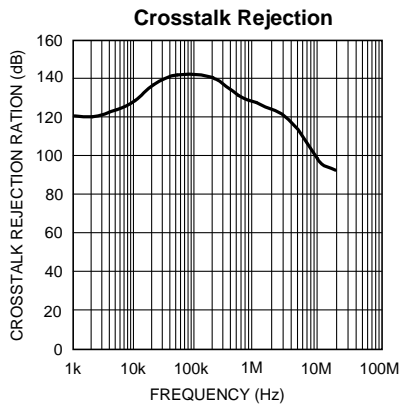


Figure 38.

**Small Signal Transient Response,  $A_V = +10$**

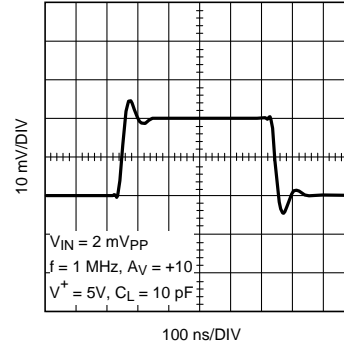


Figure 39.

**Large Signal Transient Response,  $A_V = +10$**

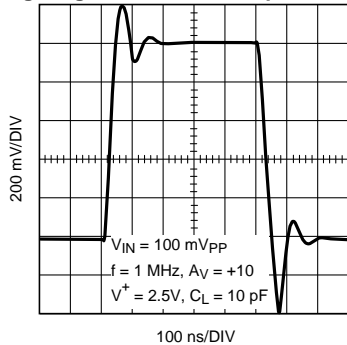


Figure 40.

**Small Signal Transient Response,  $A_V = +10$**

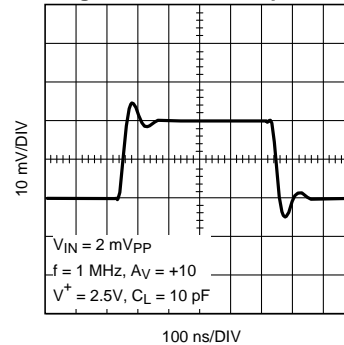
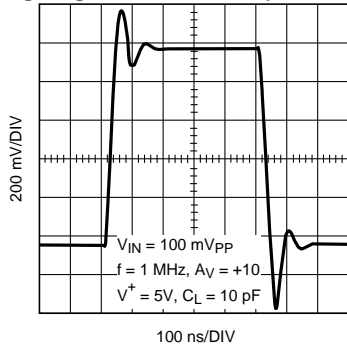


Figure 41.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

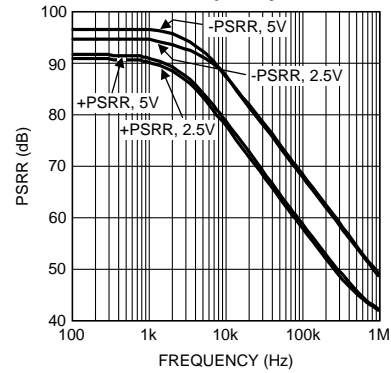
Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V^- = 0$ ,  $V^+ = 5\text{V}$ ,  $V_S = V^+ - V^-$ ,  $V_{CM} = V_S/2$ .

**Large Signal Transient Response,  $A_V = +10$**



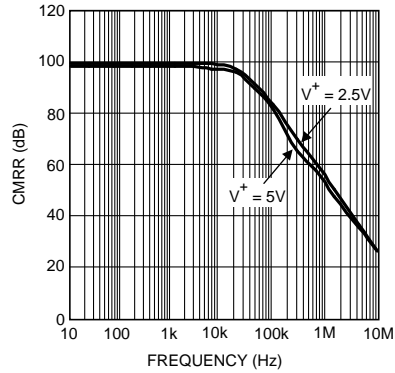
**Figure 42.**

**PSRR vs. Frequency**



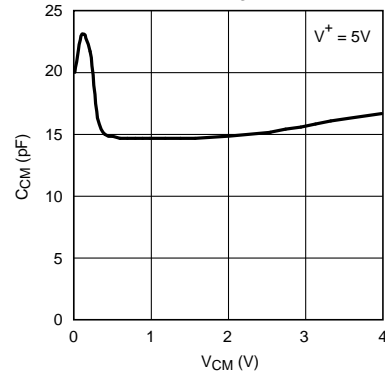
**Figure 43.**

**CMRR vs. Frequency**



**Figure 44.**

**Input Common Mode Capacitance vs.  $V_{CM}$**



**Figure 45.**

## APPLICATION INFORMATION

### ADVANTAGES OF THE LMP7717/LMP7718

#### Wide Bandwidth at Low Supply Current

The LMP7717/LMP7718 are high performance op amps that provide a GBW of 88 MHz with a gain of 10 while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in data acquisition applications.

With the proper external compensation the LMP7717 can be operated at gains of  $\pm 1$  and still maintain much faster slew rates than comparable unity gain stable amplifiers. The increase in bandwidth and slew rate is obtained without any additional power consumption over the LMP7715.

#### Low Input Referred Noise and Low Input Bias Current

The LMP7717/LMP7718 have a very low input referred voltage noise density ( $5.8 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise ( $0.01 \text{ pA}/\sqrt{\text{Hz}}$ ). This is very helpful in maintaining signal integrity, and makes the LMP7717/LMP7718 ideal for audio and sensor based applications.

#### Low Supply Voltage

The LMP7717 and the LMP7718 have performance ensured at 2.5V and 5V supply. These parts are ensured to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ , thus utilizing the entire battery lifetime. The LMP7717/LMP7718 are also ensured to be operational at 1.8V supply voltage, for temperatures between  $0^\circ\text{C}$  and  $125^\circ\text{C}$  optimizing their usage in low-voltage applications.

#### RRO and Ground Sensing

Rail-to-Rail output swing provides the maximum possible dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMP7717/LMP7718 to source more than 40 mA of current at 1.8V supply. This also limits the performance of the these parts as comparators, and hence the usage of the LMP7717 and the LMP7718 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

#### Small Size

The small footprints of the LMP7717 packages and the LMP7718 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path more susceptible to noise pick up.

The physically smaller LMP7717 or LMP7718 packages allow the op amp to be placed closer to the signal source, thus reducing noise pickup and maintaining signal integrity.

### USING THE DECOMPENSATED LMP7717

#### Advantages of Decompensated Op Amp

A unity gain stable op amp, which is fully compensated, is designed to operate with good stability down to gains of  $\pm 1$ . The large amount of compensation does provide an op amp that is relatively easy to use; however, a decompensated op amp is designed to maximize the bandwidth and slew rate without any additional power consumption. This can be very advantageous.

The LMP7717/LMP7718 require a gain of  $\pm 10$  to be stable. However, with an external compensation network (a simple RC network) these parts can be stable with gains of  $\pm 1$  and still maintain the higher slew rate. Looking at the Bode plots for the LMP7717 and its closest equivalent unity gain stable op amp, the LMP7715, one can clearly see the increased bandwidth of the LMP7717. Both plots are taken with a parallel combination of 20 pF and 10 k $\Omega$  for the output load.

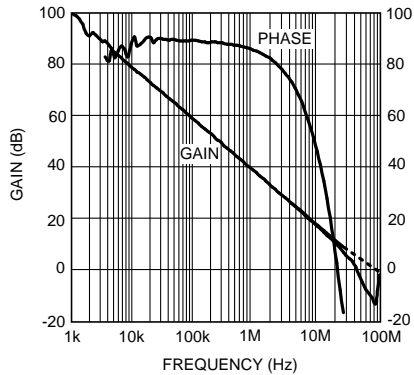
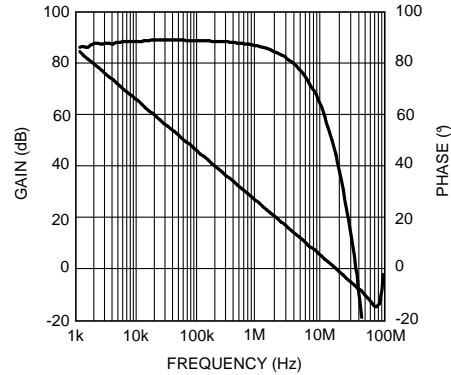
Figure 46. LMP7717  $A_{VOL}$  vs. FrequencyFigure 47. LMP7715  $A_{VOL}$  vs. Frequency

Figure 46 shows the much larger 88 MHz bandwidth of the LMP7717 as compared to the 17 MHz bandwidth of the LMP7715 shown in Figure 47. The decompensated LMP7717 has five times the bandwidth of the LMP7715.

### What is a Decompensated Op Amp?

The differences between the unity gain stable op amp and the decompensated op amp are shown in Figure 48. This Bode plot assumes an ideal two pole system. The dominant pole of the decompensated op amp is at a higher frequency,  $f_1$ , as compared to the unity gain stable op amp which is at  $f_d$  as shown in Figure 48. This is done in order to increase the speed capability of the op amp while maintaining the same power dissipation of the unity gain stable op amp. The LMP7717/LMP7718 have a dominant pole at 1.6 kHz. The unity gain stable LMP7715/LMP7716 have their dominant pole at 300 Hz.

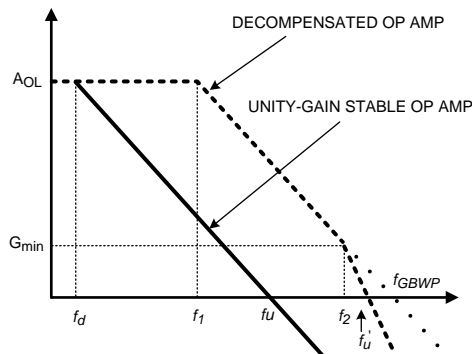


Figure 48. Open Loop Gain for Unity Gain Stable Op Amp and Decompensated Op Amp

Having a higher frequency for the dominate pole will result in:

1. The DC open loop gain ( $A_{VOL}$ ) extending to a higher frequency.
2. A wider closed loop bandwidth.
3. Better slew rate due to reduced compensation capacitance within the op amp.

The second open loop pole ( $f_2$ ) for the LMP7717/LMP7718 occurs at 45 MHz. The unity gain ( $f_u'$ ) occurs after the second pole at 51 MHz. An ideal two pole system would give a phase margin of  $45^\circ$  at the location of the second pole. The LMP7717/LMP7718 have parasitic poles close to the second pole, giving a phase margin closer to  $0^\circ$ . Therefore it is necessary to operate the LMP7717/LMP7718 at a closed loop gain of 10 or higher, or to add external compensation in order to assure stability.

For the LMP7715, the gain bandwidth product occurs at 17 MHz. The curve is constant from  $f_d$  to  $f_u$  which occurs before the second pole.

For the LMP7717/LMP7718 the GBW = 88 MHz and is constant between  $f_1$  and  $f_2$ . The second pole at  $f_2$  occurs before  $A_{VOL} = 1$ . Therefore  $f_u'$  occurs at 51 MHz, well before the GBW frequency of 88 MHz. For decompensated op amps the unity gain frequency and the GBW are no longer equal.  $G_{min}$  is the minimum gain for stability and for the LMP7717/LMP7718 this is a gain of 18 to 20 dB.

### Input Lead-Lag Compensation

The recommended technique which allows the user to compensate the LMP7717/LMP7718 for stable operation at any gain is lead-lag compensation. The compensation components added to the circuit allow the user to shape the feedback function to make sure there is sufficient phase margin when the loop gain is as low as 0 dB and still maintain the advantages over the unity gain op amp. Figure 49 shows the lead-lag configuration. Only  $R_C$  and  $C$  are added for the necessary compensation.

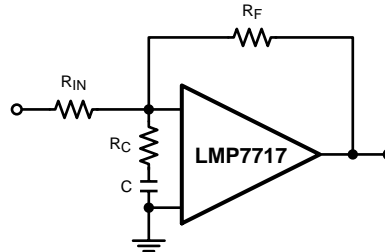


Figure 49. LMP7717 with Lead-Lag Compensation for Inverting Configuration

To cover how to calculate the compensation network values it is necessary to introduce the term called the feedback factor or  $F$ . The feedback factor  $F$  is the feedback voltage  $V_A - V_B$  across the op amp input terminals relative to the op amp output voltage  $V_{OUT}$ .

$$F = \frac{V_A - V_B}{V_{OUT}} \quad (1)$$

From feedback theory the classic form of the feedback equation for op amps is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + AF} \quad (2)$$

$A$  is the open loop gain of the amplifier and  $AF$  is the loop gain. Both are highly important in analyzing op amps. Normally  $AF \gg 1$  and so the above equation reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{F} \quad (3)$$

Deriving the equations for the lead-lag compensation is beyond the scope of this datasheet. The derivation is based on the feedback equations that have just been covered. The inverse of feedback factor for the circuit in Figure 49 is:

$$\frac{1}{F} = \left( 1 + \frac{R_F}{R_{IN}} \right) \left( \frac{1 + s(R_C + R_{IN} \parallel R_F) C}{1 + sR_C C} \right) \quad (4)$$

where  $1/F$ 's pole is located at

$$f_p = \frac{1}{2\pi R_C C} \quad (5)$$

$1/F$ 's zero is located at

$$f_z = \frac{1}{2\pi(R_C + R_{IN} \parallel R_F) C} \quad (6)$$

$$\left. \frac{1}{F} \right|_{f=0} = 1 + \frac{R_F}{R_{IN}} \quad (7)$$

The circuit gain for Figure 49 at low frequencies is  $-R_F/R_{IN}$ , but  $F$ , the feedback factor is not equal to the circuit gain. The feedback factor is derived from feedback theory and is the same for both inverting and non-inverting configurations. Yes, the feedback factor at low frequencies is equal to the gain for the non-inverting configuration.

$$\left. \frac{1}{F} \right|_{f=\infty} = \left( 1 + \frac{R_F}{R_{IN}} \right) \left( 1 + \frac{R_{IN} \parallel R_F}{R_C} \right) \quad (8)$$

From this formula, we can see that

- 1/F's zero is located at a lower frequency compared with 1/F's pole.
- 1/F's value at low frequency is  $1 + R_F/R_{IN}$ .
- This method creates one additional pole and one additional zero.
- This pole-zero pair will serve two purposes:
  - To raise the 1/F value at higher frequencies prior to its intercept with A, the open loop gain curve, in order to meet the  $G_{min} = 10$  requirement. For the LMP7717 some overcompensation will be necessary for good stability.
  - To achieve the previous purpose above with no additional loop phase delay.

Please note the constraint  $1/F \geq G_{min}$  needs to be satisfied only in the vicinity where the open loop gain A and 1/F intersect; 1/F can be shaped elsewhere as needed. The 1/F pole must occur before the intersection with the open loop gain A.

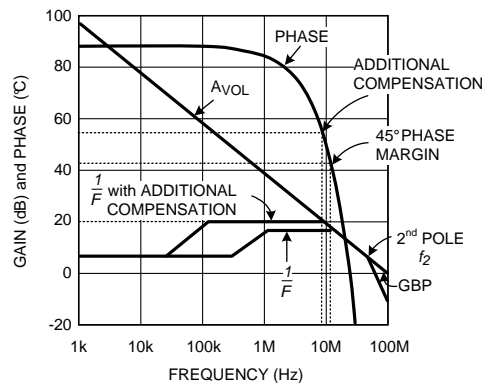
In order to have adequate phase margin, it is desirable to follow these two rules:

**Rule 1** 1/F and the open loop gain A should intersect at the frequency where there is a minimum of 45° of phase margin. When over-compensation is required the intersection point of A and 1/F is set at a frequency where the phase margin is above 45°, therefore increasing the stability of the circuit.

**Rule 2** 1/F's pole should be set at least one decade below the intersection with the open loop gain A in order to take advantage of the full 90° of phase lead brought by 1/F's pole which is F's zero. This ensures that the effect of the zero is fully neutralized when the 1/F and A plots intersect each other.

### Calculating Lead-Lag Compensation for LMP7717

Figure 50 is the same plot as Figure 46, but the  $A_{VOL}$  and phase curves have been redrawn as smooth lines to more readily show the concepts covered, and to clearly show the key parameters used in the calculations for lead-lag compensation.



**Figure 50. LMP7717/LMP7718 Simplified Bode Plot**

To obtain stable operation with gains under 10 V/V the open loop gain margin must be reduced at high frequencies to where there is a 45° phase margin when the gain margin of the circuit with the external compensation is 0 dB. The pole and zero in F, the feedback factor, control the gain margin at the higher frequencies. The distance between F and  $A_{VOL}$  is the gain margin; therefore, the unity gain point (0 dB) is where F crosses the  $A_{VOL}$  curve.

For the example being used  $R_{IN} = R_F$  for a gain of  $-1$ . Therefore  $F = 6$  dB at low frequencies. At the higher frequencies the minimum value for F is 18 dB for 45° phase margin. From Equation 5 we have the following relationship:

$$\left(1 + \frac{R_F}{R_{IN}}\right) \left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) = 18 \text{ dB} = 7.9 \quad (9)$$

Now set  $R_F = R_{IN} = R$ . With these values and solving for  $R_C$  we have  $R_C = R/5.9$ . Note that the value of  $C$  does not affect the ratio between the resistors. Once the value of the resistors is set, then the position of the pole in  $F$  must be set. A 2 k $\Omega$  resistor is used for  $R_F$  and  $R_{IN}$  in this design. Therefore the value for  $R_C$  is set at 330 $\Omega$ , the closest standard value for 2 k $\Omega$ /5.9.

Rewriting *Equation 2* to solve for the minimum capacitor value gives the following equation:

$$C = 1/(2\pi f_p R_C) \quad (10)$$

The feedback factor curve,  $F$ , intersects the  $A_{VOL}$  curve at about 12 MHz. Therefore the pole of  $F$  should not be any larger than 1.2 MHz. Using this value and  $R_C = 330\Omega$  the minimum value for  $C$  is 390 pF. [Figure 51](#) shows that there is too much overshoot, but the part is stable. Increasing  $C$  to 2.2 nF did not improve the ringing, as shown in [Figure 52](#).

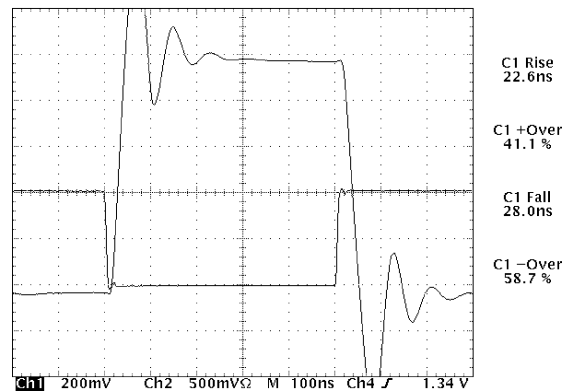


Figure 51. First Try at Compensation, Gain = -1

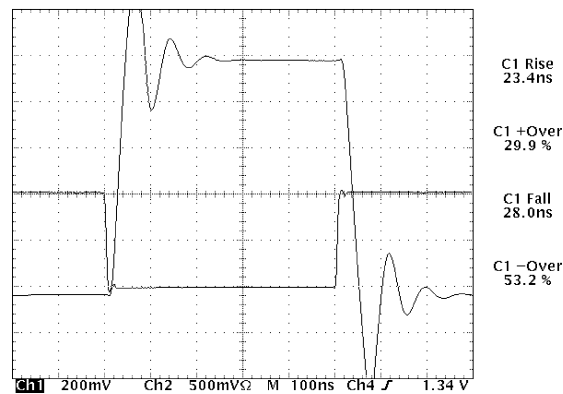
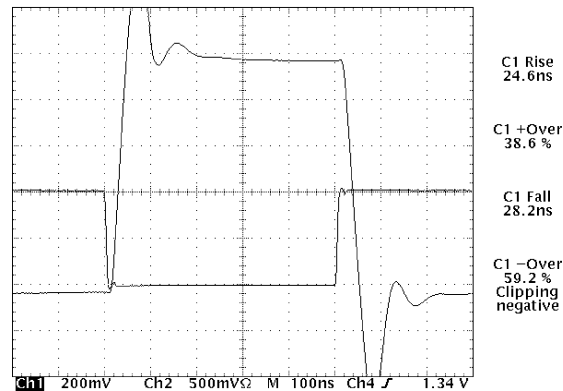
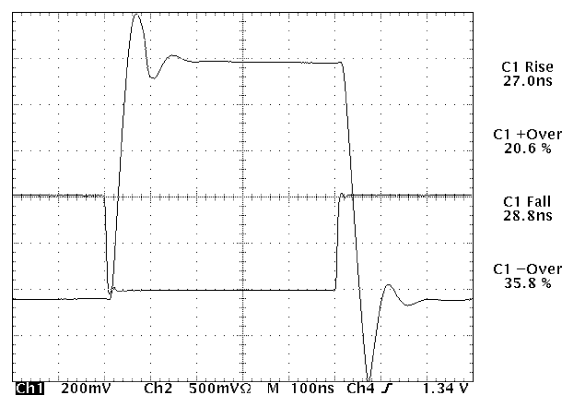


Figure 52. C Increased to 2.2 nF, Gain = -1

Some over-compensation appears to be needed for the desired overshoot characteristics. Instead of intersecting the  $A_{VOL}$  curve at 18 dB, 2 dB of over-compensation will be used, and the  $A_{VOL}$  curve will be intersected at 20 dB. Using *Equation 5* for 20 dB, or 10 V/V, the closest standard value of  $R_C$  is 240 $\Omega$ . The following two waveforms show the new resistor value with  $C = 390$  pF and 2.2 nF. [Figure 54](#) shows the final compensation and a very good response for the 1 MHz square wave.



**Figure 53.  $R_C = 240\Omega$  and  $C = 390$  pF, Gain = -1**

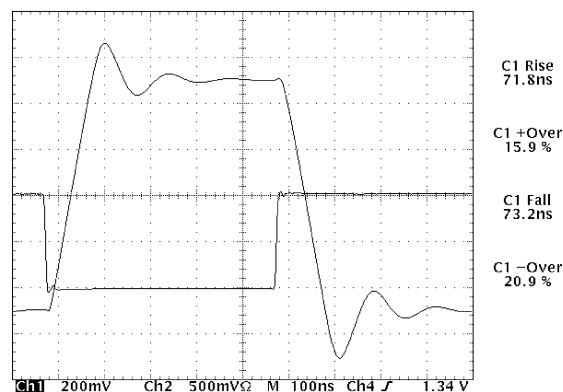


**Figure 54.  $R_C = 240\Omega$  and  $C = 2.2$  nF, Gain = -1**

To summarize, the following steps were taken to compensate the LMP7717 for a gain of -1:

1. Values for  $R_C$  and  $C$  were calculated from the Bode plot to give an expected phase margin of  $45^\circ$ . The values were based on  $R_{IN} = R_F = 2$  k $\Omega$ . These calculations gave  $R_C = 330\Omega$  and  $C = 390$  pF.
2. To reduce the ringing  $C$  was increased to 2.2 nF which moved the pole of  $F$ , the feedback factor, farther away from the  $A_{VOL}$  curve.
3. There was still too much ringing so 2 dB of over-compensation was added to  $F$ . This was done by decreasing  $R_C$  to 240 $\Omega$ .

The LMP7715 is the fully compensated part which is comparable to the LMP7717. Using the LMP7715 in the same setup, but removing the compensation network, provided the response shown in Figure 55.



**Figure 55. LMP7715 Response**

For large signal response the rise and fall times are dominated by the slew rate of the op amps. Even though both parts are quite similar the LMP7717 will give rise and fall times about 2.5 times faster than the LMP7715. This is possible because the LMP7717 is a decompensated op amp and even though it is being used at a gain of  $-1$ , the speed is preserved by using a good technique for external compensation.

### Non-Inverting Compensation

For the non-inverting amp the same theory applies for establishing the needed compensation. When setting the inverting configuration for a gain of  $-1$ ,  $F$  has a value of 2. For the non-inverting configuration both  $F$  and the actual gain are the same, making the non-inverting configuration more difficult to compensate. Using the same circuit as shown in Figure 49, but setting up the circuit for non-inverting operation (gain of  $+2$ ) results in similar performance as the inverting configuration with the inputs set to half the amplitude to compensate for the additional gain. Figure 56 below shows the results.

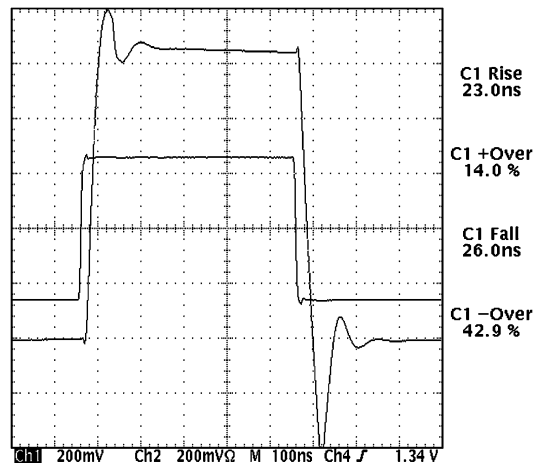


Figure 56.  $R_C = 240\Omega$  and  $C = 2.2 \text{ nF}$ , Gain =  $+2$

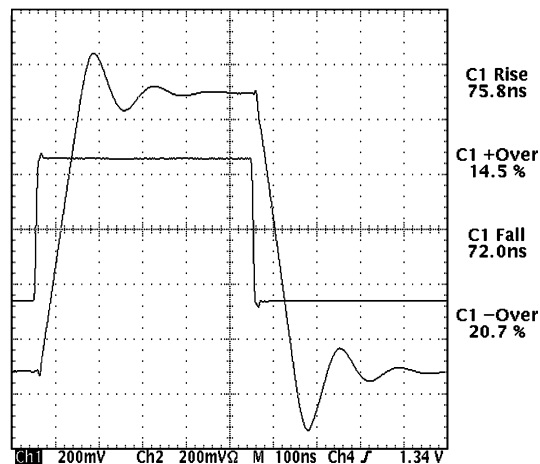
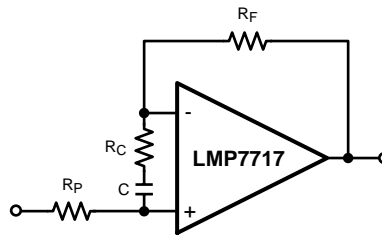


Figure 57. LMP7715 Response Gain =  $+2$

The response shown in Figure 56 is close to the response shown in Figure 54. The part is actually slightly faster in the non-inverting configuration. Decreasing the value of  $R_C$  to around  $200\Omega$  can decrease the negative overshoot but will have slightly longer rise and fall times. The other option is to add a small resistor in series with the input signal. Figure 57 shows the performance of the LMP7715 with no compensation. Again the decompensated parts are almost 2.5 times faster than the fully compensated op amp.

The most difficult op amp configuration to stabilize is the gain of  $+1$ . With proper compensation the LMP7717/LMP7718 can be used in this configuration and still maintain higher speeds than the fully compensated parts. Figure 58 shows the gain = 1, or the buffer configuration, for these parts.

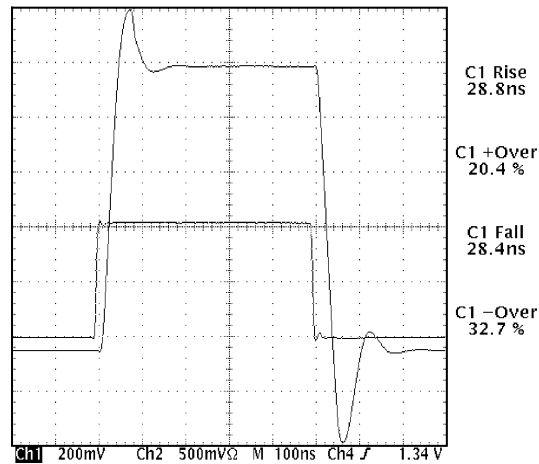


**Figure 58. LMP7717 with Lead-Lag Compensation for Non-Inverting Configuration**

Figure 58 is the result of using Equation 5 and additional experimentation in the lab.  $R_P$  is not part of Equation 5, but it is necessary to introduce another pole at the input stage for good performance at gain = +1. Equation 5 is shown below with  $R_{IN} = \infty$ .

$$\left(1 + \frac{R_F}{R_C}\right) = 18 \text{ dB} = 7.9 \quad (11)$$

Using 2 k $\Omega$  for  $R_F$  and solving for  $R_C$  gives  $R_C = 2000/6.9 = 290\Omega$ . The closest standard value for  $R_C$  is 300 $\Omega$ . After some fine tuning in the lab  $R_C = 330\Omega$  and  $R_P = 1.5 \text{ k}\Omega$  were chosen as the optimum values.  $R_P$  together with the input capacitance at the non-inverting pin inserts another pole into the compensation for the LMP7717. Adding this pole and slightly reducing the compensation for 1/F (using a slightly higher resistor value for  $R_C$ ) gives the optimum response for a gain of +1. Figure 59 is the response of the circuit shown in Figure 58. Figure 60 shows the response of the LMP7715 in the buffer configuration with no compensation and  $R_P = R_F = 0$ .



**Figure 59.  $R_C = 330\Omega$  and  $C = 10 \text{ nF}$ , Gain = +1**

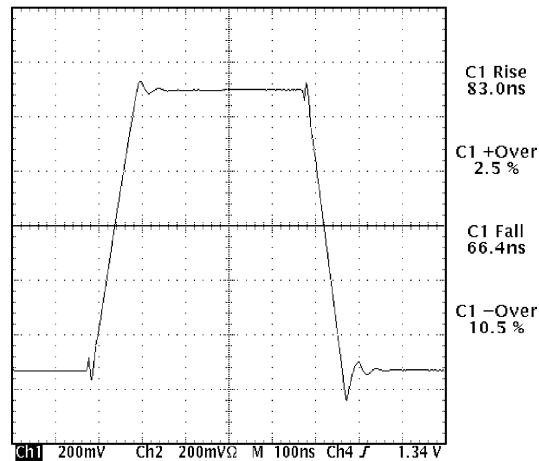


Figure 60. LMP7715 Response Gain = +1

With no increase in power consumption the decompensated op amp offers faster speed than the compensated equivalent part . These examples used  $R_F = 2 \text{ k}\Omega$ . This value is high enough to be easily driven by the LMP7717/LMP7718, yet small enough to minimize the effects from the parasitic capacitance of both the PCB and the op amp.

**NOTE**

When using the LMP7717/LMP7718, proper high frequency PCB layout must be followed. The GBW of these parts is 88 MHz, making the PCB layout significantly more critical than when using the compensated counterparts which have a GBW of 17 MHz.

**TRANSIMPEDANCE AMPLIFIER**

An excellent application for either the LMP7717 or the LMP7718 is as a transimpedance amplifier. With a GBW product of 88 MHz these parts are ideal for high speed data transmission by light. The circuit shown on the front page of the datasheet is the circuit used to test the LMP7717/LMP7718 as transimpedance amplifiers. The only change is that  $V_B$  is tied to the  $V_{CC}$  of the part, thus the direction of the diode is reversed from the circuit shown on the front page.

Very high speed components were used in testing to check the limits of the LMP7717/LMP7718 in a transimpedance configuration. The photodiode part number is PIN-HR040 from OSI Optoelectronics. The diode capacitance for this part is only about 7 pF for the 2.5V bias used ( $V_{CC}$  to virtual ground). The rise time for this diode is 1 nsec. A laser diode was used for the light source. Laser diodes have on and off times under 5 nsec. The speed of the selected optical components allowed an accurate evaluation of the LMP7717 as a transimpedance amplifier. Its evaluation board for decompensated op amps, PN 551013271-001 A, was used and only minor modifications were necessary and no traces had to be cut.

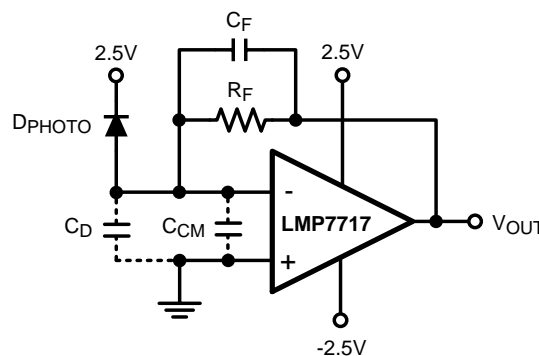
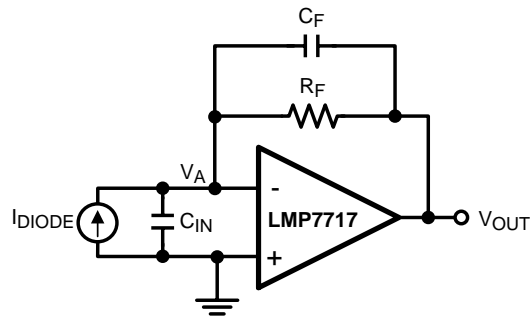


Figure 61. Transimpedance Amplifier

Figure 61 is the complete schematic for a transimpedance amplifier. Only the supply bypass capacitors are not shown.  $C_D$  represents the photodiode capacitance which is given on its datasheet.  $C_{CM}$  is the input common mode capacitance of the op amp and, for the LMP7717 it is shown in the last graph of the **TYPICAL PERFORMANCE CHARACTERISTICS** section of this datasheet. In Figure 61 the inverting input pin of the LMP7717 is kept at virtual ground. Even though the diode is connected to the 2.5V line, a power supply line is AC ground, thus  $C_D$  is connected to ground.

Figure 62 shows the schematic needed to derive F, the feedback factor, for a transimpedance amplifier. In Figure 62,  $C_D + C_{CM} = C_{IN}$ . Therefore it is critical that the designer knows the diode capacitance and the op amp input capacitance. The photodiode is close to an ideal current source once its capacitance is included in the model. What kind of circuit is this? Without  $C_F$  there is only an input capacitor and a feedback resistor. This circuit is a differentiator! Remember, differentiator circuits are inherently unstable and must be compensated. In this case  $C_F$  compensates the circuit.



**Figure 62. Transimpedance Feedback Model**

Using feedback theory,  $F = V_A/V_{OUT}$ , this becomes a voltage divider giving the following equation:

$$F = \frac{1 + sC_F R_F}{1 + sR_F (C_F + C_{IN})} \quad (12)$$

The noise gain is  $1/F$ . Because this is a differentiator circuit, a zero must be inserted. The location of the zero is given by:

$$f_z = \frac{1}{1 + sR_F (C_F + C_{IN})} \quad (13)$$

$C_F$  has been added for stability. The addition of this part adds a pole to the circuit. The pole is located at:

$$f_p = \frac{1}{1 + sC_F R_F} \quad (14)$$

To attain maximum bandwidth and still have good stability the pole is to be located on the open loop gain curve which is A. If additional compensation is required one can always increase the value of  $C_F$ , but this will also reduce the bandwidth of the circuit. Therefore  $A = 1/F$ , or  $AF = 1$ . For A the equation is:

$$A = \frac{\omega_{GBW}}{\omega} = \frac{f_{GBW}}{f} \quad (15)$$

The expression  $f_{GBW}$  is the gain bandwidth product of the part. For a unity gain stable part this is the frequency where  $A = 1$ . For the LMP7717  $f_{GBW} = 88$  MHz. Multiplying A and F results in the following equation:

$$AF \Big|_{f_p} = \frac{f_{GBW}}{f} \times \frac{1 + sC_F R_F}{1 + sR_F (C_F + C_{IN})} =$$

$$\frac{f_{GBW}}{f} \times \frac{\sqrt{1 + \left(\frac{C_F R_F}{C_F R_F}\right)^2}}{\sqrt{1 + \left(\frac{R_F (C_F + C_{IN})}{C_F R_F}\right)^2}} = 1 \quad (16)$$

For the above equation  $s = j\omega$ . To find the actual amplitude of the equation the square root of the square of the real and imaginary parts are calculated. At the intersection of F and A, we have:

$$\omega = \frac{1}{C_F R_F} \quad (17)$$

After a bit of algebraic manipulation the above equation reduces to:

$$1 + \left( \frac{C_F + C_{IN}}{C_F} \right)^2 = 8\pi^2 f_{GBW}^2 R_F^2 C_F^2 \quad (18)$$

In the above equation the only unknown is  $C_F$ . In trying to solve this equation the fourth power of  $C_F$  must be dealt with. An excel spread sheet with this equation can be used and all the known values entered. Then through iteration, the value of  $C_F$  when both sides are equal will be found. That is the correct value for  $C_F$  and of course the closest standard value is used for  $C_F$ .

Before moving to the lab, the transfer function of the transimpedance amplifier must be found and the units must be in Ohms.

$$V_{OUT} = \frac{-R_F}{1 + sC_F R_F} \times I_{DIODE} \quad (19)$$

The LMP7717 was evaluated for  $R_F = 10 \text{ k}\Omega$  and  $100 \text{ k}\Omega$ , representing a somewhat lower gain configuration and with the  $100 \text{ k}\Omega$  feedback resistor a fairly high gain configuration. The  $R_F = 10 \text{ k}\Omega$  is covered first. Looking at the *Input Common Mode Capacitance vs.  $V_{CM}$*  chart for  $C_{CM}$  for the operating point selected  $C_{CM} = 15 \text{ pF}$ . Note that for split supplies  $V_{CM} = 2.5\text{V}$ ,  $C_{IN} = 22 \text{ pF}$  and  $f_{GBW} = 88 \text{ MHz}$ . Solving for  $C_F$  the calculated value is  $1.75 \text{ pF}$ , so  $1.8 \text{ pF}$  is selected for use. Checking the frequency of the pole finds that it is at  $8.8 \text{ MHz}$ , which is right at the minimum gain recommended for this part. Some over compensation was necessary for stability and the final selected value for  $C_F$  is  $2.7 \text{ pF}$ . This moves the pole to  $5.9 \text{ MHz}$ . Figure 63 and Figure 64 show the rise and fall times obtained in the lab with a  $1\text{V}$  output swing. The laser diode was difficult to drive due to thermal effects making the starting and ending point of the pulse quite different, therefore the two separate scope pictures.

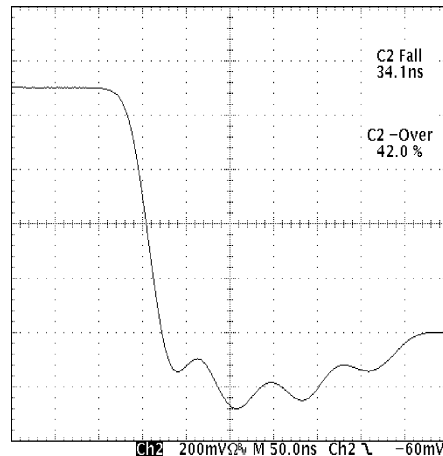
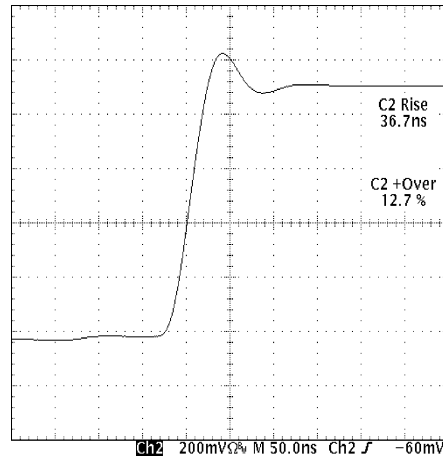


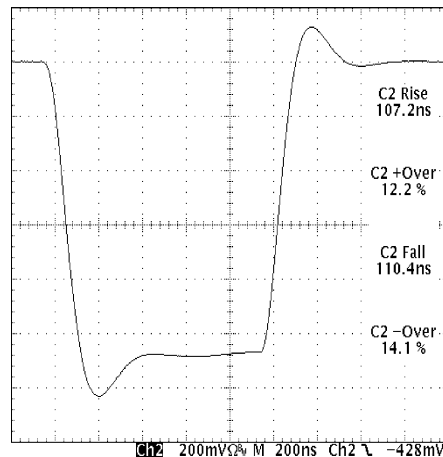
Figure 63. Fall Time



**Figure 64. Rise Time**

In [Figure 63](#) the ringing and the hump during the on time is from the laser. The higher drive levels for the laser gave ringing in the light source as well as light changing from the thermal characteristics. The hump is due to the thermal characteristics.

Solving for  $C_F$  using a 100 k $\Omega$  feedback resistor, the calculated value is 0.54 pF. One of the problems with more gain is the very small value for  $C_F$ . A 0.5 pF capacitor was used, its measured value being 0.64 pF. For the 0.64 pF location the pole is at 2.5 MHz. [Figure 65](#) shows the response for a 1V output.



**Figure 65. High Gain Response**

A transimpedance amplifier is an excellent application for the LMP7717. Even with the high gain using a 100 k $\Omega$  feedback resistor, the bandwidth is still well over 1 MHz. Other than a little over compensation for the 10 k $\Omega$  feedback resistor configuration using the LMP7717 was quite easy. Of course a very good board layout was also used for this test.

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## REVISION HISTORY

<b>Changes from Revision G (March 2013) to Revision H</b>	<b>Page</b>
<ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<a href="#">26</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7717MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 17MA	<a href="#">Samples</a>
LMP7717MAE/NOPB	ACTIVE	SOIC	D	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 17MA	<a href="#">Samples</a>
LMP7717MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AT4A	<a href="#">Samples</a>
LMP7717MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AT4A	<a href="#">Samples</a>
LMP7717MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AT4A	<a href="#">Samples</a>
LMP7718MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA	<a href="#">Samples</a>
LMP7718MAE/NOPB	ACTIVE	SOIC	D	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA	<a href="#">Samples</a>
LMP7718MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA	<a href="#">Samples</a>
LMP7718MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AP4A	<a href="#">Samples</a>
LMP7718MME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AP4A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

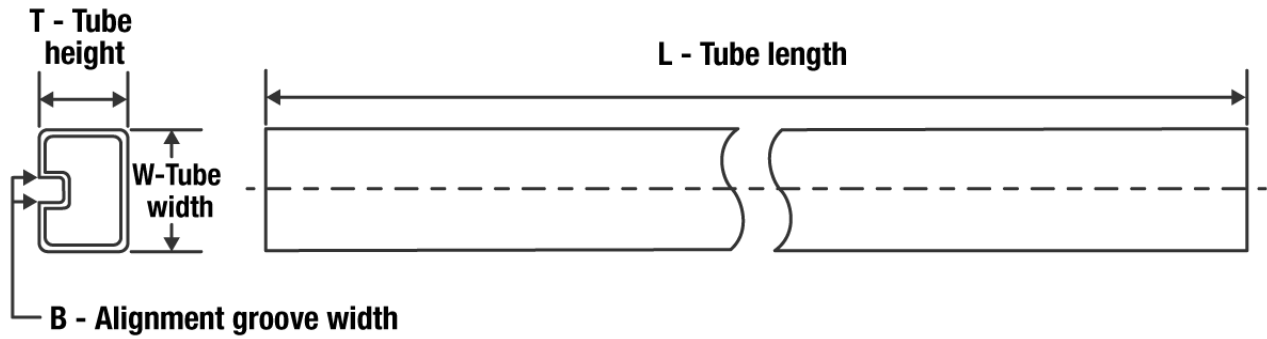

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7717MAE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7717MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7717MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7717MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7718MAE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7718MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP7718MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7718MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7717MAE/NOPB	SOIC	D	8	250	208.0	191.0	35.0
LMP7717MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMP7717MFE/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LMP7717MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMP7718MAE/NOPB	SOIC	D	8	250	208.0	191.0	35.0
LMP7718MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0
LMP7718MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMP7718MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMP7717MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP7718MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

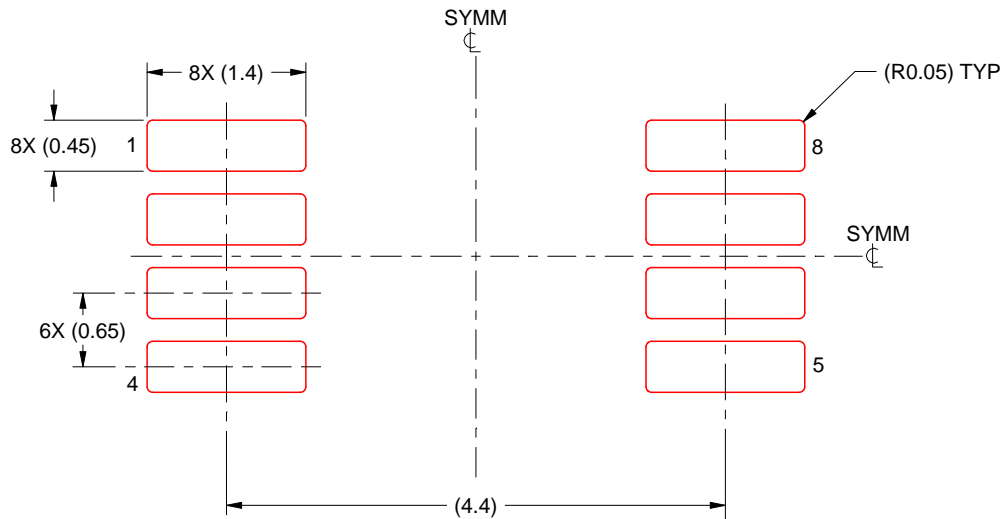
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

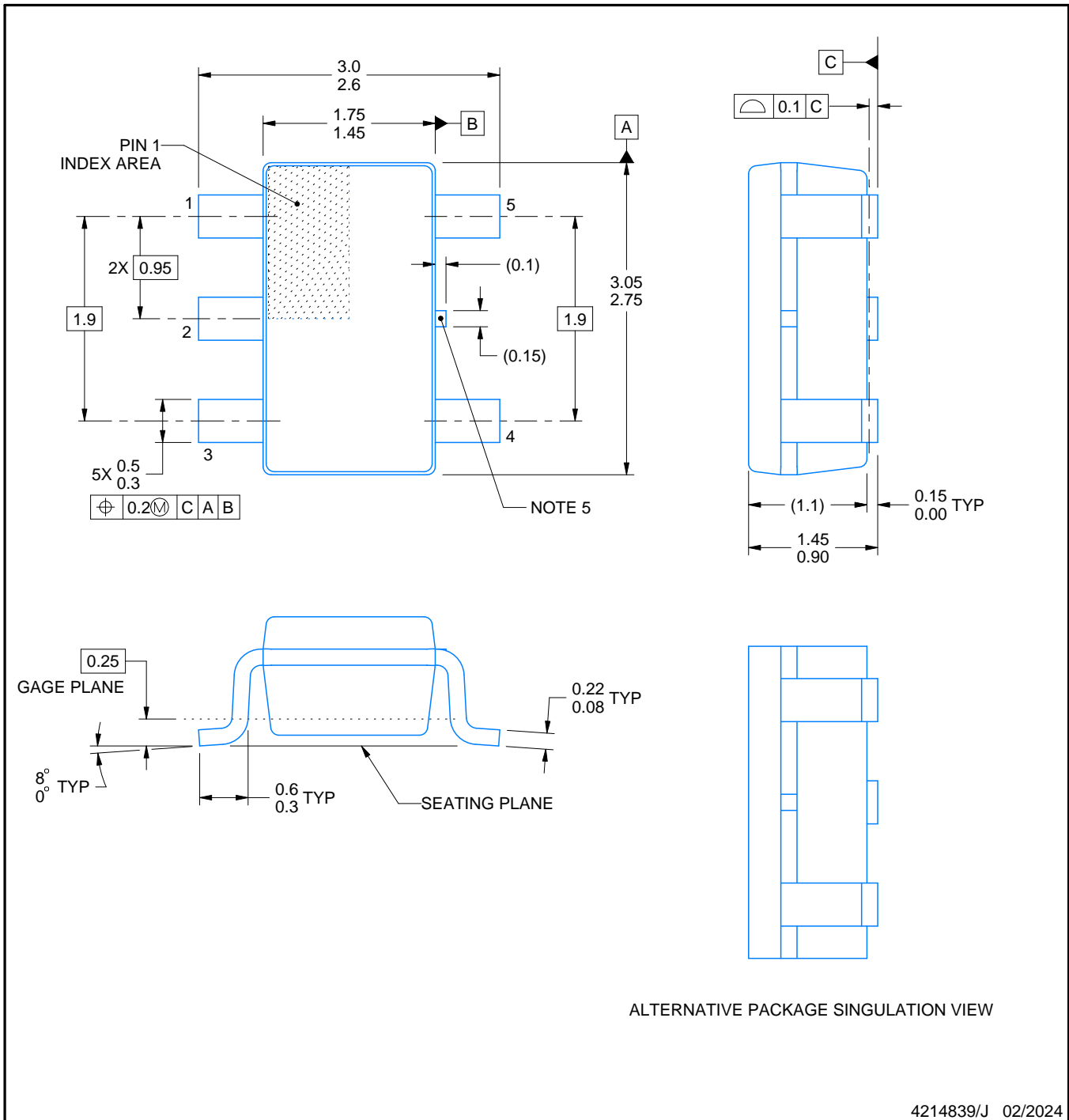
# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

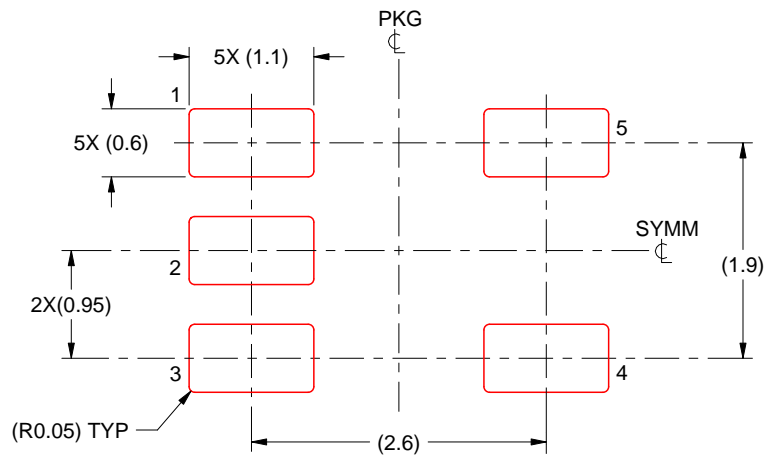


# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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