



**THE DATASHEET OF
AD5721RBRUZ-RL7**



FEATURES

- 8 software-programmable output ranges: 0 V to +5 V, 0 V to +10 V, 0 V to +16 V, 0 V to +20 V, ±3 V, ±5 V, ±10 V, and -2.5 V to +7.5 V; 5% overrange**
- Low drift 2.5 V reference: ±2 ppm/°C typical**
- Total unadjusted error (TUE): 0.1% FSR maximum**
- 16-bit resolution: ±2 LSB maximum INL**
- Guaranteed monotonicity: ±1 LSB maximum**
- Single channel, 16-/12-bit DACs**
- Settling time: 7.5 μs typical**
- Integrated reference buffers**
- Low noise: 35 nV/√Hz**
- Low glitch: 1 nV-sec (0 V to 5 V range)**
- 1.7 V to 5.5 V digital supply range**
- Asynchronous updating via $\overline{\text{LDAC}}$**
- Asynchronous $\overline{\text{RESET}}$ to zero scale/midscale**
- DSP-/microcontroller-compatible serial interface**
- Robust 4 kV HBM ESD rating**
- 16-lead, 3 mm × 3 mm LFCSP package**
- 16-lead TSSOP package**
- Operating temperature range: -40°C to +125°C**

APPLICATIONS

- Industrial automation
- Instrumentation, data acquisition
- Open-/closed-loop servo control, process control
- Programmable logic controllers

GENERAL DESCRIPTION

The AD5761R/AD5721R are single channel, 16-/12-bit serial input, voltage output, digital-to-analog converters (DACs). They operate from single supply voltages from +4.75 V to +30 V or dual supply voltages from -16.5 V to 0 V V_{SS} and +4.75 V to +16.5 V V_{DD} . The integrated output amplifier, reference buffer, and reference provide a very easy to use, universal solution.

The devices offer guaranteed monotonicity, integral nonlinearity (INL) of ±2 LSB maximum, 35 nV/√Hz noise, and 7.5 μs settling time on selected ranges.

The AD5761R/AD5721R use a serial interface that operates at clock rates of up to 50 MHz and are compatible with DSP and microcontroller interface standards. Double buffering allows the asynchronous updating of the DAC output. The input coding is user-selectable twos complement or straight binary. The asynchronous reset function resets all registers to their default state. The output range is user selectable, via the RA[2:0] bits in the control register.

The devices available in a 3 mm × 3 mm LFCSP package and a 16-lead TSSOP package offer guaranteed specifications over the -40°C to +125°C industrial temperature range.

FUNCTIONAL BLOCK DIAGRAM

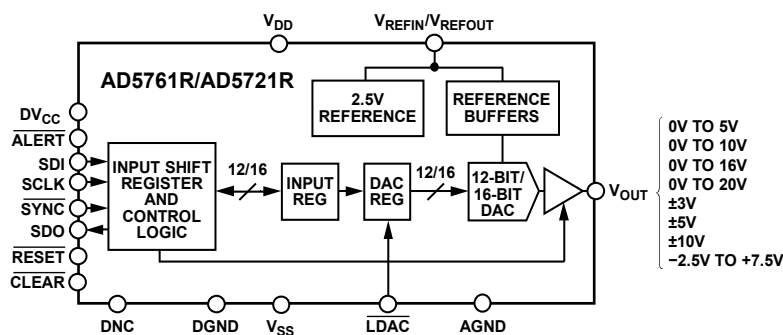


Figure 1.

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1/2018—Rev. B to Rev. C

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10/2016—Rev. A to Rev. B

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5/2015—Rev. 0 to Rev. A

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Added Figure 79	35
Updated Outline Dimensions	35
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11/2014—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD}^1 = 4.75 \text{ V to } 30 \text{ V}$, $V_{SS}^1 = -16.5 \text{ V to } 0 \text{ V}$, $AGND = DGND = 0 \text{ V}$, $V_{REFIN}/V_{REFOUT} = 2.5 \text{ V external}$, $DV_{CC} = 1.7 \text{ V to } 5.5 \text{ V}$, $R_{LOAD} = 1 \text{ k}\Omega$ for all ranges except $0 \text{ V to } 16 \text{ V}$ and $0 \text{ V to } 20 \text{ V}$ for which $R_{LOAD} = 2 \text{ k}\Omega$, $C_{LOAD} = 200 \text{ pF}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter ²	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Programmable Output Ranges	0		5	V	External reference ³ and internal reference, outputs unloaded
	0		10	V	
	0		16	V	
	0		20	V	
	-2.5		+7.5	V	
	-3		+3	V	
	-5		+5	V	
	-10		+10	V	
AD5761R					
Resolution	16			Bits	
Relative Accuracy, INL					
A Grade	-8		+8	LSB	External reference ³ and internal reference
B Grade ⁴	-2		+2	LSB	All ranges except $0 \text{ V to } 16 \text{ V}$ and $0 \text{ V to } 20 \text{ V}$, $V_{REFIN}/V_{REFOUT} = 2.5 \text{ V external}$ and internal reference
Differential Nonlinearity, DNL	-1		+1	LSB	
AD5721R					
Resolution	12			Bits	
Relative Accuracy, INL					
B Grade	-0.5		+0.5	LSB	External reference ³ and internal reference
Differential Nonlinearity, DNL	-0.5		+0.5	LSB	
Zero-Scale Error	-6		+6	mV	All ranges except $\pm 10 \text{ V}$ and $0 \text{ V to } 20 \text{ V}$, external reference ³
	-10		+10	mV	$0 \text{ V to } 20 \text{ V}$, $\pm 10 \text{ V}$ ranges, external reference ³
	-6		+6	mV	All ranges except $\pm 5 \text{ V}$, $\pm 10 \text{ V}$ and $0 \text{ V to } 20 \text{ V}$, internal reference
	-8		+8	mV	$\pm 5 \text{ V}$ range, internal reference
	-9		+9	mV	$0 \text{ V to } 20 \text{ V}$ range, internal reference
	-13		+13	mV	$\pm 10 \text{ V}$ range, internal reference
Zero-Scale Temperature Coefficient (TC) ⁵		± 5		$\mu\text{V}/^\circ\text{C}$	Unipolar ranges, external reference ³ and internal reference
		± 15		$\mu\text{V}/^\circ\text{C}$	Bipolar ranges, external reference ³ and internal reference
Bipolar Zero Error	-5		+5	mV	All bipolar ranges except $\pm 10 \text{ V}$
	-7		+7	mV	$\pm 10 \text{ V}$ output range
Bipolar Zero TC ⁵		± 2		$\mu\text{V}/^\circ\text{C}$	$\pm 3 \text{ V}$ range, external reference ³ and internal reference
		± 5		$\mu\text{V}/^\circ\text{C}$	All bipolar ranges except $\pm 3 \text{ V}$ range, external reference ³ and internal reference
Offset Error	-6		+6	mV	All ranges except $\pm 10 \text{ V}$ and $0 \text{ V to } 20 \text{ V}$, external reference ³
	-10		+10	mV	$0 \text{ V to } 20 \text{ V}$, $\pm 10 \text{ V}$ ranges, external reference ³
	-6		+6	mV	All ranges except $\pm 5 \text{ V}$, $\pm 10 \text{ V}$, and $0 \text{ V to } 20 \text{ V}$; internal reference
	-8		+8	mV	$\pm 5 \text{ V}$ range, internal reference
	-9		+9	mV	$0 \text{ V to } 20 \text{ V}$ range, internal reference
	-13		+13	mV	$\pm 10 \text{ V}$ range, internal reference

Parameter ²	Min	Typ	Max	Unit	Test Conditions/Comments
Offset Error TC ⁵		±5		μV/°C	Unipolar ranges, external reference ³ and internal reference
		±15		μV/°C	Bipolar ranges, external reference ³ and internal reference
Gain Error	−0.1		+0.1	% FSR	External reference ³
	−0.15		+0.15	% FSR	Internal reference
Gain Error TC ⁵		±1.5		ppm FSR/°C	External reference ³ and internal reference
TUE	−0.1		+0.1	% FSR	External reference ³
	−0.15		+0.15	% FSR	Internal reference
REFERENCE INPUT (EXTERNAL) ⁵					
Reference Input Voltage (V _{REF})		2.5		V	±1% for specified performance
Input Current	−2	±0.5	+2	μA	
Reference Range	2		3	V	
REFERENCE OUTPUT (INTERNAL) ⁵					
Output Voltage		2.5		V	±3 mV, at ambient temperature
Voltage Reference TC		2	5	ppm/°C	
Output Impedance		25		kΩ	
Output Voltage Noise		6		μV p-p	0.1 Hz to 10 Hz
Noise Spectral Density		10		nV/√Hz	At ambient; f = 10 kHz
Line Regulation		6		μV/V	At ambient
Thermal Hysteresis		80		ppm	First temperature cycle
Start-Up Time		3.5		ms	Coming out of power-down mode with a 10 nF capacitor on the V _{REFIN} /V _{REFOUT} pin to improve noise performance; outputs unloaded
OUTPUT CHARACTERISTICS ⁵					
Output Voltage Range	−V _{OUT}		+V _{OUT}		See Table 7 for the different output voltage ranges available
	−10		+10	V	V _{DD} /V _{SS} = ±11 V, ±10 V output range
	−10.5		+10.5	V	V _{DD} /V _{SS} = ±11 V, ±10 V output range with 5% overrange
Capacitive Load Stability			1	nF	
Headroom		0.5	1	V	R _{LOAD} = 1 kΩ for all ranges except 0 V to 16 V and 0 V to 20 V ranges (R _{LOAD} = 2 kΩ)
Output Voltage TC		±3		ppm FSR/°C	±10 V range, external reference
Short-Circuit Current		25		mA	Short on the V _{OUT} pin
Resistive Load			1	kΩ	All ranges except 0 V to 16 V and 0 V to 20 V
			2	kΩ	0 V to 16 V, 0 V to 20 V ranges
Load Regulation		0.3		mV/mA	Outputs unloaded
DC Output Impedance		0.5		Ω	Outputs unloaded
LOGIC INPUTS ⁵					DV _{CC} = 1.7 V to 5.5 V, JEDEC compliant
Input Voltage					
High, V _{IH}	0.7 × DV _{CC}			V	
Low, V _{IL}			0.3 × DV _{CC}	V	
Input Current					
Leakage Current	−1		+1	μA	SDI, SCLK, SYNC
	−1		+1	μA	LDAC, CLEAR, RESET pins held high
	−55			μA	LDAC, CLEAR, RESET pins held low
Pin Capacitance		5		pF	Per pin, outputs unloaded

Parameter ²	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (SDO, ALERT)⁵					
Output Voltage					
Low, V_{OL}			0.4	V	$DV_{CC} = 1.7\text{ V to }5.5\text{ V}$, sinking 200 μA
High, V_{OH}	$DV_{CC} - 0.5$			V	$DV_{CC} = 1.7\text{ V to }5.5\text{ V}$, sourcing 200 μA
High Impedance, SDO Pin					
Leakage Current	-1		+1	μA	
Pin Capacitance		5		pF	
POWER REQUIREMENTS					
V_{DD}	4.75		30	V	
V_{SS}	-16.5		0	V	
DV_{CC}	1.7		5.5	V	
I_{DD}		5.1	6.5	mA	Outputs unloaded, external reference
I_{SS}		1	3	mA	Outputs unloaded
$D I_{CC}$		0.005	1	μA	$V_{IH} = DV_{CC}$, $V_{IL} = \text{DGND}$
Power Dissipation		67.1		mW	$\pm 11\text{ V}$ operation, outputs unloaded, TSSOP package
DC Power Supply Rejection Ratio (PSRR) ⁵		0.1		mV/V	$V_{DD} \pm 10\%$, $V_{SS} = -15\text{ V}$
AC PSRR ⁵		0.1		mV/V	$V_{SS} \pm 10\%$, $V_{DD} = +15\text{ V}$
		65		dB	$V_{DD} \pm 200\text{ mV}$, 50 Hz/60 Hz, $V_{SS} = -15\text{ V}$, internal reference, $C_{LOAD} = 100\text{ nF}$
		65		dB	$V_{SS} \pm 200\text{ mV}$, 50 Hz/60 Hz, $V_{DD} = +15\text{ V}$, internal reference, $C_{LOAD} = 100\text{ nF}$
		80		dB	$V_{DD} \pm 200\text{ mV}$, 50 Hz/60 Hz, $V_{SS} = -15\text{ V}$, external reference, $C_{LOAD} = \text{unloaded}$
		80		dB	$V_{SS} \pm 200\text{ mV}$, 50 Hz/60 Hz, $V_{DD} = +15\text{ V}$, external reference, $C_{LOAD} = \text{unloaded}$

¹ For specified performance, headroom requirement is 1 V.

² Temperature range: -40°C to $+125^{\circ}\text{C}$, typical at $+25^{\circ}\text{C}$.

³ External reference means 2 V to 2.85 V with overrange and 2 V to 3 V without overrange.

⁴ Integral nonlinearity error is specified at $\pm 4\text{ LSB}$ (min/max) for 16 V and 20 V ranges with $V_{REFIN}/V_{REFOUT} = 2.5\text{ V}$ external and internal, and for all ranges with $V_{REFIN}/V_{REFOUT} = 2\text{ V}$ to 2.85 V with overrange and 2 V to 3 V without overrange.

⁵ Guaranteed by design and characterization, not production tested.

AC PERFORMANCE CHARACTERISTICS

$V_{DD}^1 = 4.75 \text{ V to } 30 \text{ V}$, $V_{SS}^1 = -16.5 \text{ V to } 0 \text{ V}$, $AGND = DGND = 0 \text{ V}$, $V_{REFIN}/V_{REFOUT} = 2.5 \text{ V external}$, $DV_{CC} = 1.7 \text{ V to } 5.5 \text{ V}$, $R_{LOAD} = 1 \text{ k}\Omega$ for all ranges except $0 \text{ V to } 16 \text{ V}$ and $0 \text{ V to } 20 \text{ V}$ for which $R_{LOAD} = 2 \text{ k}\Omega$, $C_{LOAD} = 200 \text{ pF}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter ²	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE³					
Output Voltage Settling Time	9	12.5		μs	20 V step to 1 LSB at 16-bit resolution
	7.5	8.5		μs	10 V step to 1 LSB at 16-bit resolution
			5	μs	512 LSB step to 1 LSB at 16-bit resolution
Digital-to-Analog Glitch Impulse	8			nV-sec	$\pm 10 \text{ V range}$
	1			nV-sec	$0 \text{ V to } 5 \text{ V range}$
Glitch Impulse Peak Amplitude	15			mV	$\pm 10 \text{ V range}$
	10			mV	$0 \text{ V to } 5 \text{ V range}$
Power-On Glitch	100			mV p-p	
Digital Feedthrough	0.6			nV-sec	
Output Noise					
0.1 Hz to 10 Hz Bandwidth	15			$\mu\text{V p-p}$	
100 kHz Bandwidth	45			$\mu\text{V rms}$	$0 \text{ V to } 20 \text{ V}$ and $0 \text{ V to } 16 \text{ V}$ ranges, 2.5 V external reference
	35			$\mu\text{V rms}$	$0 \text{ V to } 10 \text{ V}$, $\pm 10 \text{ V}$, and $-2.5 \text{ V to } +7.5 \text{ V}$ ranges, 2.5 V external reference
	25			$\mu\text{V rms}$	$\pm 5 \text{ V range}$, 2.5 V external reference
	15			$\mu\text{V rms}$	$0 \text{ V to } 5 \text{ V}$ and $\pm 3 \text{ V}$ ranges, 2.5 V external reference
Output Noise Spectral Density, at 10 kHz	80			nV/ $\sqrt{\text{Hz}}$	$\pm 10 \text{ V range}$, 2.5 V external reference
	35			nV/ $\sqrt{\text{Hz}}$	$\pm 3 \text{ V range}$, 2.5 V external reference
	70			nV/ $\sqrt{\text{Hz}}$	$\pm 5 \text{ V}$, $0 \text{ V to } 10 \text{ V}$, and $-2.5 \text{ V to } +7.5 \text{ V}$ ranges, 2.5 V external reference
	110			nV/ $\sqrt{\text{Hz}}$	$0 \text{ V to } 20 \text{ V range}$, 2.5 V external reference
	90			nV/ $\sqrt{\text{Hz}}$	$0 \text{ V to } 16 \text{ V range}$, 2.5 V external reference
	45			nV/ $\sqrt{\text{Hz}}$	$0 \text{ V to } 5 \text{ V range}$, 2.5 V external reference
Total Harmonic Distortion (THD) ⁴	-87			dB	2.5 V external reference, 1 kHz tone
Signal-to-Noise Ratio (SNR)	92			dB	At ambient, 2.5 V external reference, BW = 20 kHz, $f_{OUT} = 1 \text{ kHz}$
Peak Harmonic or Spurious Noise (SFDR)	92			dB	At ambient, 2.5 V external reference, BW = 20 kHz, $f_{OUT} = 1 \text{ kHz}$
Signal-to-Noise-and-Distortion (SINAD) Ratio	85			dB	At ambient, 2.5 V external reference, BW = 20 kHz, $f_{OUT} = 1 \text{ kHz}$

¹ For specified performance, headroom requirement is 1 V.

² Temperature range: -40°C to $+125^\circ\text{C}$, typical at $+25^\circ\text{C}$.

³ Guaranteed by design and characterization, not production tested.

⁴ Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

$DV_{CC} = 1.7\text{ V to }5.5\text{ V}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN} , T_{MAX}	Unit	Description
t_1^1	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{\text{SYNC}}$ falling edge to $\overline{\text{SCLK}}$ falling edge setup time
t_5	10	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge time
t_6	20	ns min	Minimum $\overline{\text{SYNC}}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	10	ns min	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge
t_{10}	20	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge
t_{11}	20	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{12}	9	$\mu\text{s typ}$	DAC output settling time, 20 V step to 1 LSB at 16-bit resolution (see Table 2)
	7.5	$\mu\text{s typ}$	DAC output settling time, 10 V step to 1 LSB at 16-bit resolution
t_{13}	20	ns min	$\overline{\text{CLEAR}}$ pulse width low
t_{14}	200	ns typ	$\overline{\text{CLEAR}}$ pulse activation time
t_{15}	10	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK falling edge
t_{16}	40	ns max	SCLK rising edge to SDO valid ($C_{L_SDO}^2 = 15\text{ pF}$)
t_{17}	50	ns min	Minimum $\overline{\text{SYNC}}$ high time (readback/daisy-chain mode)

¹ Maximum SCLK frequency is 50 MHz for write mode and 33 MHz for readback mode.

² C_{L_SDO} is the capacitive load on the SDO output.

TIMING DIAGRAMS

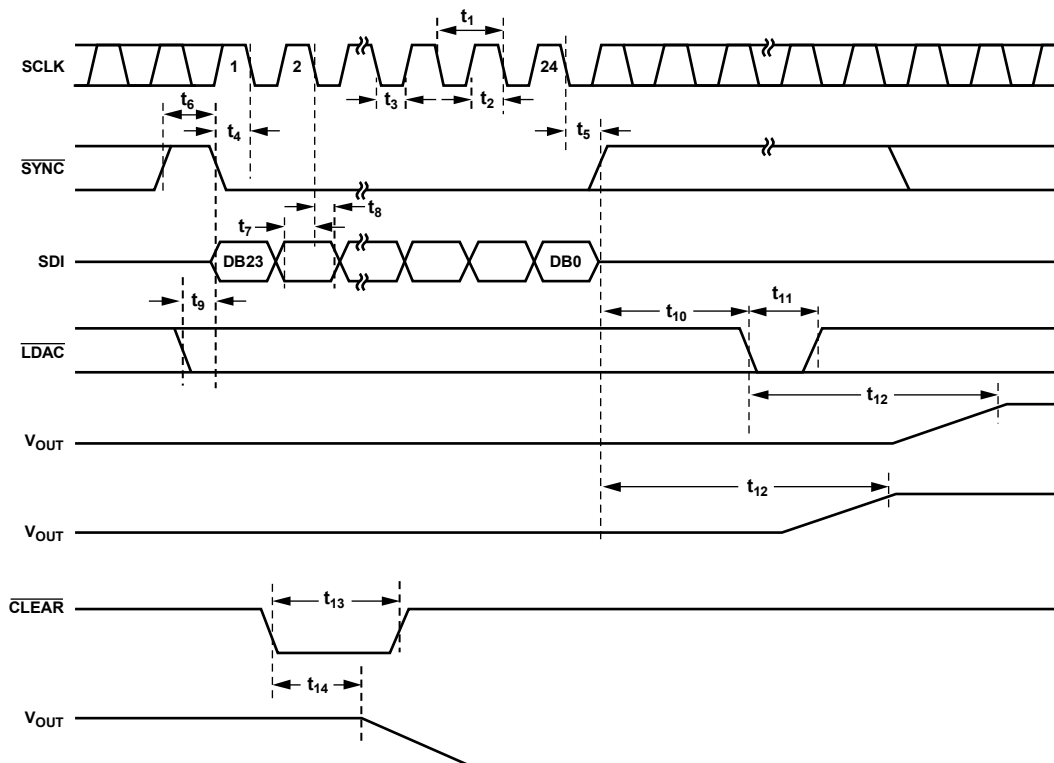


Figure 2. Serial Interface Timing Diagram

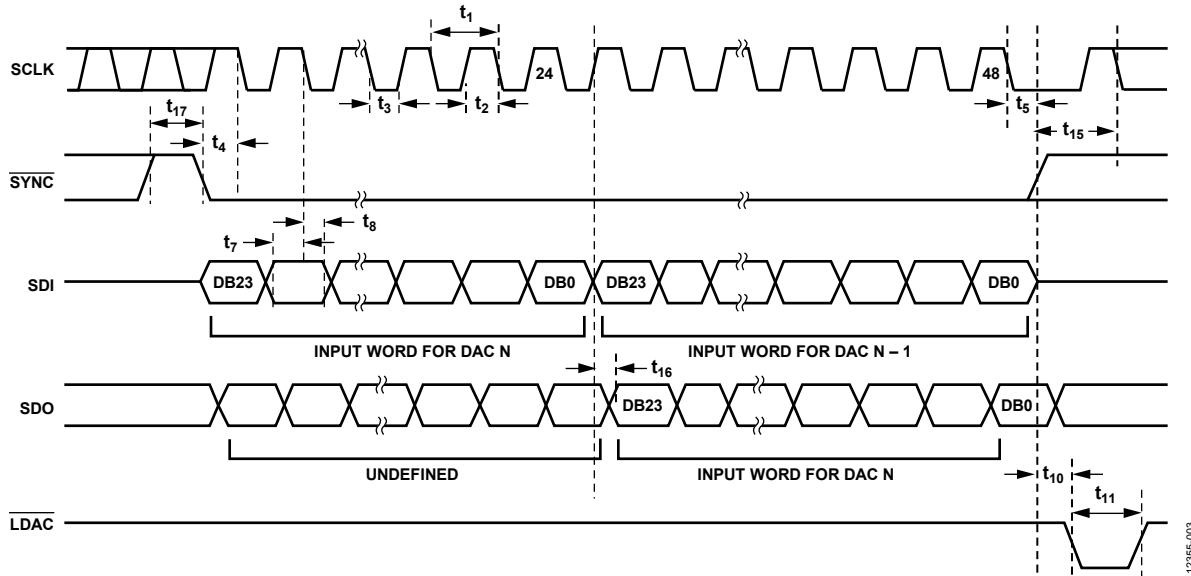


Figure 3. Daisy-Chain Timing Diagram

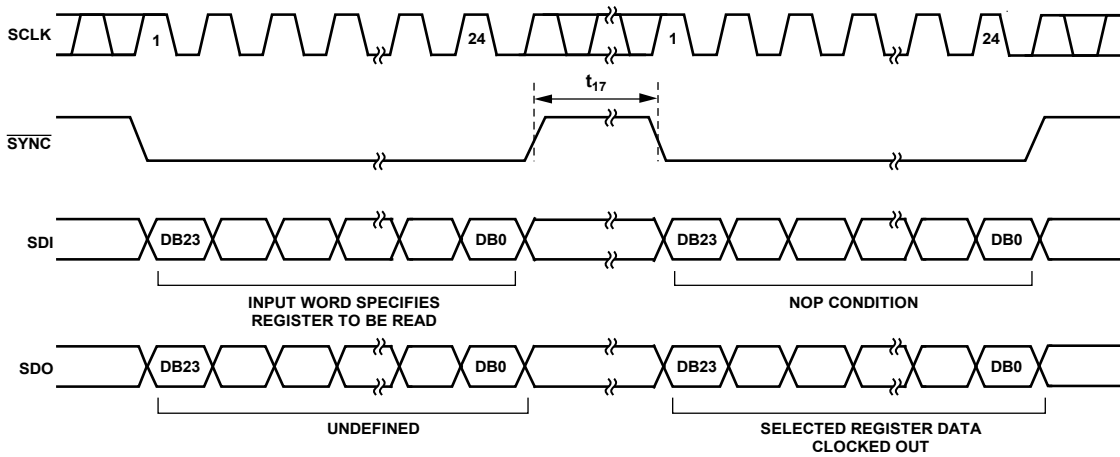


Figure 4. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. Transient currents of up to 200 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 4.

Parameter	Rating
V_{DD} to AGND	-0.3 V to +34 V
V_{SS} to AGND	+0.3 V to -17 V
V_{DD} to V_{SS}	-0.3 V to +34 V
DV_{CC} to DGND	-0.3 V to +7 V
Digital Inputs to DGND	-0.3 V to $DV_{CC} + 0.3$ V or 7 V (whichever is less)
Digital Outputs to DGND	-0.3 V to $DV_{CC} + 0.3$ V or 7 V (whichever is less)
V_{REFIN}/V_{REFOUT} to DGND	-0.3 V to +7 V
V_{OUT} to AGND	V_{SS} to V_{DD}
AGND to DGND	-0.3 V to +0.3 V
Operating Temperature Range, T_A Industrial	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature, $T_{J\text{MAX}}$	150°C
16-Lead TSSOP Package	
θ_{JA} Thermal Impedance	113°C/W ¹
θ_{JC} Thermal Impedance	28°C/W
16-Lead LFCSP Package	
θ_{JA} Thermal Impedance	75°C/W ¹
θ_{JC} Thermal Impedance	4.5°C/W ²
Power Dissipation	$(T_{J\text{MAX}} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD (Human Body Model)	4 kV

¹ JEDEC 2S2P test board, still air (0 m/sec airflow).

² Measured to exposed paddle, with infinite heat sink on package top surface.

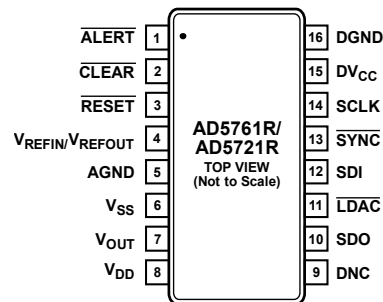
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES

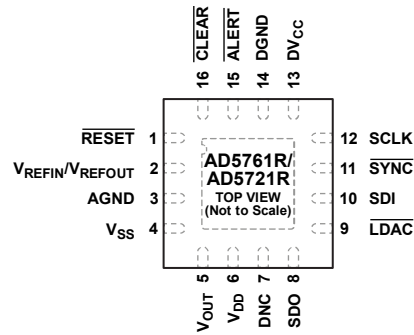
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

12385-008

Figure 5. 16-Lead TSSOP Pin Configuration

Table 5. 16-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{ALERT}}$	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset, for which a write to the control register asserts the pin high.
2	$\overline{\text{CLEAR}}$	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
3	$\overline{\text{RESET}}$	Active Low Reset Input. Asserting this pin returns the AD5761R/AD5721R to their default power-on status where the output is clamped to ground and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
4	$V_{\text{REFIN}}/V_{\text{REFOUT}}$	Internal Reference Voltage Output and External Reference Voltage Input. For specified performance, $V_{\text{REFIN}}/V_{\text{REFOUT}} = 2.5 \text{ V}$. Connect a 10 nF capacitor with the internal reference to minimize the noise.
5	AGND	Ground Reference Pin for Analog Circuitry.
6	V_{SS}	Negative Analog Supply Connection. A voltage in the range of -16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V . V_{SS} must be decoupled to AGND.
7	V_{OUT}	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a $2 \text{ k}\Omega$, 1 nF load.
8	V_{DD}	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V . V_{DD} must be decoupled to AGND.
9	DNC	Do Not Connect. Do not connect to this pin.
10	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
11	$\overline{\text{LDAC}}$	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If $\overline{\text{LDAC}}$ is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of $\overline{\text{LDAC}}$. This pin can be left floating because there is an internal pull-up resistor.
12	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
13	$\overline{\text{SYNC}}$	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While $\overline{\text{SYNC}}$ is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of $\overline{\text{SYNC}}$.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
15	DV _{CC}	Digital Supply. The voltage range is from 1.7 V to 5.5 V . The applied voltage sets the voltage at which the digital interface operates.
16	DGND	Digital Ground.



NOTES

1. DNC = DO NOT CONNECT.
2. THE EXPOSED PAD MUST BE MECHANICALLY CONNECTED TO THE PCB COPPER PLANE FOR OPTIMAL THERMAL PERFORMANCE. THE EXPOSED PAD CAN BE LEFT ELECTRICALLY FLOATING.

12335-106

Figure 6. 16-Lead LFCSP Pin Configuration

Table 6. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RESET	Active Low Reset Input. Asserting this pin returns the AD5761R/AD5721R to their default power-on status where the output is clamped to ground and the output buffer is powered down. This pin can be left floating because there is an internal pull-up resistor.
2	VREFIN/VREFOUT	Internal Reference Voltage Output and External Reference Voltage Input. For specified performance, $V_{REFIN}/V_{REFOUT} = 2.5$ V. Connect a 10 nF capacitor with the internal reference to minimize the noise.
3	AGND	Ground Reference Pin for Analog Circuitry.
4	VSS	Negative Analog Supply Connection. A voltage in the range of -16.5 V to 0 V can be connected to this pin. For unipolar output ranges, connect this pin to 0 V. V_{SS} must be decoupled to AGND.
5	VOUT	Analog Output Voltage of the DAC. The output amplifier is capable of directly driving a 2 k Ω , 1 nF load.
6	VDD	Positive Analog Supply Connection. A voltage in the range of 4.75 V to 30 V can be connected to this pin for unipolar output ranges. Bipolar output ranges accept a voltage in the range of 4.75 V to 16.5 V. V_{DD} must be decoupled to AGND.
7	DNC	Do Not Connect. Do not connect to this pin.
8	SDO	Serial Data Output. This pin clocks data from the serial register in daisy-chain or readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
9	LDAC	Load DAC. This logic input updates the DAC register and, consequently, the analog output. When tied permanently low, the DAC register is updated when the input register is updated. If LDAC is held high during the write to the input register, the DAC output register is not updated, and the DAC output update is held off until the falling edge of LDAC. This pin can be left floating because there is an internal pull-up resistor.
10	SDI	Serial Data Input. Data must be valid on the falling edge of SCLK.
11	SYNC	Active Low Synchronization Input. This pin is the frame synchronization signal for the serial interface. While SYNC is low, data is transferred in on the falling edge of SCLK. Data is latched on the rising edge of SYNC.
12	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds of up to 50 MHz.
13	DVCC	Digital Supply. The voltage range is from 1.7 V to 5.5 V. The applied voltage sets the voltage at which the digital interface operates.
14	DGND	Digital Ground.
15	ALERT	Active Low Alert. This pin is asserted low when the die temperature exceeds approximately 150°C, or when an output short circuit or a brownout occurs. This pin is also asserted low during power-up, a full software reset, or a hardware reset, for which a write to the control register asserts the pin high.
16	CLEAR	Falling Edge Clear Input. Asserting this pin sets the DAC register to zero scale, midscale, or full-scale code (user selectable) and updates the DAC output. This pin can be left floating because there is an internal pull-up resistor.
	EPAD	Exposed Pad. The exposed pad must be mechanically connected to the PCB copper plane for optimal thermal performance. The exposed pad can be left electrically floating.

TYPICAL PERFORMANCE CHARACTERISTICS

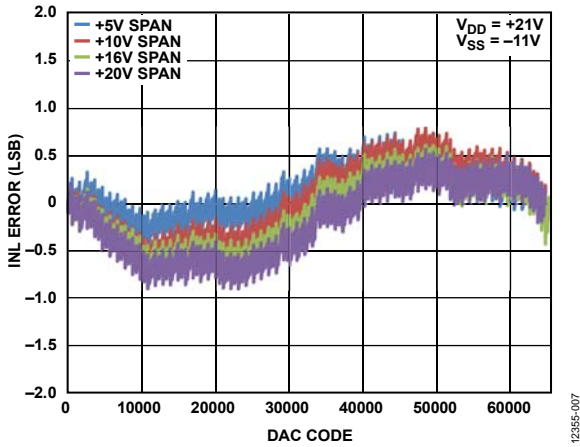


Figure 7. AD5761R INL Error vs. DAC Code, Unipolar Output

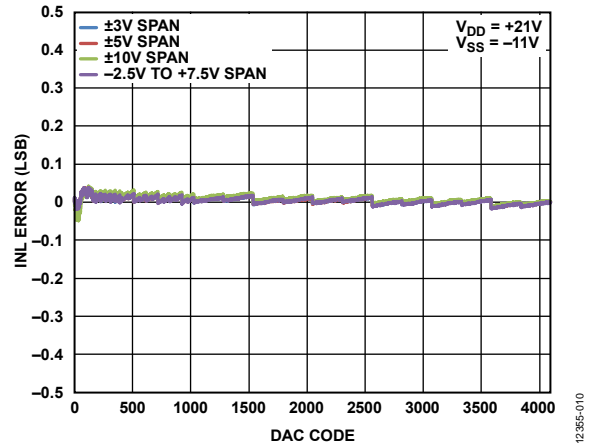


Figure 10. AD5721R INL Error vs. DAC Code, Bipolar Output

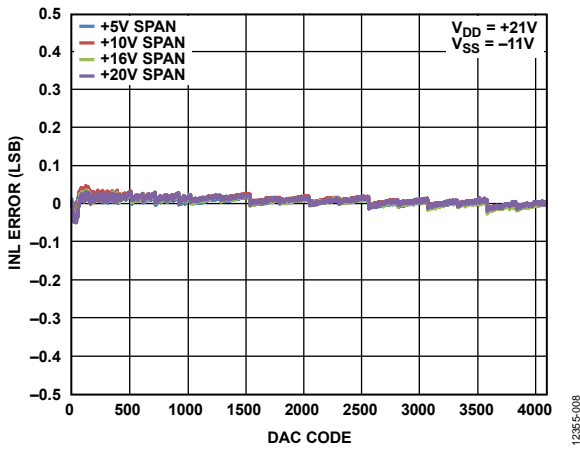


Figure 8. AD5721R INL Error vs. DAC Code, Unipolar Output

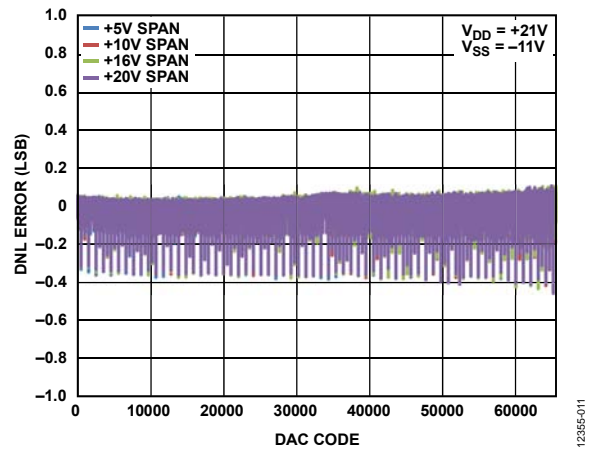


Figure 11. AD5761R DNL Error vs. DAC Code, Unipolar Output

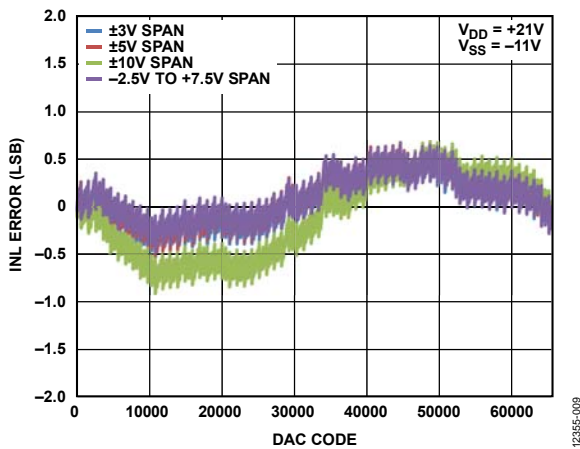


Figure 9. AD5761R INL Error vs. DAC Code, Bipolar Output

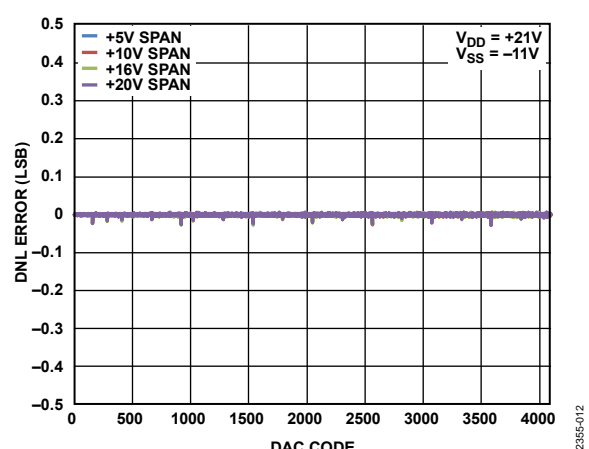


Figure 12. AD5721R DNL Error vs. DAC Code, Unipolar Output

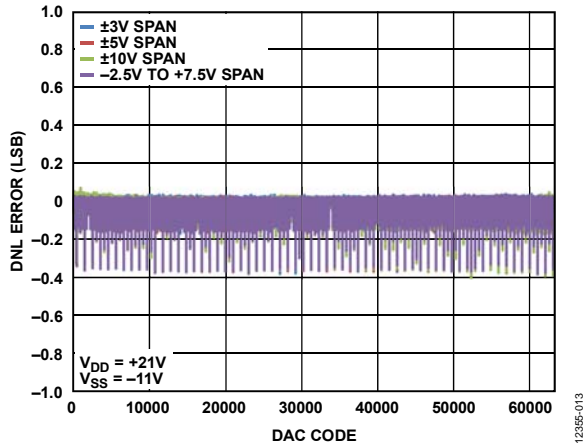


Figure 13. AD5761R DNL Error vs. DAC Code, Bipolar Output

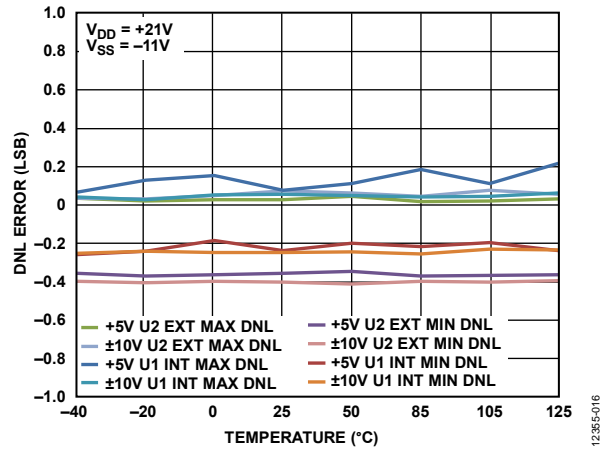


Figure 16. DNL Error vs. Temperature

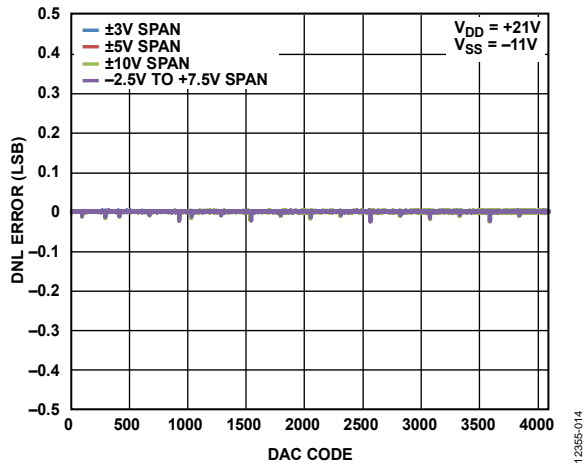


Figure 14. AD5721R DNL Error vs. DAC Code, Bipolar Output

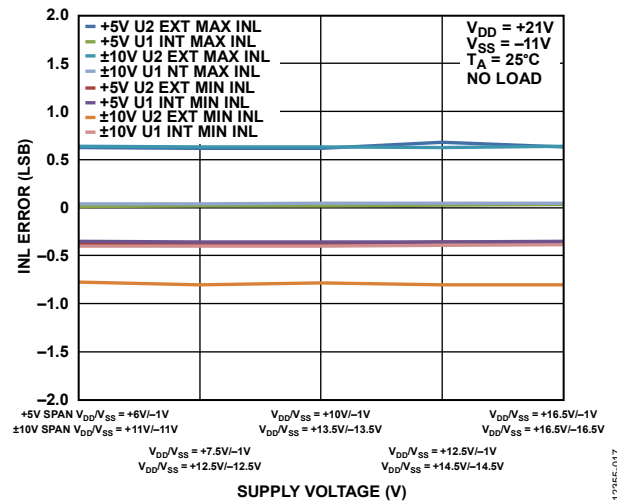


Figure 17. INL Error vs. Supply Voltage

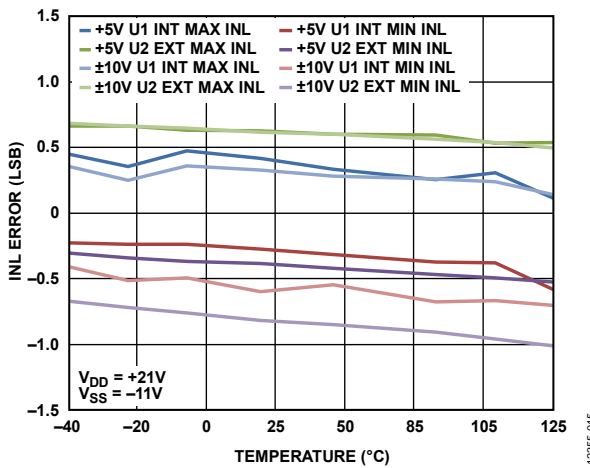


Figure 15. INL Error vs. Temperature

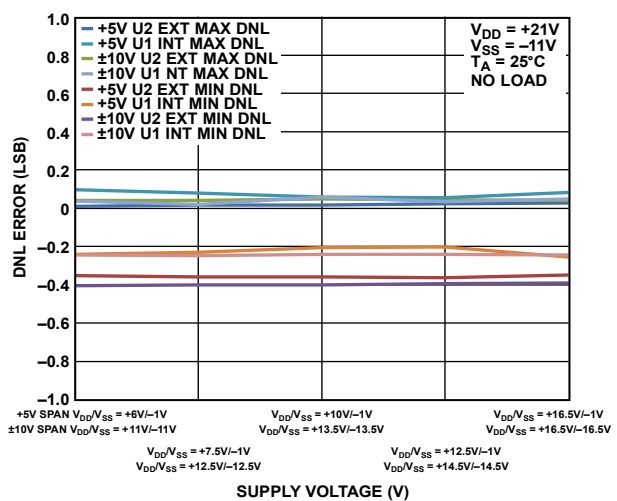


Figure 18. DNL Error vs. Supply Voltage

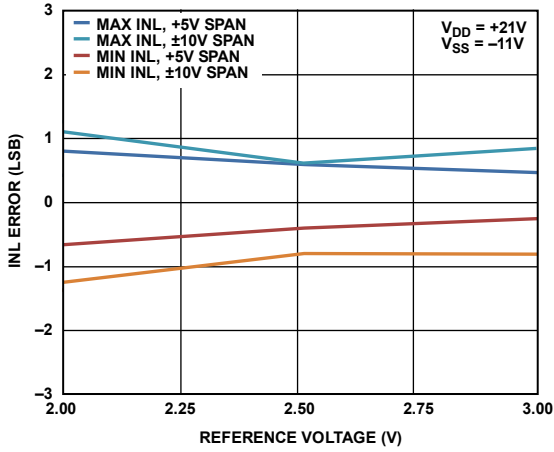


Figure 19. INL Error vs. Reference Voltage

12355-019

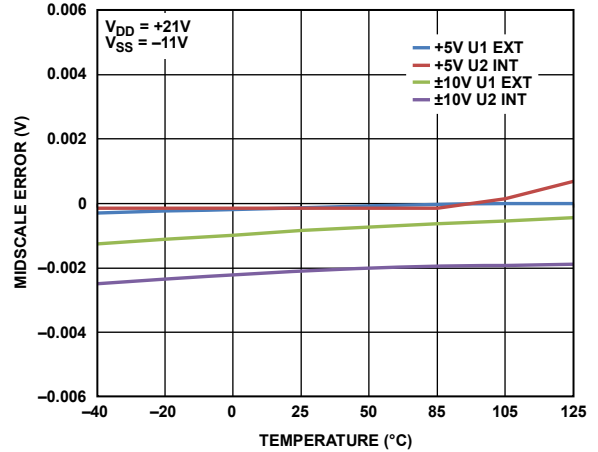


Figure 22. Midscale Error vs. Temperature

12355-022

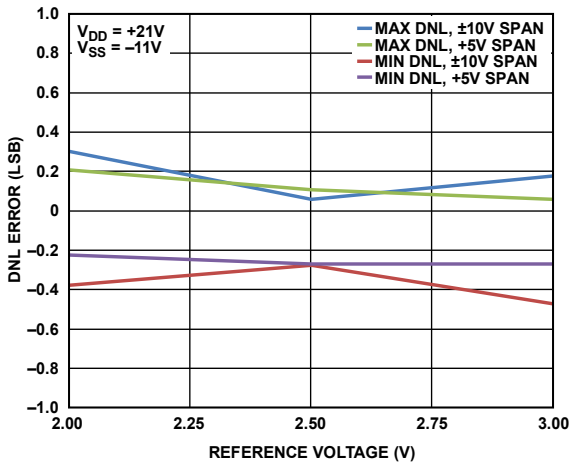


Figure 20. DNL Error vs. Reference Voltage

12355-020

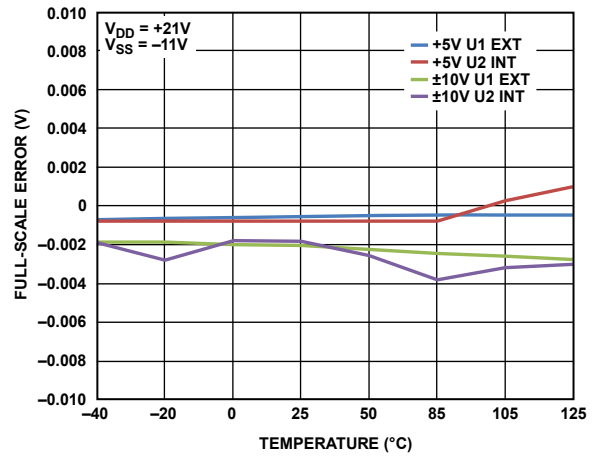


Figure 23. Full-Scale Error vs. Temperature

12355-023

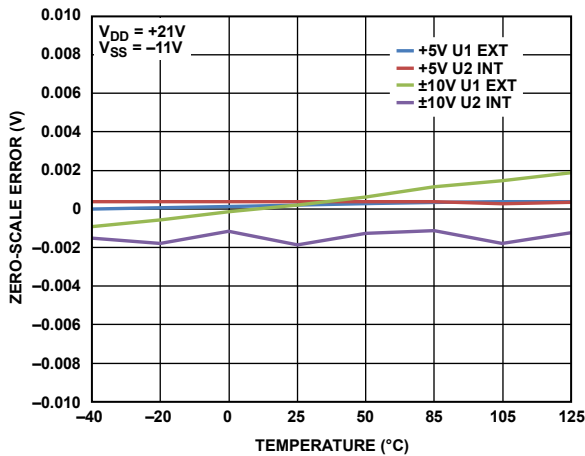


Figure 21. Zero-Scale Error vs. Temperature

12355-021

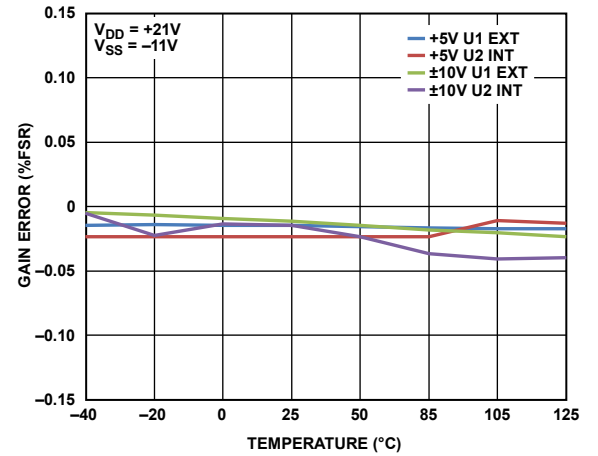


Figure 24. Gain Error vs. Temperature

12355-024

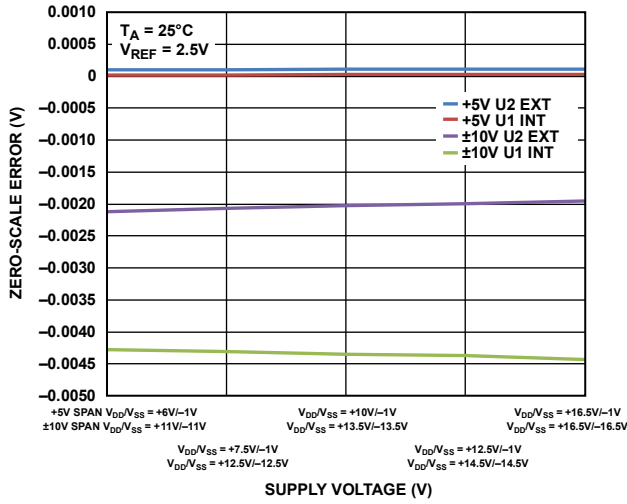


Figure 25. Zero-Scale Error vs. Supply Voltage

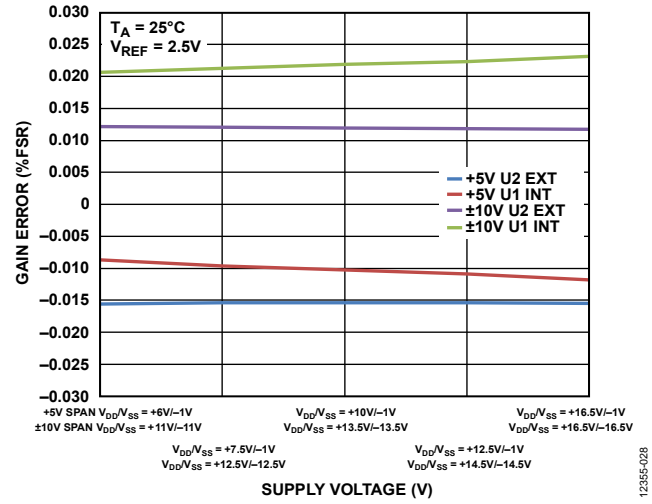


Figure 28. Gain Error vs. Supply Voltage

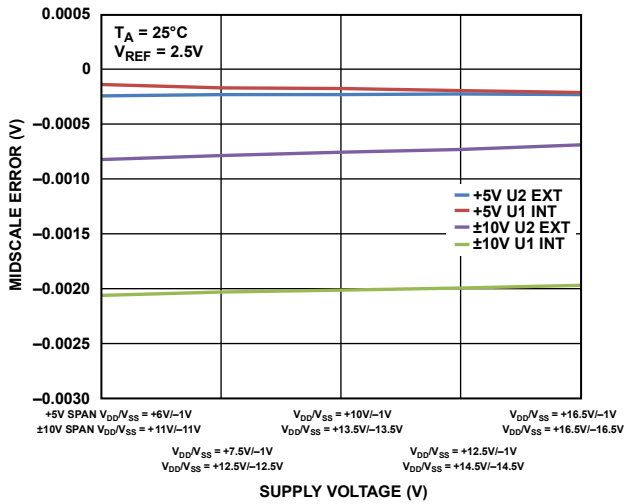


Figure 26. Midscale Error vs. Supply Voltage

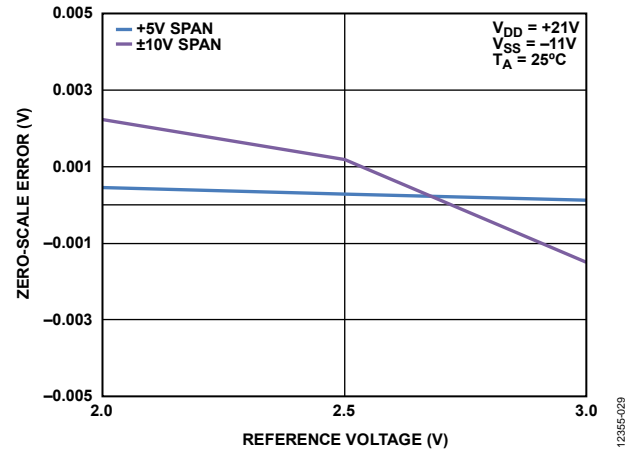


Figure 29. Zero-Scale Error vs. Reference Voltage

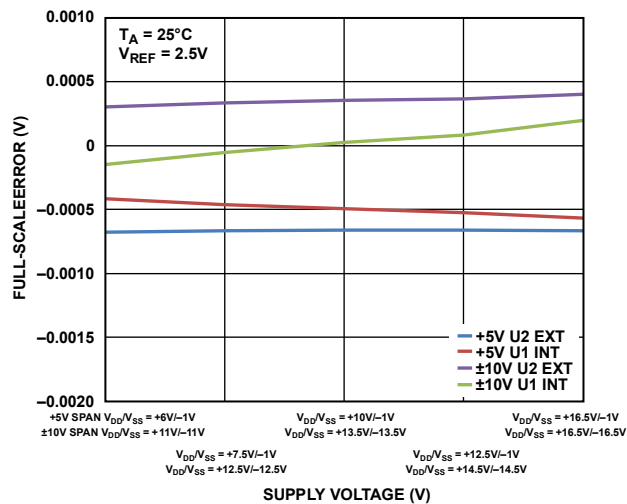


Figure 27. Full-Scale Error vs. Supply Voltage

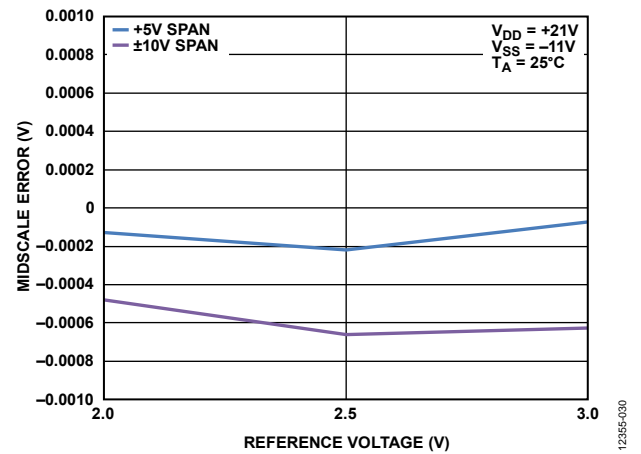


Figure 30. Midscale Error vs. Reference Voltage

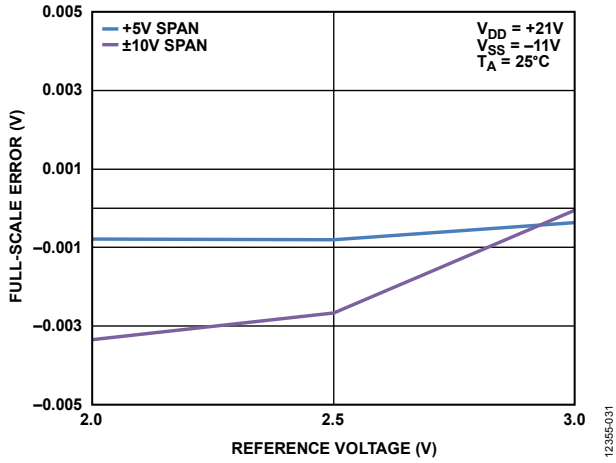


Figure 31. Full-Scale Error vs. Reference Voltage

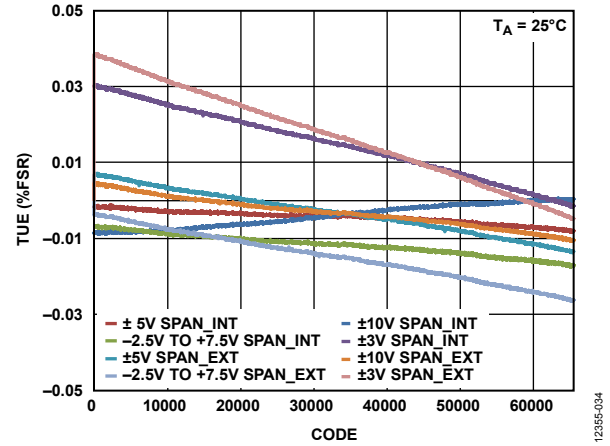


Figure 34. TUE vs. Code, Bipolar Output

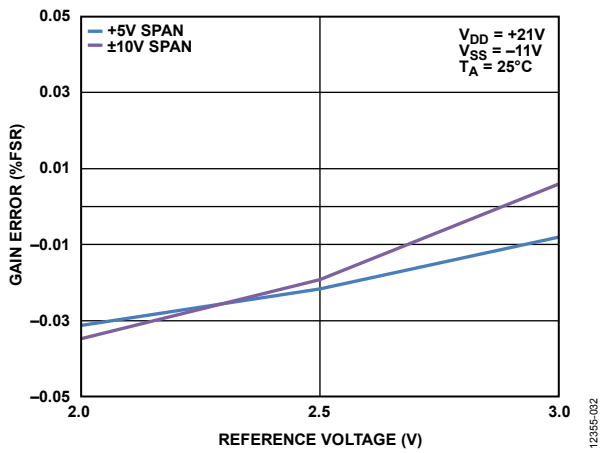


Figure 32. Gain Error vs. Reference Voltage

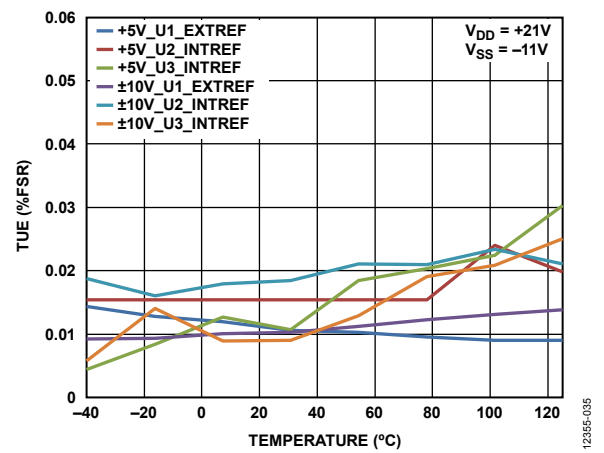


Figure 35. TUE vs. Temperature

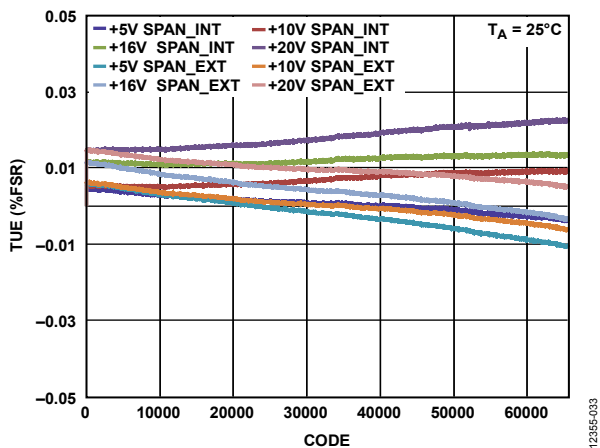


Figure 33. TUE vs. Code, Unipolar Output

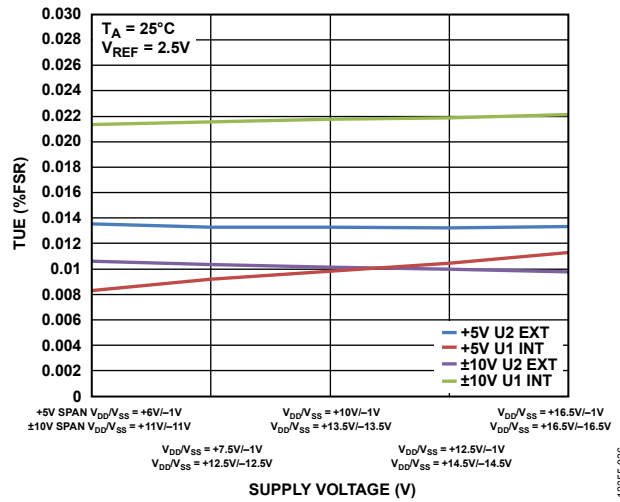


Figure 36. TUE vs. Supply Voltage

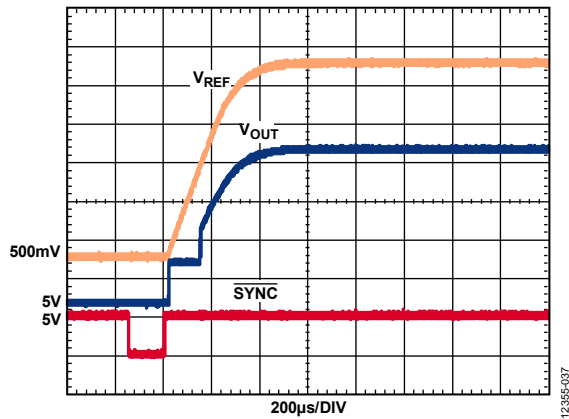


Figure 37. Reference Output Voltage Turn On Transient

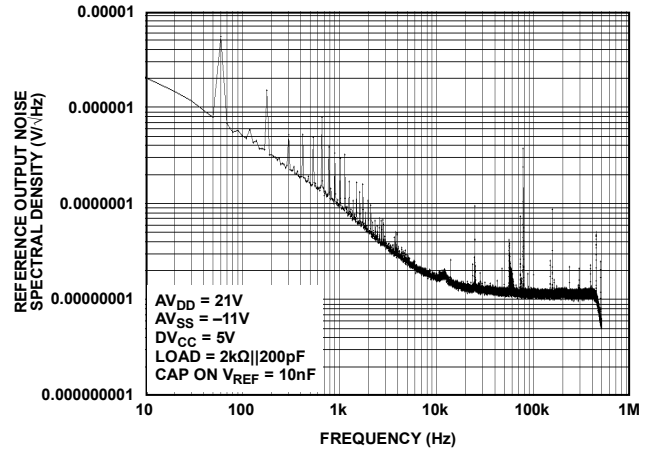


Figure 40. Reference Output Noise Spectral Density vs. Frequency

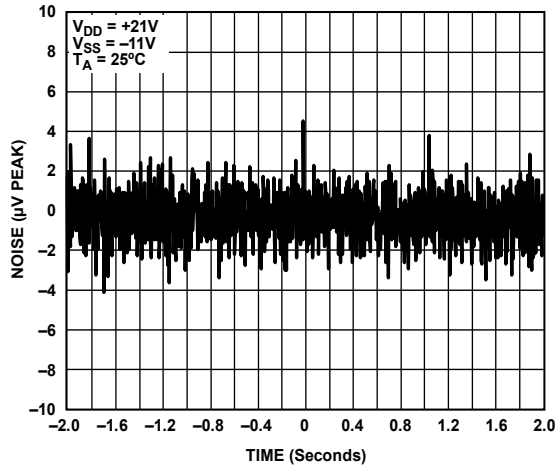


Figure 38. Internal Reference Noise (100 kHz Bandwidth)

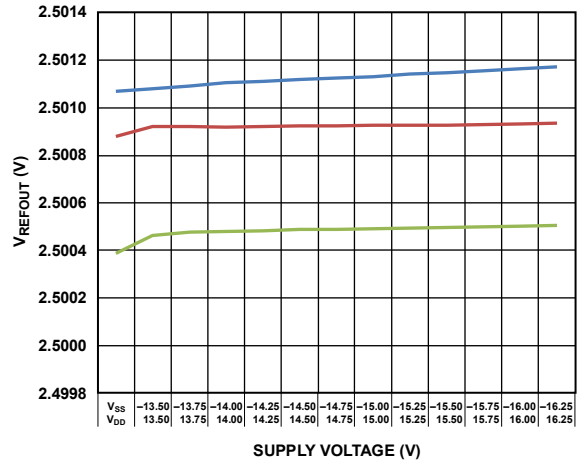


Figure 41. Reference Output Voltage (V_{REFOUT}) vs. Supply Voltage

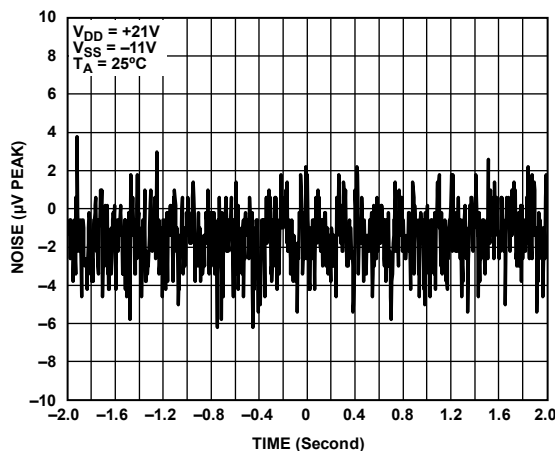


Figure 39. Internal Reference Noise (0.1 Hz to 10 Hz Bandwidth)

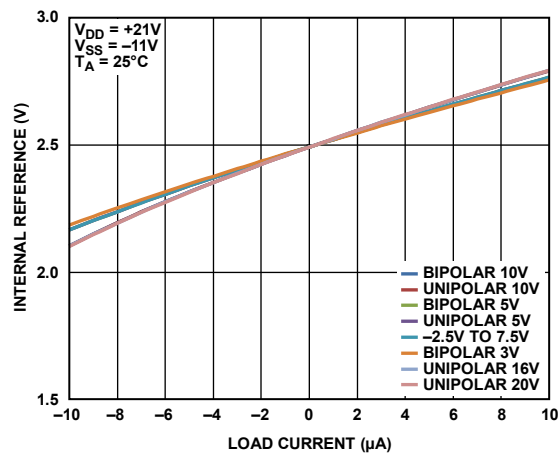


Figure 42. Internal Reference vs. Load Current

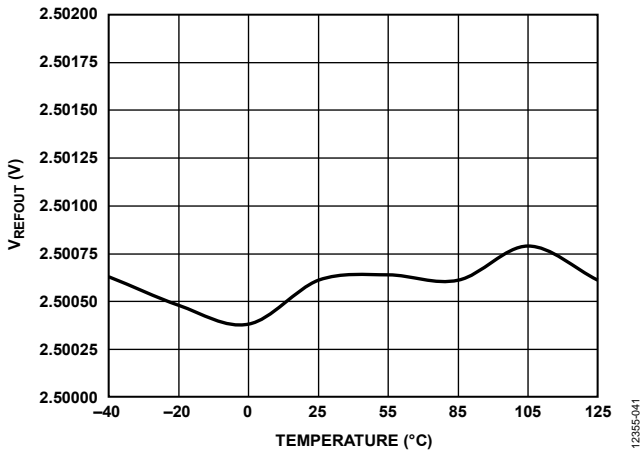


Figure 43. Reference Output Voltage vs. Temperature

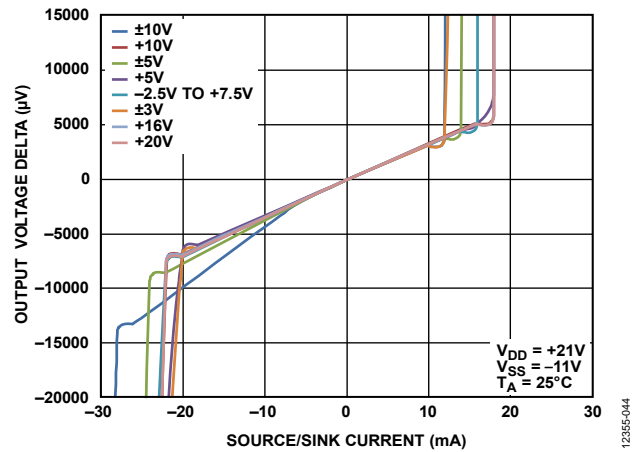


Figure 46. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded

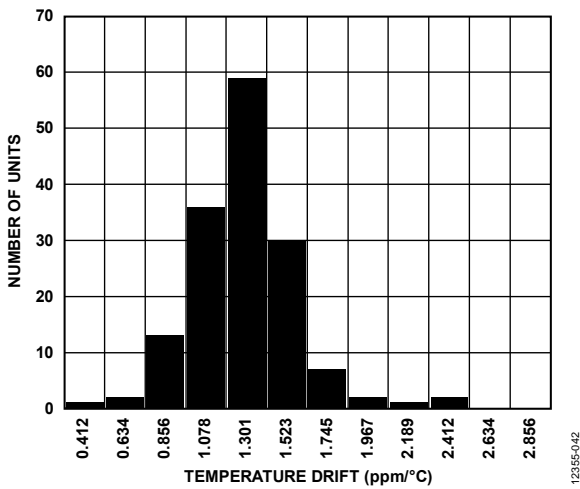


Figure 44. Reference Output TC

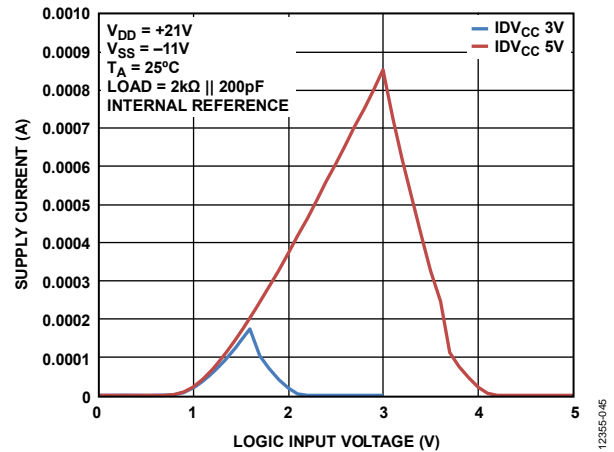


Figure 47. Supply Current vs. Logic Input Voltage

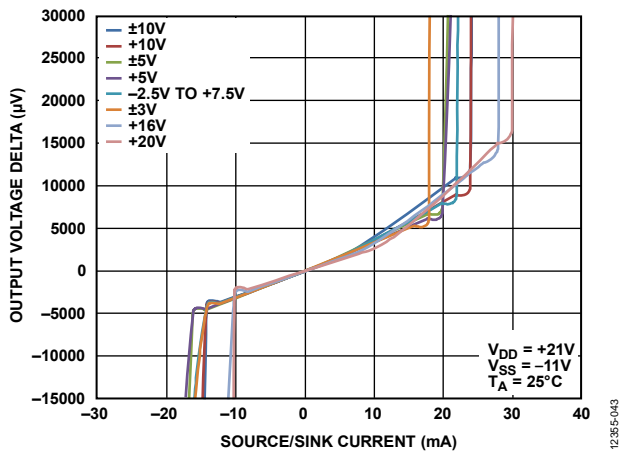


Figure 45. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded

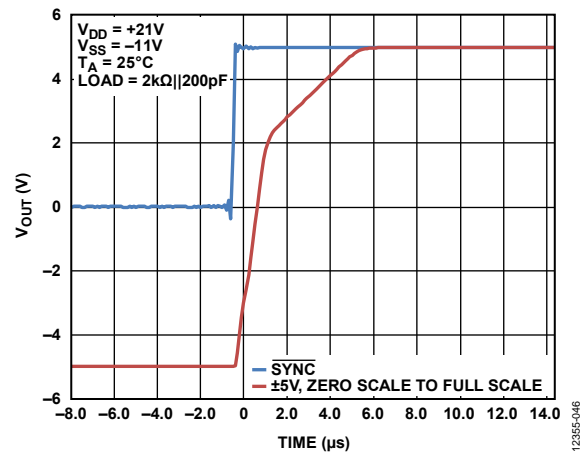


Figure 48. Full-Scale Settling Time (Rising Voltage Step), ±5 V Range

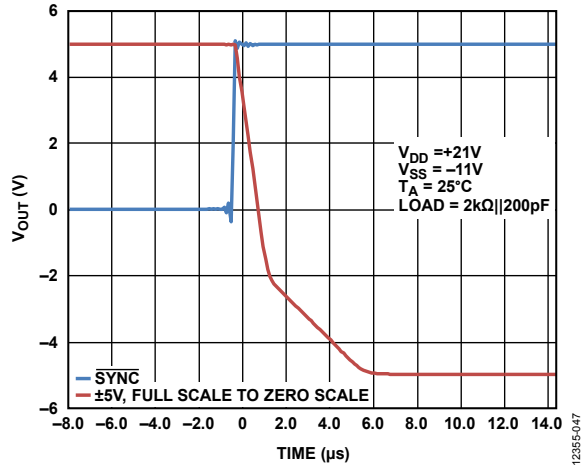


Figure 49. Full-Scale Settling Time (Falling Voltage Step), ±5 V Range

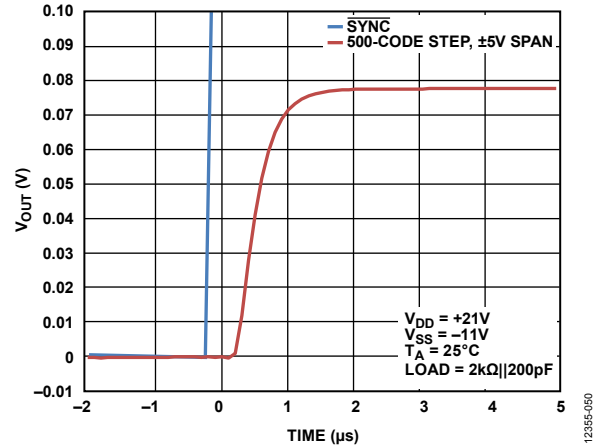


Figure 52. 500-Code Step Settling Time, ±5 V Range

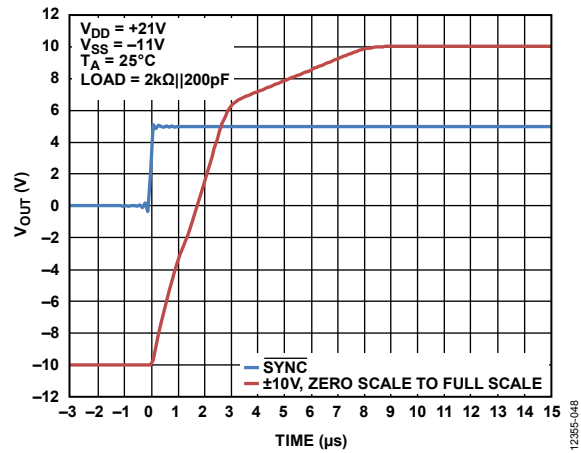


Figure 50. Full-Scale Settling Time (Rising Voltage Step), ±10 V Range

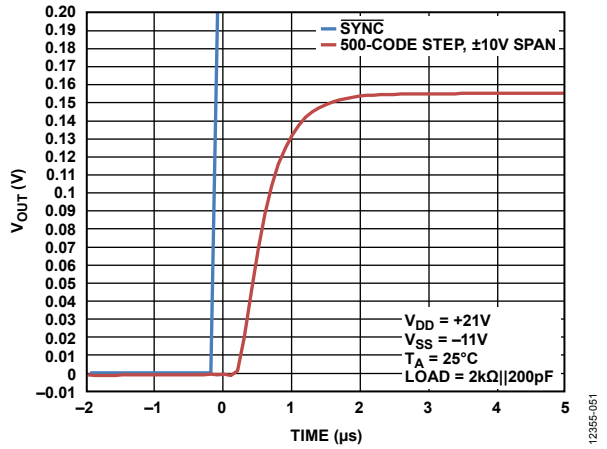


Figure 53. 500-Code Step Settling Time, ±10 V Range

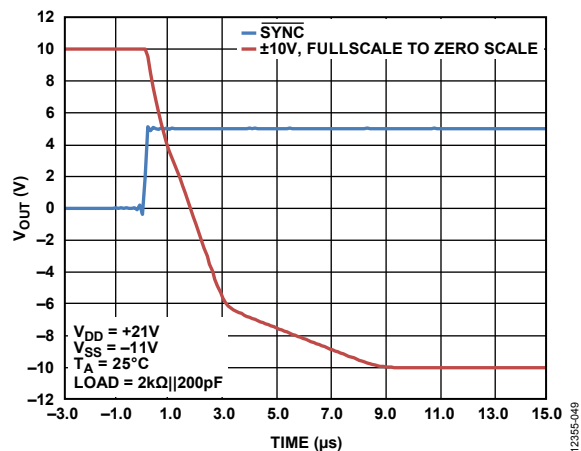


Figure 51. Full-Scale Settling Time (Falling Voltage Step), ±10 V Range

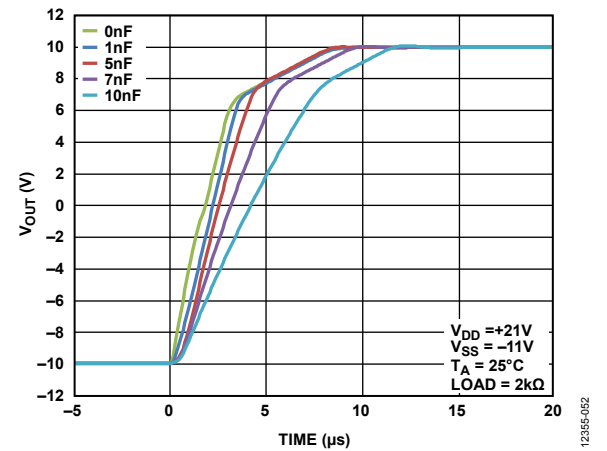


Figure 54. Full-Scale Settling Time at Various Capacitive Loads, ±10 V Range

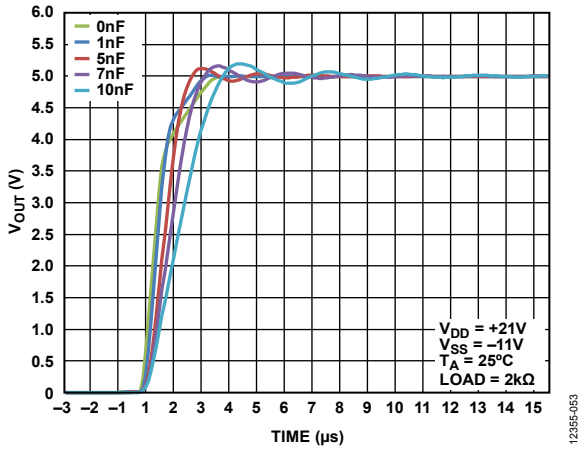


Figure 55. Full-Scale Settling Time at Various Capacitive Loads, 0 V to 5 V Range

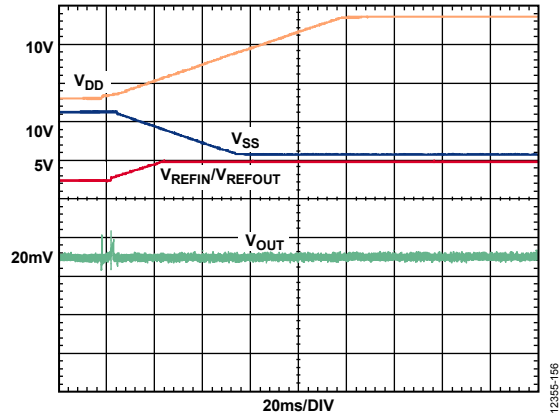


Figure 58. Power-Up Glitch

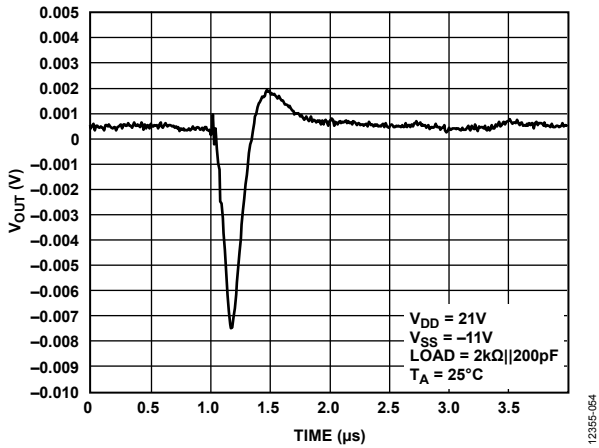


Figure 56. Digital-to-Analog Glitch Energy, 5 V Range

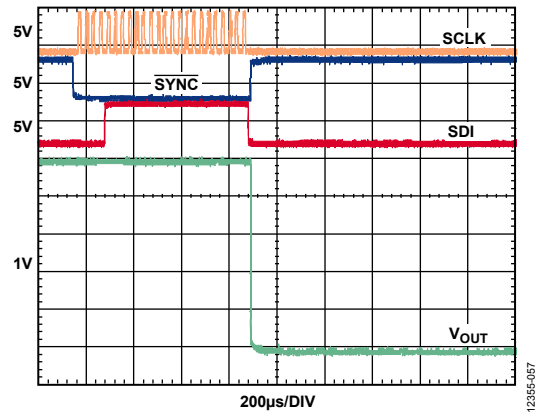


Figure 59. Software Full Reset Glitch from Full Scale with Output Loaded, 0 V to 5 V Range

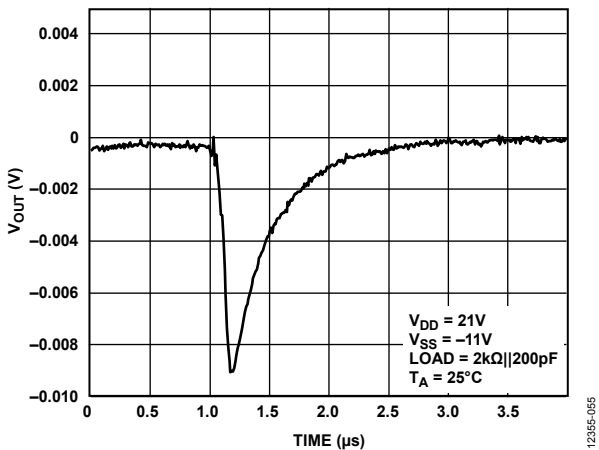


Figure 57. Digital-to-Analog Glitch Energy, ±10 V Range

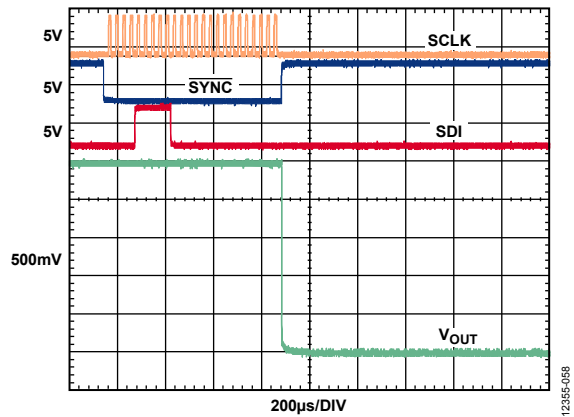


Figure 60. Software Full Reset Glitch from Midscale with Output Loaded, 5 V Range

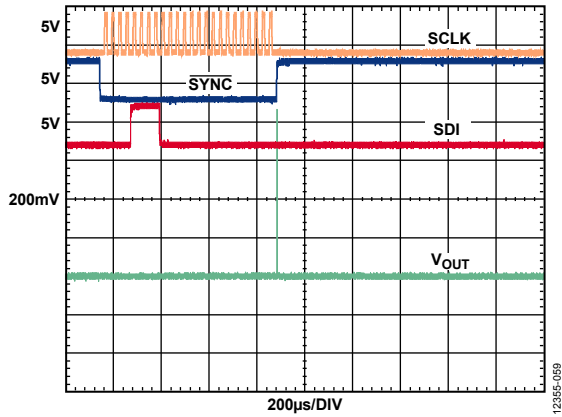


Figure 61. Software Full Reset Glitch from Zero Scale with Output Loaded, 0 V to 5 V Range

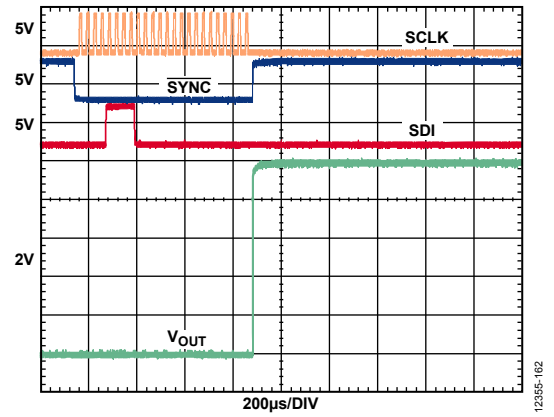


Figure 64. Software Full Reset Glitch from Zero Scale with Output Loaded, ±10 V Range

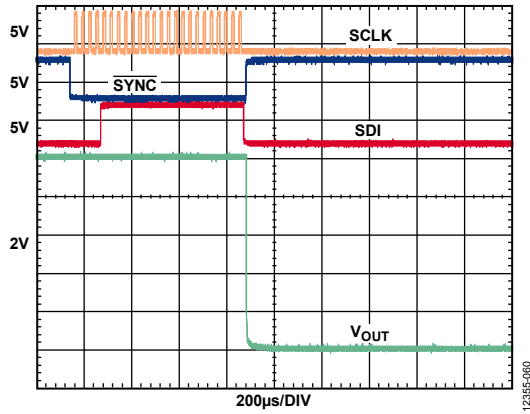


Figure 62. Software Full Reset Glitch from Full Scale with Output Loaded, ±10 V Range

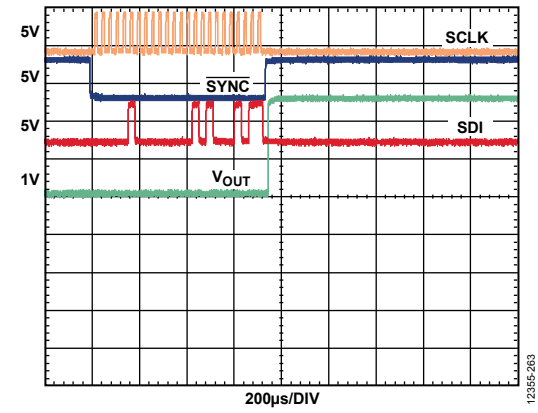


Figure 65. Output Range Change Glitch, 0 V to 5 V Range

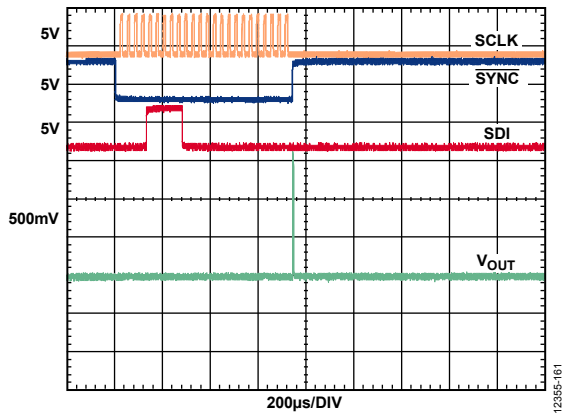


Figure 63. Software Full Reset Glitch from Midscale with Output Loaded, ±10 V Range

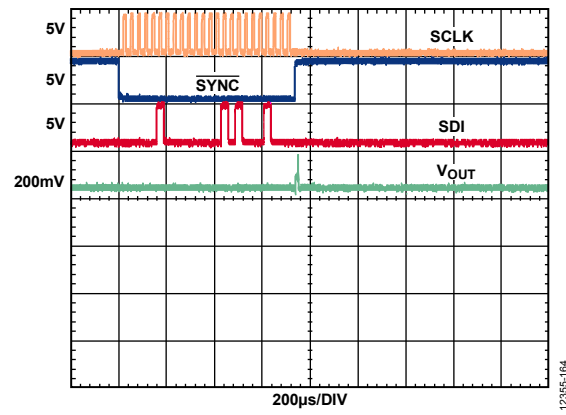


Figure 66. Output Range Change Glitch, ±10 V Range

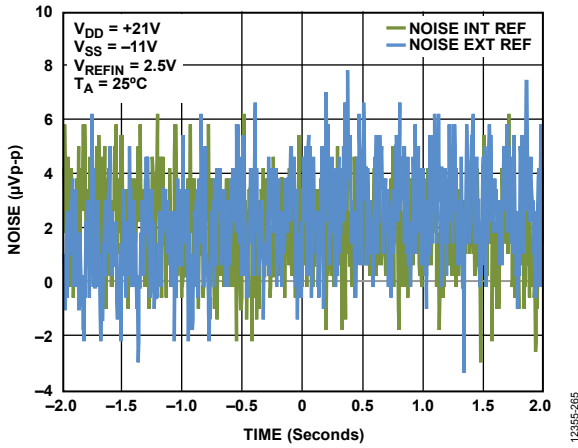


Figure 67. Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth

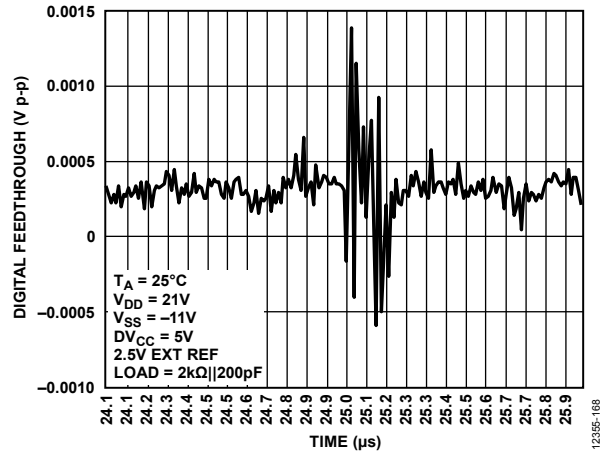


Figure 70. Digital Feedthrough

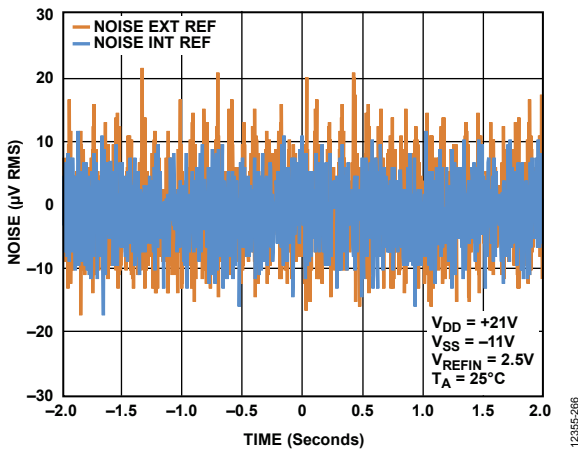


Figure 68. Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth

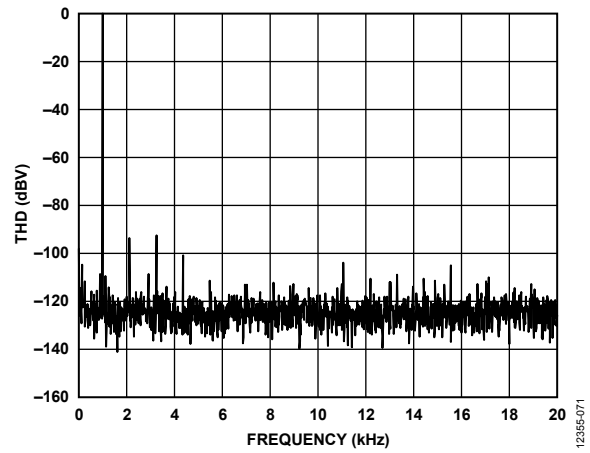


Figure 71. Total Harmonic Distortion

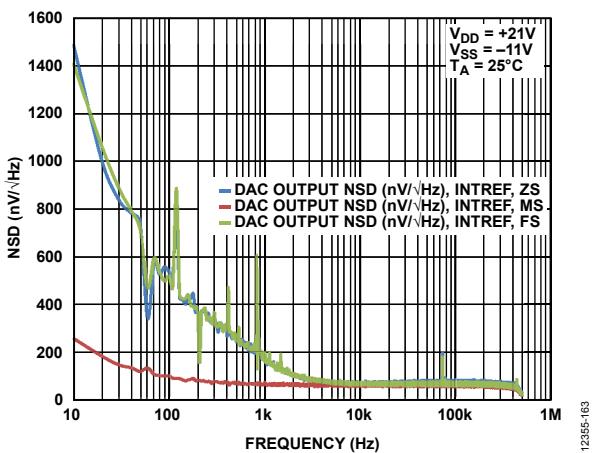


Figure 69. DAC Output Noise Spectral Density (NSD) vs. Frequency, ±10 V Range

TERMINOLOGY

Total Unadjusted Error (TUE)

Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. A typical INL error vs. DAC code plot is shown in Figure 7.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. The AD5761R/AD5721R are guaranteed monotonic. A typical DNL error vs. code plot is shown in Figure 11.

Monotonicity

A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5761R/AD5721R are monotonic over their full operating temperature range.

Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding) for the AD5761R/AD5721R.

Bipolar Zero Temperature Coefficient (TC)

Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage is negative full scale. A plot of zero-scale error vs. temperature is shown in Figure 21.

Zero-Scale Error Temperature Coefficient (TC)

Zero-scale error TC is a measure of the change in zero-scale error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function.

Offset Error Temperature Coefficient (TC)

Offset error TC is a measurement of the change in offset error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature is shown in Figure 24.

Gain Error Temperature Coefficient (TC)

Gain error TC is a measure of the change in gain error with changes in temperature. It is expressed in ppm FSR/ $^\circ\text{C}$.

DC Power Supply Rejection Ratio (DC PSRR)

DC power supply rejection ratio is a measure of the rejection of the output voltage to dc changes in the power supplies applied to the DAC. It is measured for a given dc change in power supply voltage and is expressed in mV/V.

AC Power Supply Rejection Ratio (AC PSRR)

AC power supply rejection ratio is a measure of the rejection of the output voltage to ac changes in the power supplies applied to the DAC. It is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. Full-scale settling time is shown in Figure 48 to Figure 51.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (see Figure 56 and Figure 57).

Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Noise Spectral Density (NSD)

Noise spectral density is a measurement of the internally generated random noise characterized as a spectral density ($\text{nV}/\sqrt{\text{Hz}}$). It is measured by loading the DAC to full scale and measuring noise at the output. It is measured in $\text{nV}/\sqrt{\text{Hz}}$. A plot of noise spectral density is shown in Figure 69.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C as follows:

$$TC = \left[\frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF_NOM} \times Temp\ Range} \right] \times 10^6$$

where:

V_{REF_MAX} is the maximum reference output measured over the total temperature range.

V_{REF_MIN} is the minimum reference output measured over the total temperature range.

V_{REF_NOM} is the nominal reference output voltage, 2.5 V.

Temp Range is the specified temperature range, -40°C to +125°C.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental.

For the AD5761R/AD5721R, it is defined as

$$THD (dB) = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

V_2 , V_3 , V_4 , V_5 , and V_6 are the rms amplitudes of the second through the sixth harmonics.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5761R/AD5721R are single channel, 16-/12-bit voltage output DACs. The AD5761R/AD5721R output ranges are software selectable and can be configured as follows:

- Unipolar output voltage: 0 V to 5 V, 0 V to 10 V, 0 V to 16 V, 0 V to 20 V
- Bipolar output voltage: -2.5 V to +7.5 V, ± 3 V, ± 5 V, ± 10 V

Data is written to the AD5761R/AD5721R in a 24-bit word format via a 4-wire, serial peripheral interface (SPI) compatible, digital interface. The devices also offer an SDO pin to facilitate daisy-chaining and readback.

TRANSFER FUNCTION

The internal reference is on by default. The input coding to the DAC can be straight binary or twos complement (bipolar ranges case only). Therefore, the transfer function is given by

$$V_{OUT} = V_{REF} \times \left[\left(M \times \frac{D}{2^N} \right) - C \right]$$

where:

V_{REF} is 2.5 V.

M is the slope for a given output range.

D is the decimal equivalent of the code loaded to the DAC register as follows:

0 to 4095 for the 12-bit device.

0 to 65,535 for the 16-bit device.

N is the number of bits. N is 12 for the AD5721R and 16 for the AD5761R.

C is the offset for a given output range.

The values for M and C are as shown in Table 7.

Table 7. M and C Values for Various Output Ranges

Range	M	C
± 10 V	8	4
± 5 V	4	2
± 3 V	2.4	1.2
-2.5 V to +7.5 V	4	1
0 V to 20 V	8	0
0 V to 16 V	6.4	0
0 V to 10 V	4	0
0 V to 5 V	2	0

DAC ARCHITECTURE

The DAC architecture consists of an R-2R DAC followed by an output buffer amplifier. Figure 72 shows a block diagram of the DAC architecture. Note that the reference input is buffered prior to being applied to the DAC. The AD5761R/AD5721R offer a 2.5 V, 5 ppm/°C maximum internal reference on chip.

The output voltage range obtained from the configurable output amplifier is selected by writing to the 3 LSBs (RA[2:0]) in the control register.

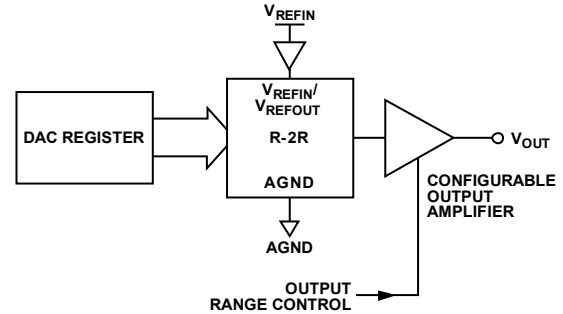


Figure 72. DAC Architecture

R-2R DAC

The architecture of the AD5761R consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 73. The 6 MSBs of the 16-bit data-word are decoded to drive 63 switches, E0 to E62, while the remaining 10 bits of the data-word drive the S0 to S9 switches of a 10-bit voltage mode R-2R ladder network.

The code loaded into the DAC register determines which arms of the ladder are switched between V_{REF} and ground (AGND). The output voltage is taken from the end of the ladder and amplified afterwards to provide the selected output voltage.

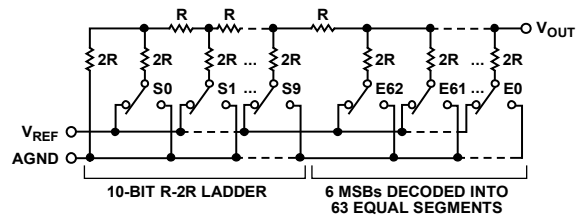


Figure 73. DAC Ladder Structure

Internal Reference

The AD5761R/AD5721R feature an on-chip reference. The on-chip reference is on at power-up, and this reference can be turned off by setting the software-programmable bit, DB5, in the control register. Table 12 shows how the state of the bit corresponds to the mode of operation.

The internal reference is available at the V_{REFIN}/V_{REFOUT} pin. A buffer is required if the reference output is used to drive external loads. Place a capacitor in the range of 1 nF to 100 nF between the reference output and DGND to improve the noise performance.

Reference Buffer

The AD5761R/AD5721R can operate with either an external or internal reference. The reference input has an input range of 2 V to 3 V with 2.5 V for specified performance. This input voltage is then buffered before it is applied to the DAC core.

DAC Output Amplifier

The output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 2 k Ω in parallel with 1 nF to AGND. The source and sink capabilities of the output amplifier are shown in Figure 45.

SERIAL INTERFACE

The AD5761R/AD5721R 4-wire digital interface ($\overline{\text{SYNC}}$, SCLK, SDI, and SDO) is SPI compatible. The write sequence begins after bringing the $\overline{\text{SYNC}}$ line low, and maintaining this line low until the complete data-word is loaded from the SDI pin. Data is loaded in at the SCLK falling edge transition (see Figure 2). When $\overline{\text{SYNC}}$ is brought high again, the serial data-word is decoded according to the instructions in Table 10. The AD5761R/AD5721R contain an SDO pin to allow the user to daisy-chain multiple devices together or to read back the contents of the registers.

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only when $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles.

In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. Exactly 24 falling clock edges must be applied to SCLK before $\overline{\text{SYNC}}$ is brought high again. If $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, the data written is invalid. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, the input data is also invalid.

The input shift register is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again. After the end of the serial data transfer, data is automatically transferred from the input shift register to the addressed register. When the write cycle is complete, the output can be updated by taking $\overline{\text{LDAC}}$ low while $\overline{\text{SYNC}}$ is high.

Readback Operation

The contents of the input, DAC, and control registers can be read back via the SDO pin. Figure 4 shows how the registers are decoded. After a register has been addressed for a read, the next 24 clock cycles clock the data out on the SDO pin. The clocks must be applied while $\overline{\text{SYNC}}$ is low. When $\overline{\text{SYNC}}$ is returned high, the SDO pin is placed in tristate. For a read of a single register, the no operation (NOP) function clocks out the data. Alternatively, if more than one register is to be read, the data of the first register to be addressed clocks out at the same time that the second register to be read is being addressed. The SDO pin must be enabled to complete a readback operation. The SDO pin is enabled by default.

Daisy-Chain Operation

For systems that contain several devices, use the SDO pin to daisy chain several devices together. Daisy-chain mode is useful in system diagnostics and in reducing the number of serial interface lines. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge.

By connecting the SDO of the first device to the SDI input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal $24 \times N$, where N is the total number of AD5761R/AD5721R devices in the chain. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high, which latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register.

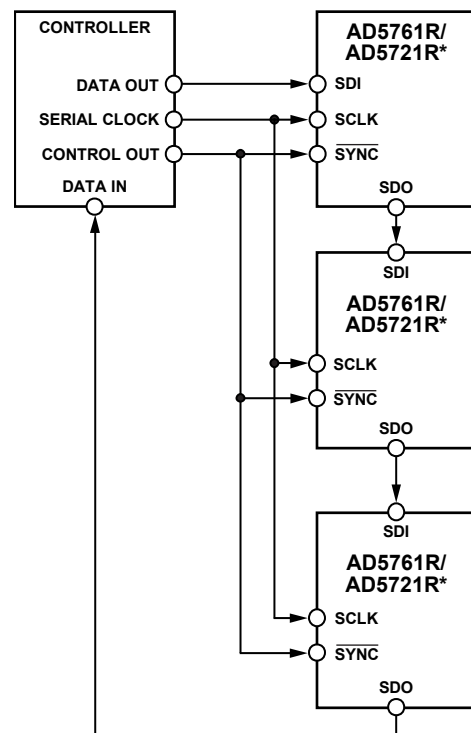


Figure 74. Daisy-Chain Block Diagram

HARDWARE CONTROL PINS

Load DAC Function ($\overline{\text{LDAC}}$)

After data transfers into the input register of the DAC, there are two ways to update the DAC register and DAC output. Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, one of two update modes is selected: synchronous DAC update or asynchronous DAC update.

Synchronous DAC Update

In synchronous DAC update mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the input shift register. The DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Asynchronous DAC Update

In asynchronous DAC update mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the input shift register. The DAC output is asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high. The update then occurs on the falling edge of $\overline{\text{LDAC}}$.

Reset Function ($\overline{\text{RESET}}$)

The AD5761R/AD5721R can be reset to their power-on state by two means: either by asserting the $\overline{\text{RESET}}$ pin or by using the software full reset registers (see Table 26).

Asynchronous Clear Function ($\overline{\text{CLEAR}}$)

The $\overline{\text{CLEAR}}$ pin is a falling edge active input that allows the output to be cleared to a user defined value. The clear code value is programmed by writing to Bit 10 and Bit 9 in the control register (see Table 11 and Table 12). Maintain $\overline{\text{CLEAR}}$ low for the minimum time of 20 ns to complete the operation (see Figure 2). When the $\overline{\text{CLEAR}}$ signal is returned high, the output remains at the clear value until a new value is loaded to the DAC register.

Alert Function ($\overline{\text{ALERT}}$)

When the $\overline{\text{ALERT}}$ pin is asserted low, a readback from the control register is required to clarify whether a short-circuit or brownout condition occurred, depending on the values of Bit 12 and Bit 11, the SC and BO bits, respectively (see Table 15 and Table 16). If neither of these conditions occurred, the temperature exceeded approximately 150°C.

The $\overline{\text{ALERT}}$ pin is low during power-up, a software full reset, or a hardware reset. After the first write to the control register to configure the DAC, the $\overline{\text{ALERT}}$ pin is asserted high.

In the event of the die temperature exceeding approximately 150°C, the $\overline{\text{ALERT}}$ pin is low and the value of the ETS bit determines the state of the digital supply of the device, whether the internal digital supply is powered on or powered down. If the ETS bit is set to 0, the internal digital supply is powered on when the internal die temperature exceeds approximately 150°C. If the ETS bit is set to 1, the internal digital supply is powered down when the internal die temperature exceeds approximately 150°C, and the device becomes nonfunctional (see Table 11 and Table 12).

The AD5761R/AD5721R temperature at power-up must be less than 150°C for proper operation of the devices.

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient. Thermal hysteresis data was tested for the AD5761R as shown in Figure 75. It is measured by sweeping the temperature from ambient to -40°C, then to 125°C, and returning to ambient. The V_{REF} delta is then measured between the two ambient measurements (shown in Figure 75).

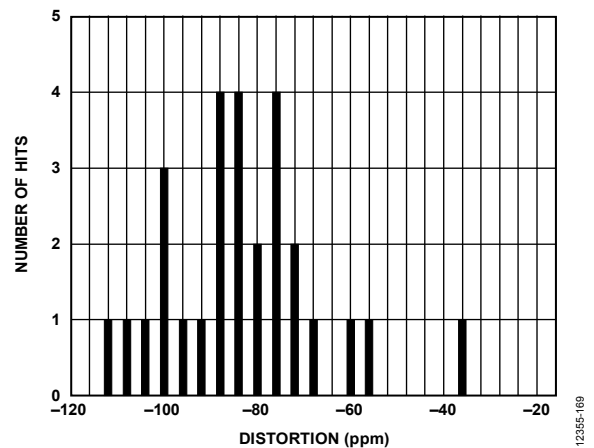


Figure 75. Thermal Hysteresis

REGISTER DETAILS

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK, which can operate at rates of up to 50 MHz. The input shift register consists of three don't care bits, one fixed value bit (DB20 = 0), four address bits, and a 16-bit or 12-bit data-word as shown in Table 8 and Table 9, respectively.

Table 8. AD5761R 16-Bit Input Shift Register Format

MSB								LSB	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]	
X ¹	X ¹	X ¹	0	Register address				Register data	

¹ X is don't care.

Table 9. AD5721R 12-Bit Input Shift Register Format

MSB								LSB	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:4]	DB[3:0]
X ¹	X ¹	X ¹	0	Register address				Register data	XXXX ¹

¹ X is don't care.

Table 10. Input Shift Register Commands

Register Address				Command
DB19	DB18	DB17	DB16	
0	0	0	0	No operation
0	0	0	1	Write to input register (no update)
0	0	1	0	Update DAC register from input register
0	0	1	1	Write and update DAC register
0	1	0	0	Write to control register
0	1	0	1	No operation
0	1	1	0	No operation
0	1	1	1	Software data reset
1	0	0	0	Reserved
1	0	0	1	Disable daisy-chain functionality
1	0	1	0	Readback input register
1	0	1	1	Readback DAC register
1	1	0	0	Readback control register
1	1	0	1	No operation
1	1	1	0	No operation
1	1	1	1	Software full reset

CONTROL REGISTER

The control register controls the mode of operation of the AD5761R/AD5721R. The control register options are shown in Table 11 and Table 12.

On power-up, after a full reset, or after a hardware reset, the output of the DAC is clamped to ground through a 1 k Ω resistor and the output buffer remains in power-down mode. A write to the control register is required to configure the device, remove the clamp to ground, and power up the output buffer.

When the DAC output range is reconfigured during operation, a software full reset command (see Table 26) must be written to the device before writing to the control register.

Table 11. Write to Control Register

MSB									LSB	
DB[23:21]	DB20	DB[19:16]	DB[15:11]	DB[10:9]	DB8	DB7	DB6	DB5	DB[4:3]	DB[2:0]
		Register address	Register data							
XXX ¹	0	0100	XXXXX ¹	CV[1:0]	OVR	B2C	ETS	IRO	PV[1:0]	RA[2:0]

¹ X is don't care.

Table 12. Control Register Functions

Bit Name	Description
CV[1:0]	CLEAR voltage selection. 00: zero scale 01: midscale 10, 11: full scale
OVR	5% overrange. 0: 5% overrange disabled 1: 5% overrange enabled
B2C	Bipolar range. 0: DAC input for bipolar output range is straight binary coded 1: DAC input for bipolar output range is twos complement coded
ETS	Thermal shutdown alert. The alert may not work correctly if the device powers on with temperature conditions >150°C (greater than the maximum rating of the device). 0: internal digital supply does not power down if die temperature exceeds 150°C. 1: internal digital supply powers down if die temperature exceeds 150°C.
IRO	Internal reference. 0: internal reference turned off 1: internal reference turned on
PV[1:0]	Power up voltage. 00: zero scale 01: midscale 10, 11: full scale
RA[2:0]	Output range. Before an output range configuration, the device must be reset. 000: -10 V to +10 V 001: 0 V to +10 V 010: -5 V to +5 V 011: 0 V to 5 V 100: -2.5 V to +7.5 V 101: -3 V to +3 V 110: 0 V to 16 V 111: 0 V to 20 V

Table 13. Bipolar Output Range Possible Codes

Straight Binary	Decimal Code	Twos Complement
1111	7	0111
1110	6	0110
1101	5	0101
1100	4	0100
1011	3	0011
1010	2	0010
1001	1	0001
1000	0	0000
0111	-1	1111
0110	-2	1110
0101	-3	1101
0100	-4	1100
0011	-5	1011
0010	-6	1010
0001	-7	1001
0000	-8	1000

READBACK CONTROL REGISTER

The readback control register operation provides the contents of the control register by setting the register address to 1100. Table 14 outlines the 24-bit shift register for this command, where the last 16 bits are don't care bits.

During the next command, the control register contents are shifted out of the SDO pin with the MSB shifted out first. Table 15 outlines the 24-bit data read from the SDO pin, where DB23 is the first bit shifted out.

Table 14. Readback Control Register, 24-Bit Shift Register to the SDI Pin

MSB			LSB
DB[23:21]	DB20	DB[19:16]	DB[15:0]
		Register address	Register data
XXX ¹	0	1100	Don't care

¹ X is don't care.

Table 15. Readback Control Register, 24-Bit Data Read from the SDO Pin

MSB												LSB
DB[23:21]	DB20	DB[19:16]	DB[15:13]	DB12	DB11	DB[10:9]	DB8	DB7	DB6	DB5	DB[4:3]	DB[2:0]
		Register address	Register data									
XXX ¹	0	1100	XXXX ¹	SC	BO	CV[1:0]	OVR	B2C	ETS	IRO	PV[1:0]	RA[2:0]

¹ X is don't care.

Table 16. Readback Control Register Bit Descriptions

Bit Name	Description
SC	Short-circuit condition. The SC bit is reset at every control register write. 0: no short-circuit condition detected 1: short-circuit condition detected
BO	Brownout condition. The BO bit is reset at every control register write. 0: no brownout condition detected 1: brownout condition detected

UPDATE DAC REGISTER FROM INPUT REGISTER

The update DAC register function loads the DAC register with the data saved in the input register and updates the DAC output voltage. This operation is equivalent to a software $\overline{\text{LDAC}}$. Table 17 outlines how data is written to the DAC register.

Table 17. Update DAC Register from Input Register

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
				Register address				Register data
X ¹	X ¹	X ¹	0	0010				Don't care

¹ X is don't care.

READBACK DAC REGISTER

The readback DAC register operation provides the contents of the DAC register by setting the register address to 1011. Table 18 outlines the 24-bit shift register for this command. During the next command, the DAC register contents are shifted out of the SDO pin with the MSB shifted out first. Table 19 outlines the 24-bit data read from the SDO pin, where DB23 is the first bit shifted out.

Table 18. Readback DAC Register, 24-Bit Shift Register to SDI Pin

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
				Register address				Register data
X ¹	X ¹	X ¹	0	1011				Don't care

¹ X is don't care.

Table 19. Readback DAC Register, 24-Bit Data Read from SDO Pin

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
				Register address				Register data
X ¹	X ¹	X ¹	0	1011				Data read from DAC register

¹ X is don't care.

WRITE AND UPDATE DAC REGISTER

The write and update DAC register (Register Address 0011) updates the input register and the DAC register with the entered data-word from the input shift register, irrespective of the state of $\overline{\text{LDAC}}$.

Setting the register address to 0001 writes the input register with the data from the input shift register, clocked in MSB first on the SDI pin.

Table 20. Write and Update DAC Register

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
				Register address				Register data
X ¹	X ¹	X ¹	0	0001				Data loaded
X ¹	X ¹	X ¹	0	0011				Data loaded

¹ X is don't care.

READBACK INPUT REGISTER

The readback input register operation provides the contents of the input register by setting the register address to 1010. Table 21 outlines the 24-bit shift register for this command. During the next command, the input register contents are shifted out of the SDO pin with the MSB shifted out first. Table 22 outlines the 24-bit data read from the SDO pin, where DB23 is the first bit shifted out.

Table 21. Readback Input Register, 24-Bit Shift Register to the SDI Pin

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
Register address								Register data
X ¹	X ¹	X ¹	0	1010				Don't care

¹ X is don't care.

Table 22. Readback Input Register, 24-Bit Data Read from the SDO Pin

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
Register address								Register data
X ¹	X ¹	X ¹	0	1010				Data read from input register

¹ X is don't care.

DISABLE DAISY-CHAIN FUNCTIONALITY

The daisy-chain feature can be disabled to save the power consumed by the SDO buffer when this functionality is not required (see Table 23). When disabled, a readback request is not accepted because the SDO pin remains in tristate.

Table 23. Disable Daisy-Chain Functionality Register

MSB								LSB	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:1]	DB0
Register address								Register data	
X ¹	X ¹	X ¹	0	1001				Don't care	DDC

¹ X is don't care.

Table 24. Disable Daisy-Chain Bit Description

Bit Name	Description
DDC	DDC decides whether daisy-chain functionality is enabled or disabled for the device. By default, daisy-chain functionality is enabled. 0: daisy-chain functionality is enabled for the device. 1: daisy-chain functionality is disabled for the device.

SOFTWARE DATA RESET

The AD5761R/AD5721R can be reset via software to zero scale, midscale, or full scale (see Table 25). The value to which the device is reset is specified by the PV[1:0] bits, which are set in the write to control register command (see Table 11 and Table 12).

Table 25. Software Data Reset Register

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
Register address								Register data
X ¹	X ¹	X ¹	0	0111				Don't care

¹ X is don't care.

SOFTWARE FULL RESET

The device can also be reset completely via software (see Table 26). When the register address is set to 1111, the device behaves in a power-up state, where the output is clamped to AGND and the output buffer is powered down. The user must write to the control register to configure the device, remove the 1 k Ω resistor clamp to ground, and power up the output buffer.

The software full reset command is also issued when the DAC output range is reconfigured during normal operation.

Table 26. Software Full Reset Register

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
				Register address				Register data
X ¹	X ¹	X ¹	0	1111				Don't care

¹X is don't care.

NO OPERATION REGISTERS

The no operation registers are ignored and do not vary the state of the device (see Table 27).

Table 27. No Operation Registers

MSB								LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB[15:0]
				Register address				Register data
X ¹	X ¹	X ¹	0	0000/0101/0110/1101/1110				Don't care

¹X is don't care.

APPLICATIONS INFORMATION

TYPICAL OPERATING CIRCUIT

Figure 76 shows the typical operating circuit for the [AD5761R/AD5721R](#). The only external components needed for this precision 16-/12-bit DAC are decoupling capacitors on the supply pins and supply voltage. Because the [AD5761R/AD5721R](#) incorporate a voltage reference and reference buffers, they eliminate the need for an external bipolar reference and associated buffers, resulting in overall savings in both cost and board space.

In Figure 76, V_{DD} is connected to 15 V and V_{SS} is connected to -15 V, but V_{DD} and V_{SS} can operate with supplies from 4.75 V to 30 V and from -16.5 V to 0 V, respectively.

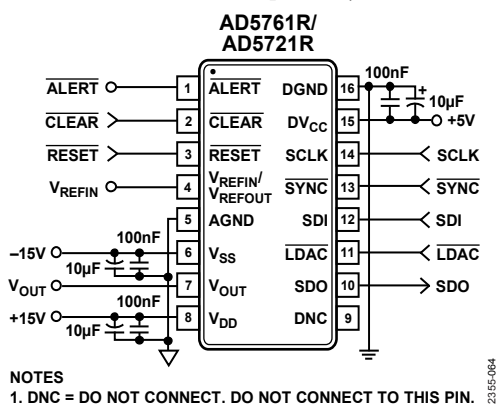


Figure 76. Typical Operating Circuit

POWER SUPPLY CONSIDERATIONS

The [AD5761R/AD5721R](#) must be powered by the following three supplies to provide any of the eight output voltage ranges available on the DAC: $V_{DD} = 21$ V, $V_{SS} = -11$ V, and $DV_{CC} = 5$ V.

For applications requiring optimal high power efficiency and low noise performance, it is recommended to use the [ADP5070](#) switching regulator to convert the 5 V input rail into two intermediate rails ($+23$ V and -13 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators ([ADP7142](#) and [ADP7182](#)). Figure 77 shows the recommended method.

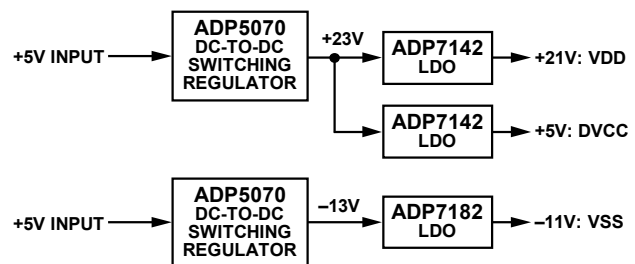
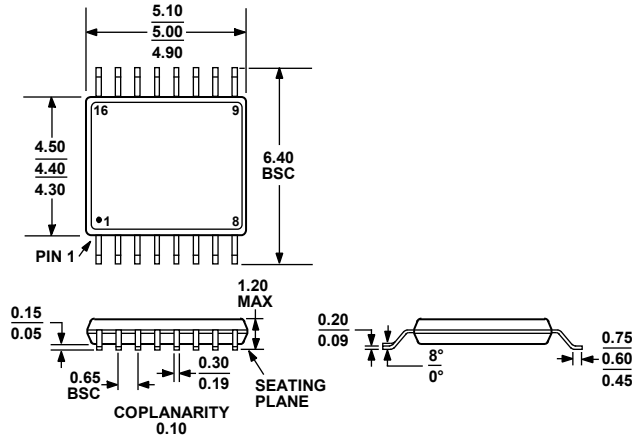


Figure 77. Postregulation by [ADP7142](#) and [ADP7182](#)

EVALUATION BOARD

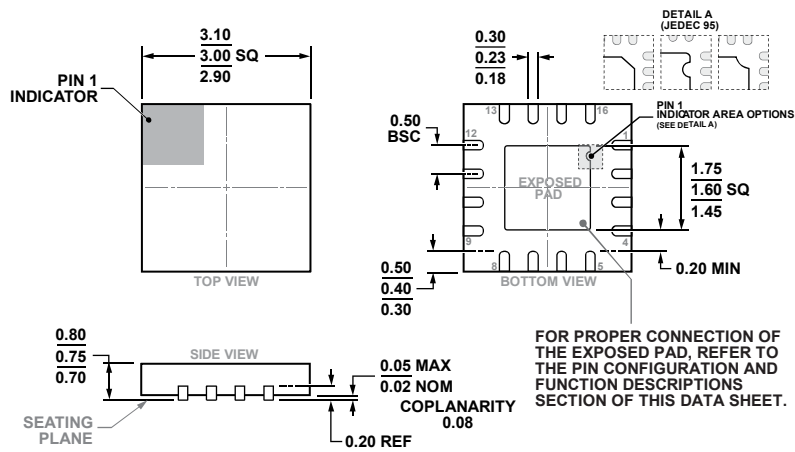
An evaluation board is available for the [AD5761R](#) to aid designers in evaluating the high performance of the device with minimum effort. The [AD5761R](#) evaluation kit includes a populated and tested [AD5761R](#) printed circuit board (PCB). The evaluation board interfaces to the USB port of a PC. Software is available with the evaluation board to allow the user to easily program the [AD5761R](#). The [EVAL-AD5761RSDZ](#) user guide provides full details on the operation of the evaluation board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 78. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 79. 16-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.75 mm Package Height (CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1, 2}	Resolution (Bits)	Internal Reference (V)	Temperature Range	INL (LSB)	Package Description	Package Option	Marking Code
AD5721RBRUZ	12	2.5	-40°C to +125°C	±0.5	16-Lead TSSOP	RU-16	
AD5721RBRUZ-RL7	12	2.5	-40°C to +125°C	±0.5	16-Lead TSSOP	RU-16	
AD5721RBCPZ-RL7	12	2.5	-40°C to +125°C	±0.5	16-Lead LFCSP	CP-16-22	DHN
AD5761RARUZ	16	2.5	-40°C to +125°C	±8	16-Lead TSSOP	RU-16	
AD5761RARUZ-RL7	16	2.5	-40°C to +125°C	±8	16-Lead TSSOP	RU-16	
AD5761RBRUZ	16	2.5	-40°C to +125°C	±2	16-Lead TSSOP	RU-16	
AD5761RBRUZ-RL7	16	2.5	-40°C to +125°C	±2	16-Lead TSSOP	RU-16	
AD5761RACPZ-RL7	16	2.5	-40°C to +125°C	±8	16-Lead LFCSP	CP-16-22	DJ5
AD5761RBCPZ-RL7	16	2.5	-40°C to +125°C	±2	16-Lead LFCSP	CP-16-22	DJ6
EVAL-AD5761RSDZ					Evaluation Board		
EVAL-SDP-CB1Z					SDP Controller Board		

¹ Z = RoHS Compliant Part.

² The EVAL-AD5761RSDZ can be used to evaluate the AD5721R.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View AD5721RBRUZ-RL7 on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management