THE DATASHEET OF

ADAR2004ACCZ

10 GHz to 40 GHz, 4-Channel Rx Mixer with 4× LO Multiplier/Filter

Data Sheet **ADAR2004**

FEATURES

Quad LNA, mixer, IF VGA
4× LO multiplier with programmable harmonic filter
RF input frequency range: 10 GHz to 40 GHz
IF output frequency range: 0 MHz to 800 MHz
LO input frequency range: 2.4 GHz to 10.1 GHz
Gain range: 21 dB to 41 dB
Input P1dB: −20 dBm typical (at minimum gain)
Noise figure: 9 dB typical (at maximum gain)
3-wire or 4-wire SPI control
On-chip programmable state machines for fast multiplier/filter and receiver switching and control
On-chip temperature sensor and ADC
DC power: 910 mW (2.5 V supply)
7 mm × 7 mm, 48-terminal LGA package

APPLICATIONS

Millimeter wave imaging
- **Security**
- **Medical**
- **Industrial**

Multichannel receivers

GENERAL DESCRIPTION

The ADAR2004 is a 4-channel receiver IC that is optimized for millimeter wave body scanning applications. Accepting differential input signals from 10 GHz to 40 GHz, the ADAR2004 provides a low intermediate frequency (IF) output up to 800 MHz. Each receive channel also has independent gain control.

The mixer local oscillator (LO) path includes a 4× multiplier requiring an applied LO frequency between 2.4 GHz and 10.1 GHz. The 4× multiplier block includes a programmable filter that helps keep harmonics down before reaching the mixer.

Two programmable state machines are included to facilitate simple configuration, control, and fast switching of the frequency multiplier, filter, and receiver sections. These sequencers are programmed through the serial peripheral interface (SPI) and are then operated by pulsed inputs (reset and advance).

The ADAR2004 requires only a single 2.5 V supply with power consumption of 910 mW with all channels turned on.

The ADAR2004 is available in a 7 × 7 mm, 48-terminal LGA package and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

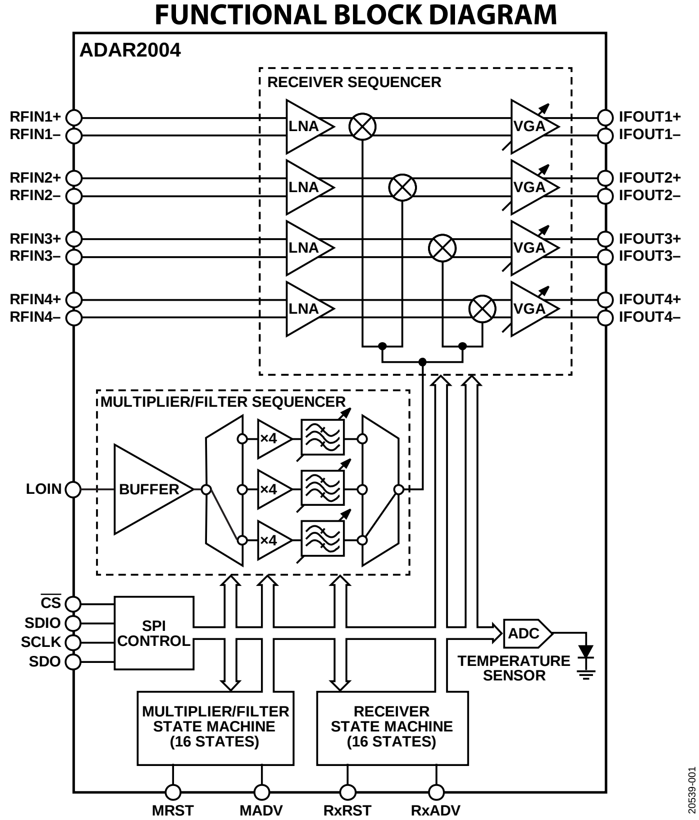

Figure 1.

Rev. 0 Document Feedback

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Technical Support **www.analog.com**

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REVISION HISTORY

8/2020—Revision 0: Initial Version

SPECIFICATIONS

V_{POS1}, V_{POS2}, V_{POS4} = 2.5 V, V_{POS3} = VREG, and T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL PERFORMANCE					
Input Power for 1 dB Compression (P1dB)	Minimum gain		−20		dBm
	Maximum gain		−36		dBm
Input Third-Order Intercept (IP3)	Minimum gain, −50 dBm per tone		−11		dBm
	Maximum gain, −50 dBm per tone		−25		dBm
Noise Figure	Minimum gain		11		dB
	Maximum gain		9		dB
Gain	Minimum gain		21		dB
	Maximum gain		41		dB
Gain Step			2.9		dB
Gain Flatness vs. RF Input Frequency			2		dB
Gain Change vs. Temperature			−0.05		dB/°C
RF INPUT					
Frequency Range		10		40	GHz
Differential Input Impedance			100		Ω
Return Loss	10 GHz to 40 GHz		−11		dB
IF OUTPUT					
Frequency Range		0		800	MHz
Bandwidth	3 dB bandwidth, maximum gain		800		MHz
Differential Output Impedance			100		Ω
Peak-to-Peak Output Voltage Swing	At P1dB point, minimum gain		1.125		V
	At P1dB point, maximum gain		0.632		V
Return Loss			−20		dB
Amplitude Settling time	<1 dB		5		ns
Output Common-Mode Voltage (V_{OCM})	Minimum		0.65		V
	Maximum		1.2		V
LO INPUT					
Frequency Range		2.4		10.1	GHz
Power Range		−25	−20	−10	dBm
Impedance			50		Ω
Return Loss			−12		dB
STATE MACHINES AND TIMING					
Minimum Pulse Width					
MADV, MRST		3			ns
RxADV, RxRST		3			ns
Minimum Pulse Separation	Pulse start to pulse start				
MADV, MRST		10			ns
RxADV, RxRST		10			ns
Switching Frequency	Using ready mode			100	MHz
Switching Time					
Multiplier Band Sleep to Active			50		ns
Multiplier Band Switch	Using ready mode		10		ns
Receiver Sleep to Active			50		ns
DIGITAL INPUT LOGIC LEVELS					
Logic Low			0	0.3	V
Logic High		1	1.8		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL OUTPUT LOGIC LEVELS					
Logic Low			0	0.4	V
Logic High		1.4	1.8		V
VREG OUTPUT			1.8		V
POWER SUPPLY					
Analog					
Supply Voltage Range (V_{POS1}, V_{POS2}, V_{POS4})		2.25	2.5	2.75	V
Current Consumption	All channels active		364		mA
	Chip disabled		3		mA
Power Consumption	All channels active		910		mW
	Chip disabled		7.5		mW
Digital					
Supply Voltage Range (V_{POS3})		1.6	1.8	2	V
Current Consumption			25		μA
Power Consumption			45		μW

TIMING SPECIFICATIONS

V_{POS1}, V_{POS2}, V_{POS4} = 2.5 V, V_{POS3} = VREG, and T_A = −40°C to +85°C, unless otherwise noted. See Figure 2 to Figure 4 for the timing diagrams.

Table 2. SPI Timing

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
f_{SCLK}	Maximum clock rate	Write only			40	MHz
		Write and read			15	MHz
t_{PWH}	Minimum pulse width high			10		ns
t_{PWL}	Minimum pulse width low			10		ns
t_{DS}	Setup time, SDIO to SCLK			5		ns
t_{DH}	Hold time, SDIO to SCLK			5		ns
t_{DV}	Data valid, SDO to SCLK			5		ns
t_{DCS}	Setup time, $\overline{CS}$ to SCLK			10		ns
t_R	SDIO, SDO rise time	Outputs loaded with 10 pF, 10% to 90%		40		ns
t_F	SDIO, SDO fall time	Outputs loaded with 10 pF, 10% to 90%		40		ns

Timing Diagrams

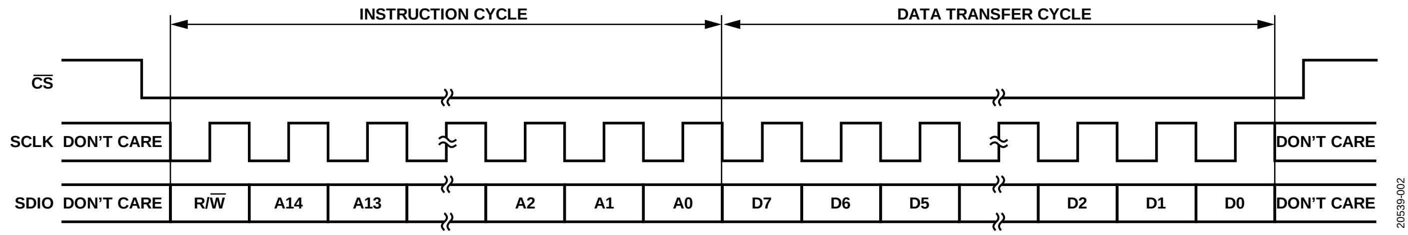


Figure 2. SPI Transaction Structure (MSB First)

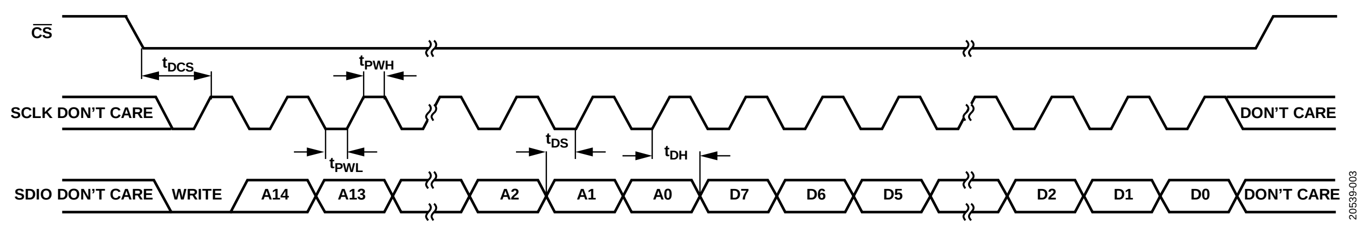


Figure 3. SPI Write Timing Diagram

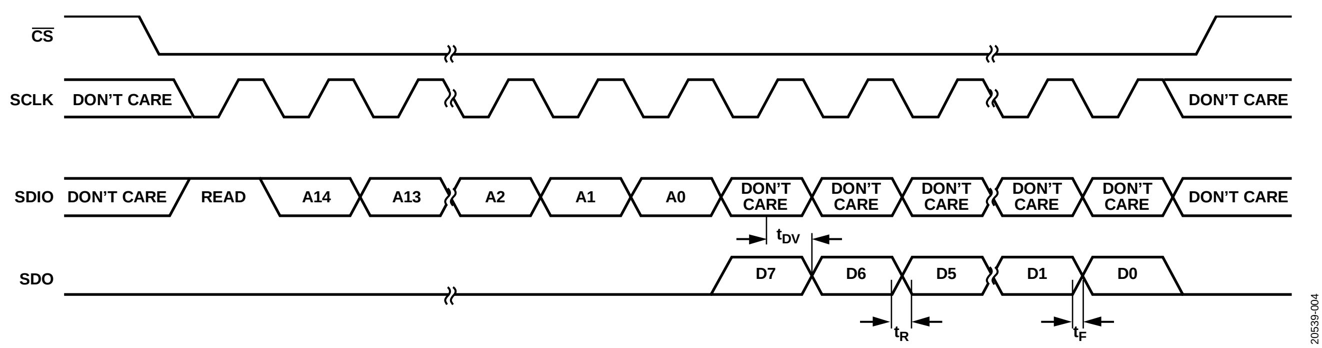


Figure 4. SPI 4-Wire Read Timing Diagram

SPI Block Write Mode

Data can be written to the SPI registers using the block write mode where the register address automatically increments and data for consecutive registers can be written without sending new address bits. Data writing can be continued indefinitely until $\overline{CS}$ is raised, ending the transaction (see Figure 5).

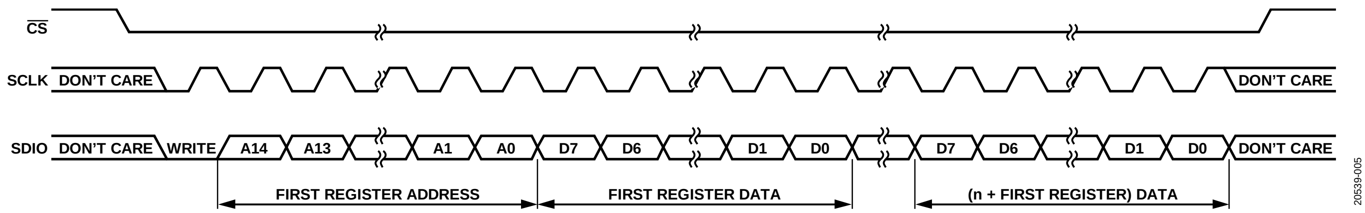


Figure 5. SPI Block Write

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{POS1}, V_{POS2}, V_{POS4} to GND[1]	+3 V, −0.3 V
V_{POS3} to GND[1]	+2 V, −0.3 V
Digital Input to GND[1]	2 V
RFINx±, LOIN to GND[1]	±0.3 V
RFINx± Power	20 dBm
LOIN Power	−5 dBm
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Junction	135°C
Reflow Soldering	
Peak Temperature	260°C

[1] GND is the common ground to which all GNDx pins are connected.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CC-48-2[1]	32.1	11	°C/W

[1] Pad soldered.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

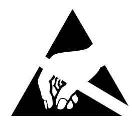
Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAR2004

Table 5. ADAR2004, 48-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	1000 to 2000	1C
CDM	1000 to 1250	C3

ESD CAUTION

	**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

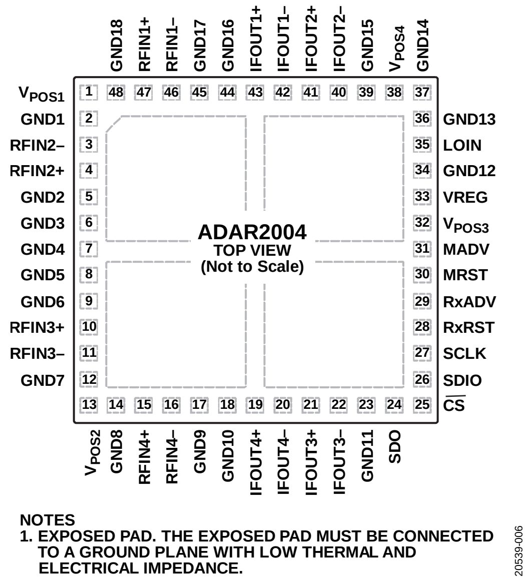


Figure 6. Pin Configuration (Top View, Not to Scale)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 13, 38	V_{POS1}, V_{POS2}, V_{POS4}	2.5 V Power Supply for the Analog Section. Connect decoupling capacitors (one 10 nF and one 100 pF on each pin and a 1 µF for the rail) to the ground plane as close as possible to the V_{POS1}, V_{POS2}, and V_{POS4} pins.
2, 5 to 9, 12, 14, 17, 18, 23, 34, 36, 37, 39, 44, 45, 48	GND1 to GND18	Ground. Connect all ground pins to a ground plane with low thermal and electrical impedance.
3, 4, 10, 11, 15, 16, 46, 47	RFIN2−, RFIN2+, RFIN3+, RFIN3−, RFIN4+, RFIN4−, RFIN1−, RFIN1+	Differential RF Inputs. RFINx± are 100 Ω differential pairs, ac-coupled internally. The RFINx± pins operate from 10 GHz to 40 GHz. All eight lines must have equal electrical and mechanical lengths to ensure consistent performance from channel to channel.
19 to 22, 40 to 43	IFOUT4+, IFOUT4−, IFOUT3+, IFOUT3−, IFOUT2−, IFOUT2+, IFOUT1−, IFOUT1+	Differential IF Outputs. IFOUTx± are 100 Ω differential pairs, dc-coupled internally. The IFOUTx± pins operate from low frequency to 800 MHz. V_{OCM} = 0.8 V. All eight lines must have equal electrical and mechanical lengths.
24	SDO	Serial Data Output. Register states can be read back on the SDO line if Register 0x000, Bits[4:3] are set high.
25	$\overline{CS}$	Chip Select Bar. Pull the $\overline{CS}$ pin low to activate the SPI port. $\overline{CS}$ is used to activate the SPI port on the ADAR2004 and is active low. When $\overline{CS}$ goes high, the data stored in the shift registers is latched. Connect a 200 kΩ pull-up resistor to 1.8 V to ensure that the SPI is shut off while not in use.
26	SDIO	Serial Data Input and Output. The SDIO pin is a high impedance data input for clocking in information. The SDIO pin can also be used to read out data if Register 0x000, Bits[4:3] are set low (default).
27	SCLK	Serial Clock. The SCLK pin is used to clock data into and out of the SPI.
28	RxRST	Receive State Machine Reset. If the state machine is enabled, RxRST immediately sets the receiver state machine back to the configuration in RX_EN_MODE_0, RX_GAIN12_MODE_0, and RX_GAIN34_MODE_0 (Register 0x040, Register 0x041, and Register 0x042).
29	RxADV	Receive State Machine Advance. If the state machine is enabled, RxADV advances the receiver state machine to the next state in its cycle. If currently at the end of the cycle, pulsing RxADV returns the pointer to the mode defined in RX_STATE_1 (Register 0x01A, Bits[7:4]).
30	MRST	Multiplier State Machine Reset. If the state machine is enabled, MRST immediately sets the multiplier/filter state machine back to the configuration in MULT_EN_MODE_0 (Register 0x070).
31	MADV	Multiplier State Machine Advance. If the state machine is enabled, MADV advances the multiplier/filter state machine to the next state in its cycle. If currently at the end of the cycle, pulsing MADV returns the pointer to the mode defined in MULT_STATE_1 (Register 0x022, Bits[7:4]).

Pin No.	Mnemonic	Description
32	V_{POS3}	1.8 V Power Supply for the Digital Section. Connect this supply directly to VREG. Place a 1 µF capacitor to ground as close as possible to V_{POS3}.
33	VREG	1.8 V Low Dropout (LDO) Output. Connect VREG directly to V_{POS3}.
35	LOIN	LO Input. LOIN is a single-ended, 50 Ω input operating from 2.4 GHz to 10.1 GHz, ac-coupled internally. The nominal input power level is −20 dBm.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal and electrical impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

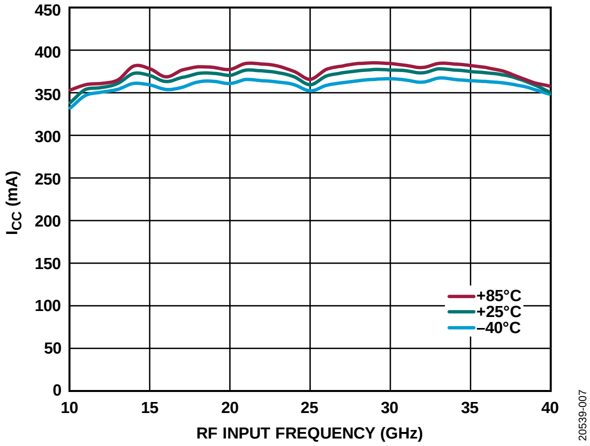


Figure 7. Supply Current (I_{CC}) vs. RF Input Frequency and Temperature

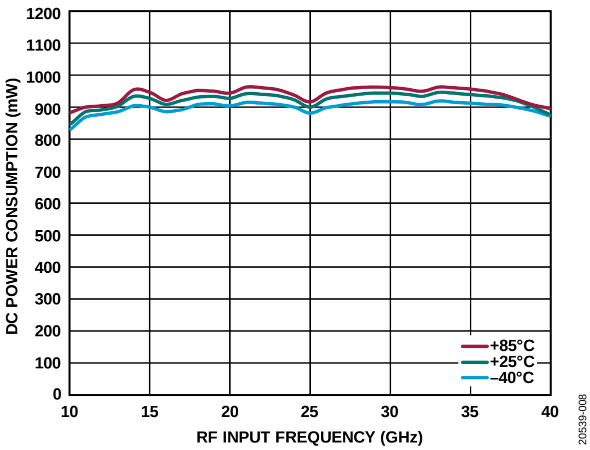


Figure 8. DC Power Consumption vs. RF Input Frequency and Temperature

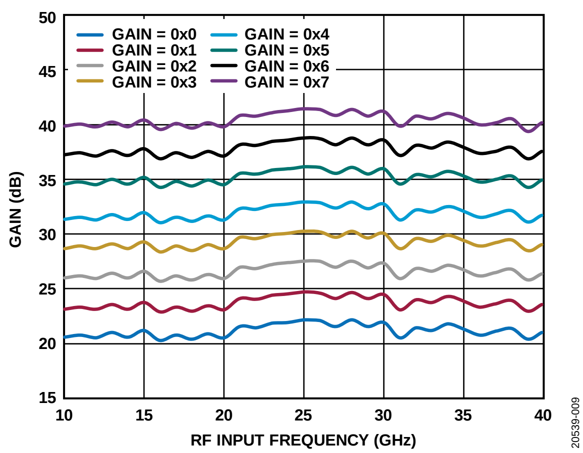


Figure 9. Gain vs. RF Input Frequency and Gain Setting

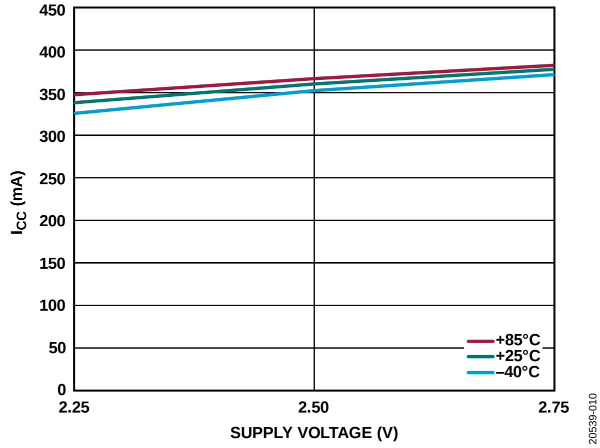


Figure 10. I_{CC} vs. Supply Voltage and Temperature

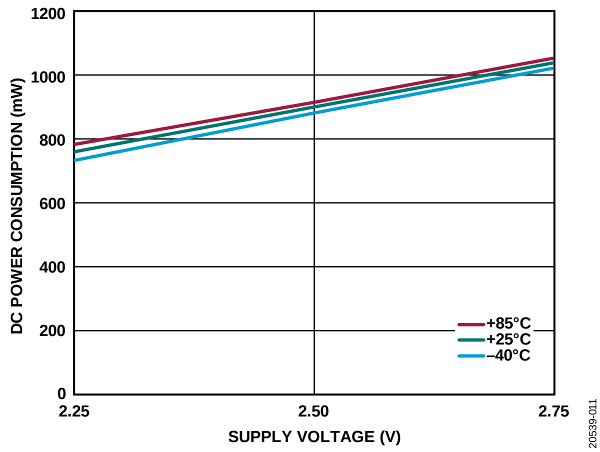


Figure 11. DC Power Consumption vs. Supply Voltage and Temperature

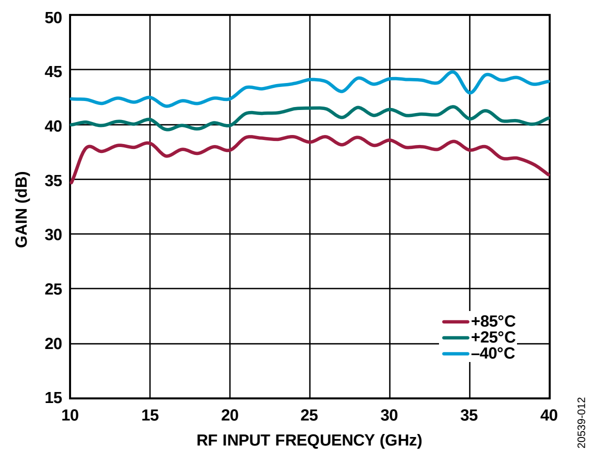


Figure 12. Gain vs. RF Input Frequency and Temperature (Gain = 0x7)

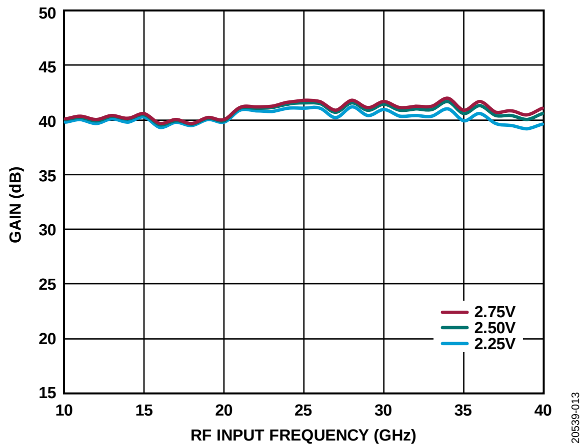


Figure 13. Gain vs. RF Input Frequency and Supply Voltage (V_{CC}) (Gain = 0x7)

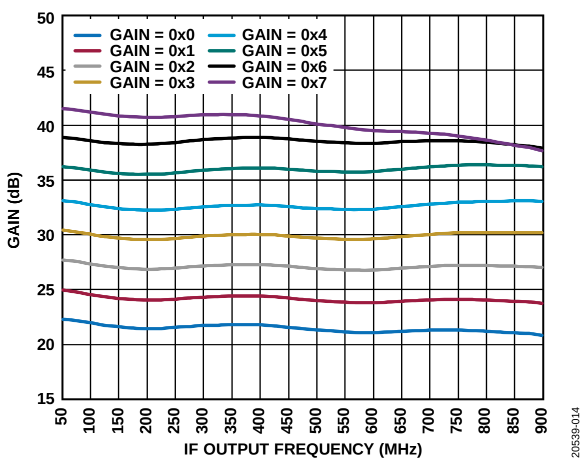


Figure 14. Gain vs. IF Output Frequency and Gain Setting (RF Input = 25 GHz)

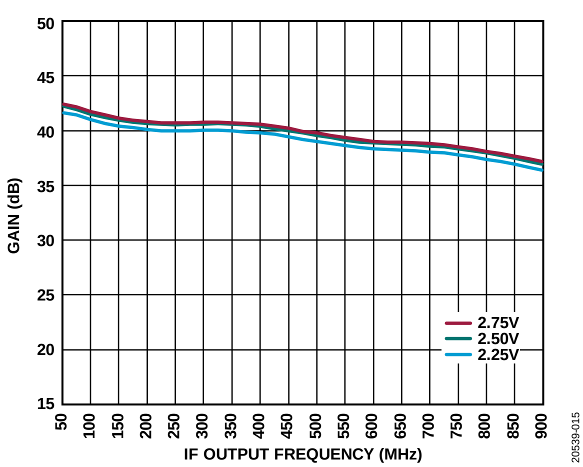


Figure 15. Gain vs. IF Output Frequency and V_{CC} (RF Input = 25 GHz, Gain = 0x7)

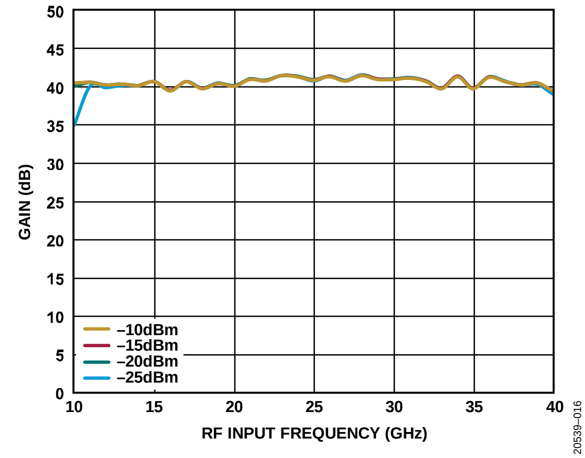


Figure 16. Gain vs. RF Input Frequency and LO Input Power

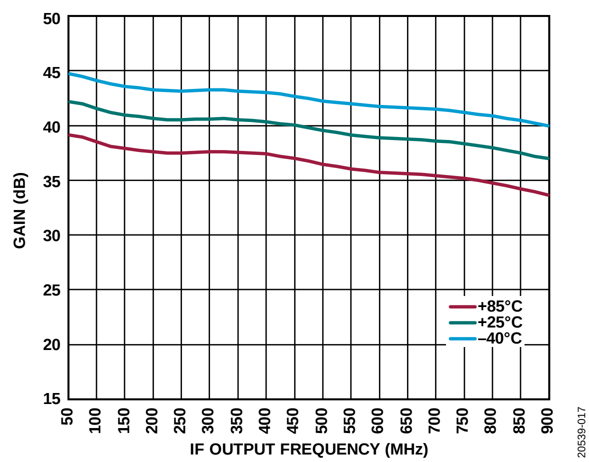


Figure 17. Gain vs. IF Output Frequency and Temperature (RF Input = 25 GHz, Gain = 0x7)

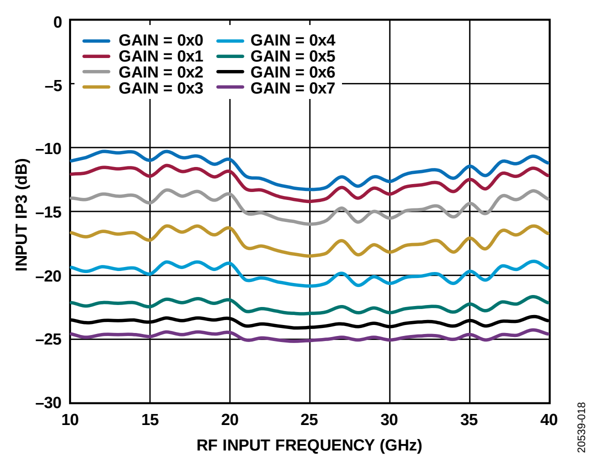


Figure 18. Input IP3 vs. RF Input Frequency and Gain Setting

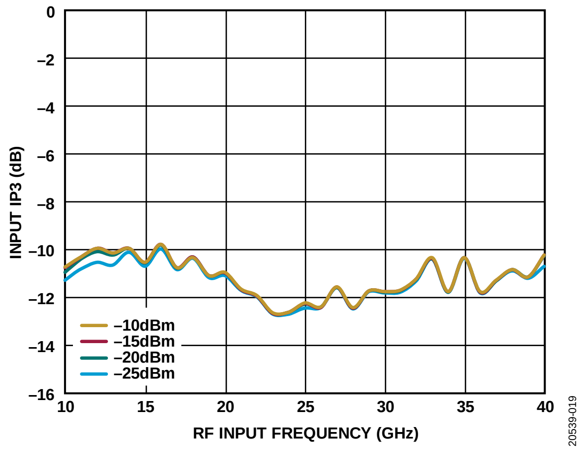


Figure 19. Input IP3 vs. RF Input Frequency and LO Input Power

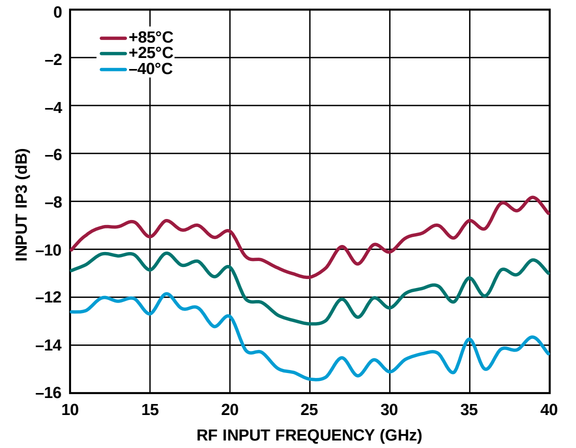


Figure 22. Input IP3 vs. RF Input Frequency and Temperature

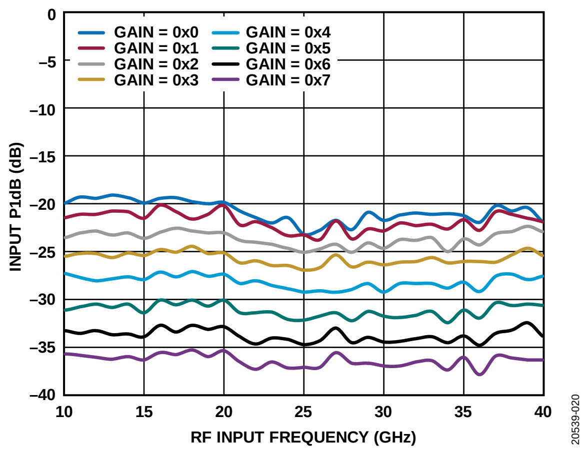


Figure 20. Input P1dB vs. RF Input Frequency and Gain Setting

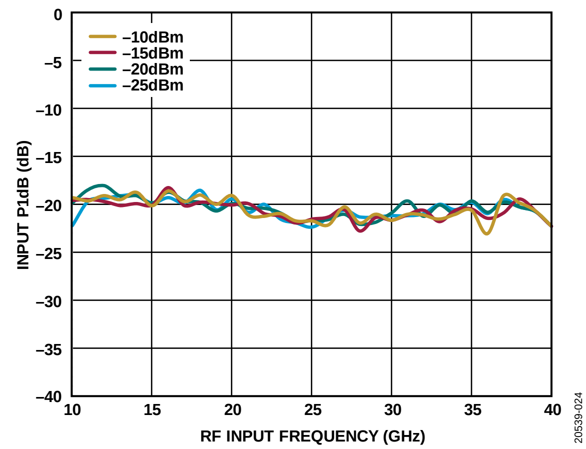


Figure 23. Input P1dB vs. RF Input Frequency and LO Input Power

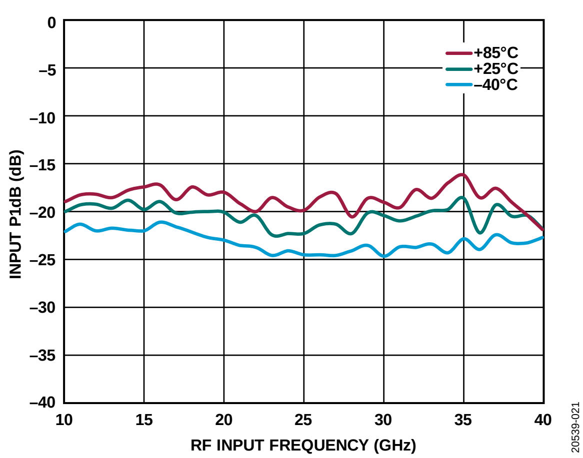


Figure 21. Input P1dB vs. RF Input Frequency and Temperature

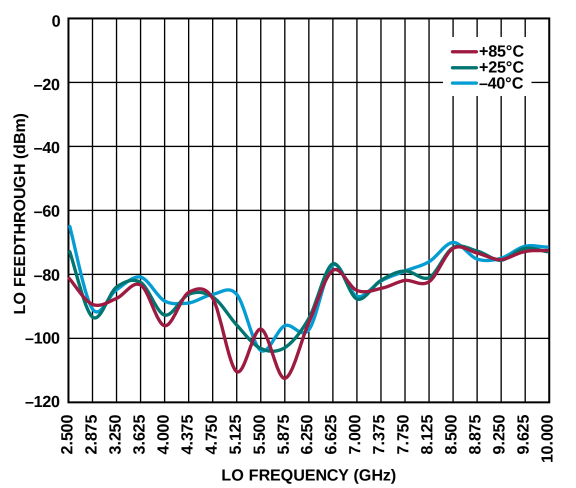


Figure 24. LO Feedthrough vs. LO Frequency and Temperature

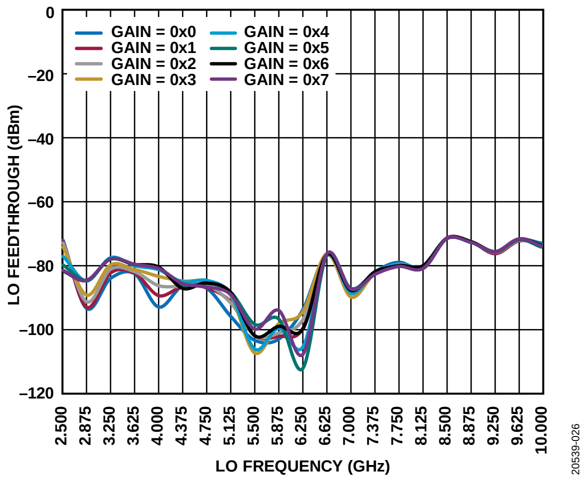


Figure 25. LO Feedthrough vs. LO Frequency and Gain Setting

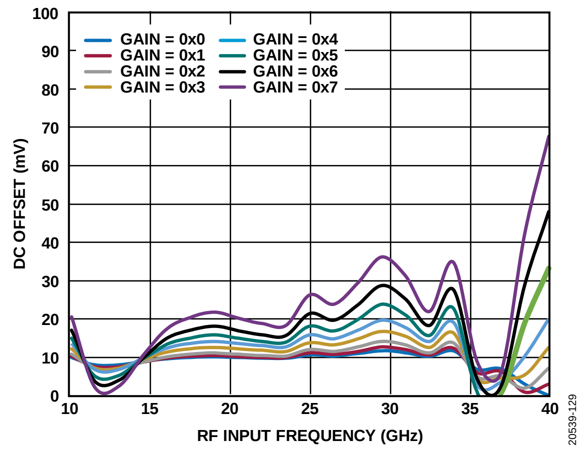


Figure 28. DC Offset vs. RF Input Frequency and Gain Setting

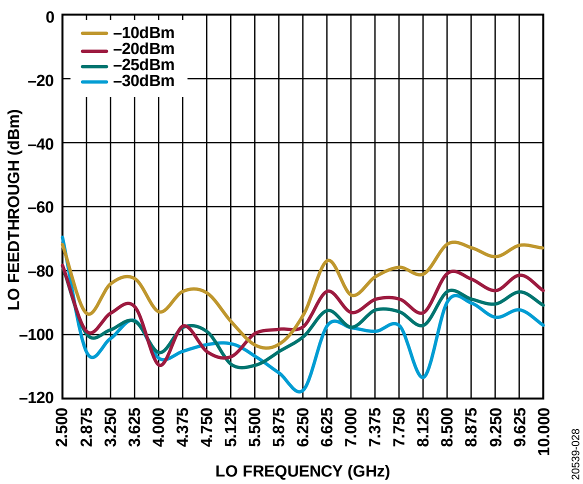


Figure 26. LO Feedthrough vs. LO Frequency and LO Input Power

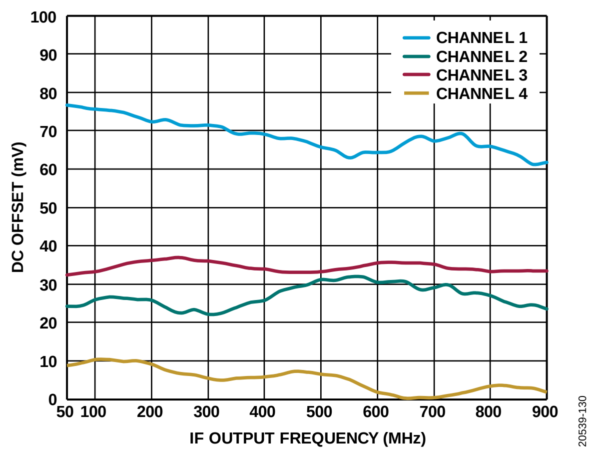


Figure 29. DC Offset vs. IF Output Frequency and Channel

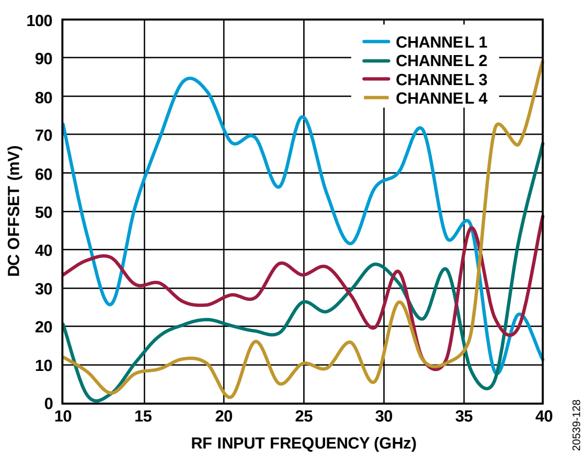


Figure 27. DC Offset vs. RF Input Frequency and Channel

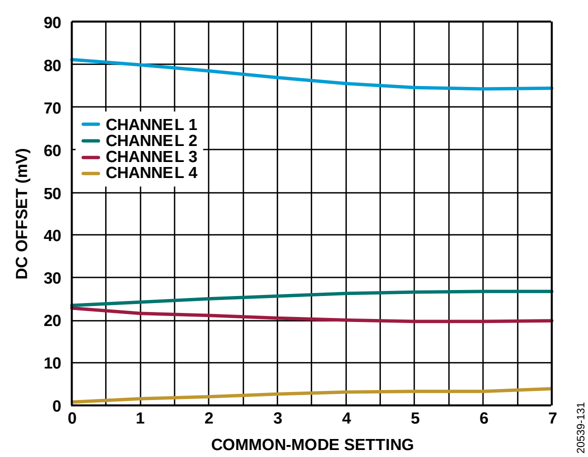


Figure 30. DC Offset vs. Common-Mode Setting and Channel (RF Input = 25 GHz, Gain = 0x7)

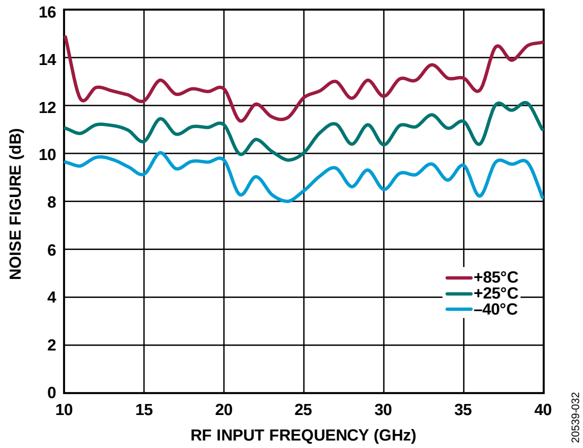


Figure 31. Noise Figure vs. RF Input Frequency and Temperature

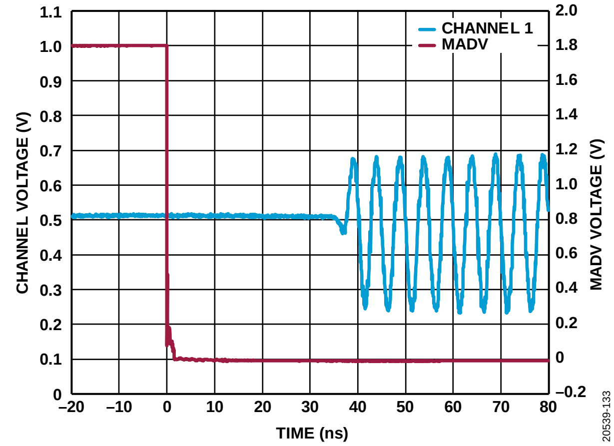


Figure 34. Multiplier Sleep to Active Switching Time

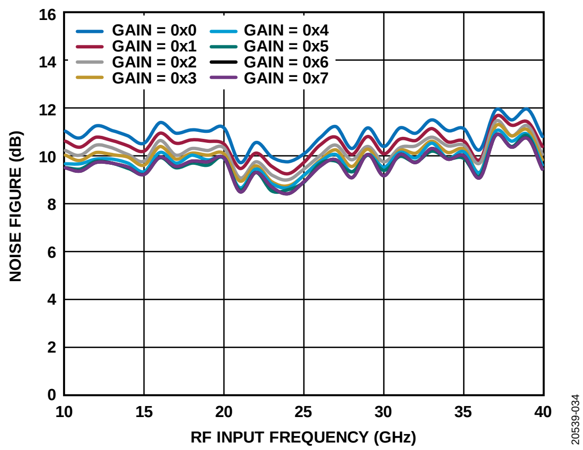


Figure 32. Noise Figure vs. RF Input Frequency and Gain Setting

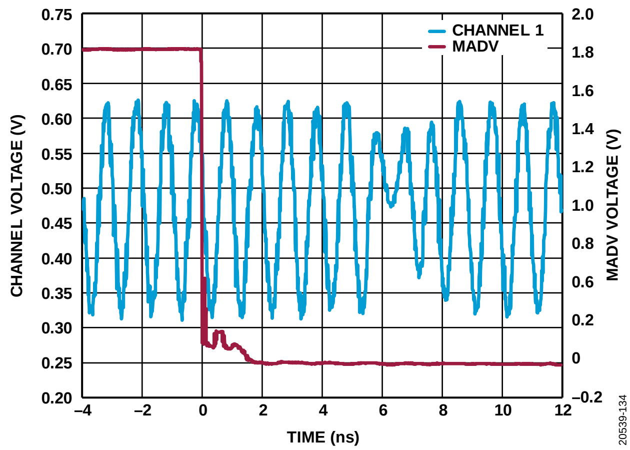


Figure 35. Frequency Band Switching Time

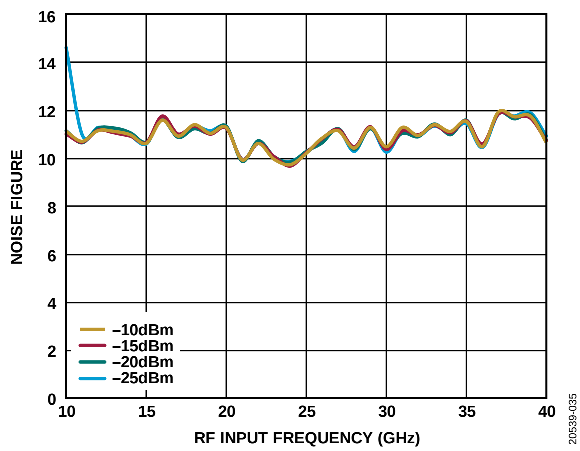


Figure 33. Noise Figure vs. RF Input Frequency and LO Input Power (Gain = 0x0)

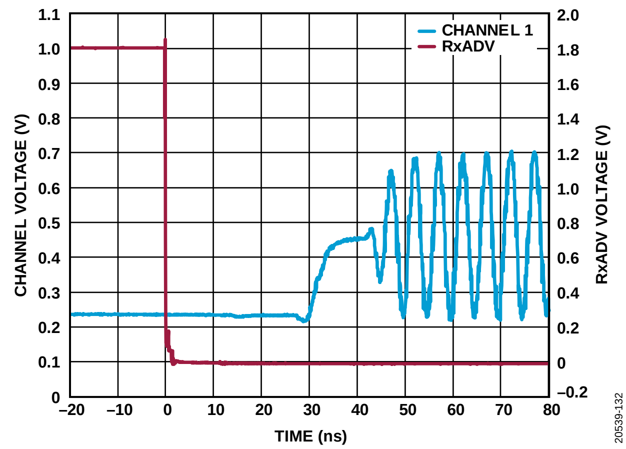


Figure 36. Receiver Sleep to Active Switching Time

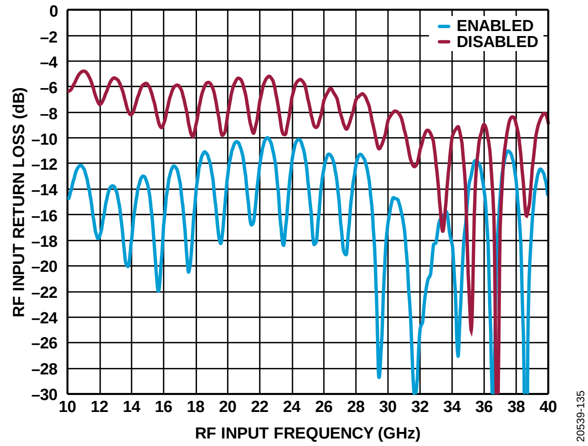


Figure 37. RF Input Return Loss vs. RF Input Frequency

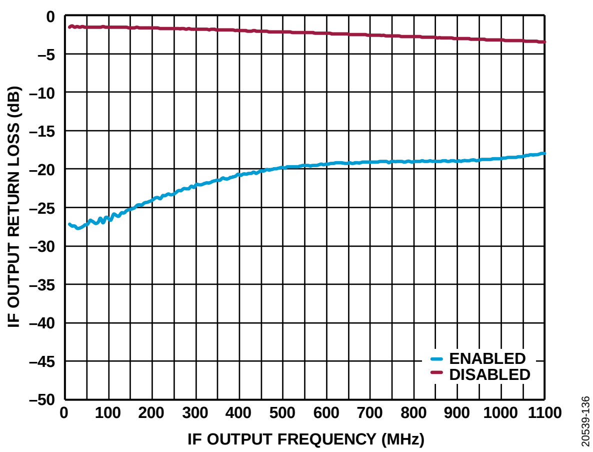


Figure 38. IF Output Return Loss vs. IF Output Frequency

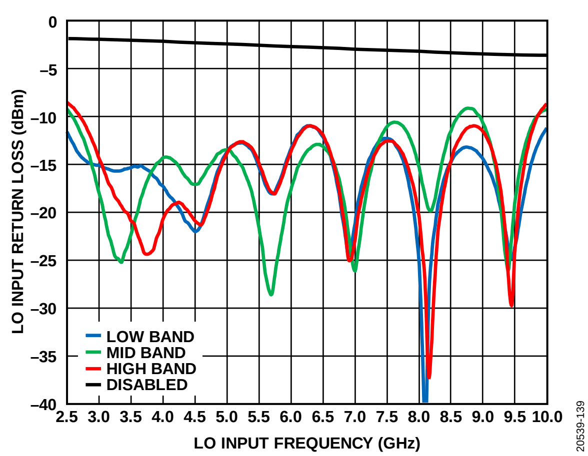


Figure 39. LO Input Return Loss vs. LO Input Frequency

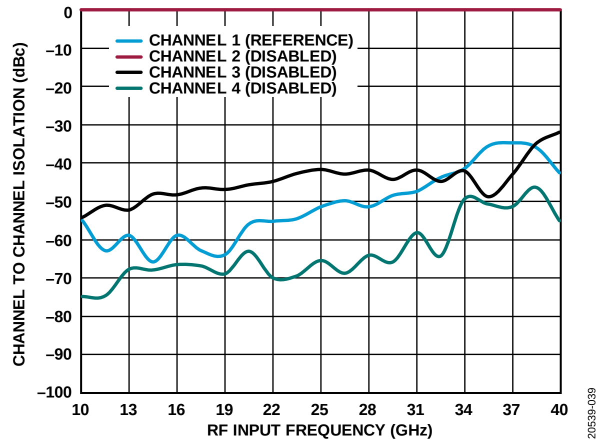


Figure 40. Channel to Channel Isolation vs. RF Input Frequency

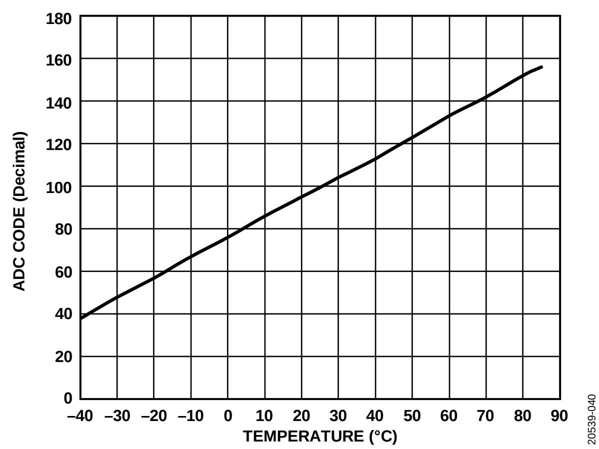


Figure 41. ADC Code vs. Temperature

THEORY OF OPERATION

OVERVIEW

The main elements of the ADAR2004 are a quad LNA, a mixer, an IF variable gain amplifier (VGA), a 4× LO frequency multiplier with integrated switchable harmonic filter, and a 1:4 signal splitter.

The four differential RF inputs are intended to be connected directly to a differential antenna structure, such as a dipole. Apply a single-tone LO input signal in the 2.4 GHz to 10.1 GHz frequency range with a power level of approximately −20 dBm to the LOIN port. This signal is frequency multiplied by 4 and filtered before driving the LO inputs of the four mixers.

The operation of these subcircuits can be controlled from the SPI port as well as two programmable state machines, one focused on LO multiplier/filter control and the other focused on quad receiver control.

The ADAR2004 also includes an Analog Devices, Inc., SPI port that is used for device configuration and readback. Although the state machines provide fast switching between states, all functions can also be controlled directly through the SPI port.

LO INPUT BUFFER, 4× MULTIPLIER, AND BAND-PASS FILTER

The LO input buffer provides approximately 17 dB of gain and provides an optimal drive signal to the 4× multiplier circuits for LO input power levels down to −25 dBm. The bias levels of the input and output stages of the input buffer are independently adjustable through the SPI via Register 0x013. See the Bias Points and Voltages section for more information.

The broadband frequency multiplier consists of three parallel subcircuits. Each subcircuit (low band, mid band, high band) is optimized to multiply and filter a segment of the total frequency range (2.4 GHz to 10.1 GHz input, 9.6 GHz to 40.4 GHz output). Recommended ranges and register settings for each band are shown in Table 7. SP3T switches at the input and output of the multiplier block are used to select the desired subcircuit.

Each subcircuit consists of a 4× multiplier and an adjustable band-pass filter (BPF). The bias levels of the 4× multipliers are adjustable through the SPI via Register 0x011 and Register 0x012. See the Bias Points and Voltages section for more information.

When the LO input frequency is in the low end of the subcircuit band, the BPF corner frequency must be set to its low state. Set the associated bit high to set the BPF corner frequency to its low state. See Table 7.

To complete a full 9.6 GHz to 40.4 GHz frequency sweep, adjust the multiplier/filter block settings six times to ensure optimum harmonic rejection and output power. These six settings are shown in Table 7.

In addition to having sleep and active modes, the 4× multipliers can be set to ready mode. Ready mode is a hybrid state between sleep and active mode. Current consumption in ready mode is higher than sleep mode but lower than active mode. The switching time between ready mode and active mode is significantly faster than from sleep mode to active mode.

1:4 SIGNAL SPLITTER NETWORK

The output of the multiplier/filter block is then applied to a 1:4 active power splitting network that is composed of two stages. The first stage is a 1:2 active splitter, which then feeds the second stage, two 1:2 active splitters. Each output path from the second stage drives a single downconverting mixer, which results in a single input signal being split into four independently controlled channels. The bias levels of each splitter stage are adjustable through the SPI via Register 0x014. See the Bias Points and Voltages section for more information.

Table 7. Multiplier/Filter Settings for Optimal LO Harmonic Rejection

LO Input Frequency (GHz)	Internal LO Frequency (GHz)	Multiplier Band	BPF	MULT_x[1] Register Value
2.40 to 3.00	9.6 to 12	Low band active (mid and high bands ready)	Low	0xFA
3.00 to 4.00	12 to 16	Low band active (mid and high bands ready)	High	0x7A
4.00 to 5.00	16 to 20	Mid band active (mid and high bands ready)	Low	0xEE
5.00 to 6.25	20 to 25	Mid band active (low and high bands ready)	High	0x6E
6.25 to 8.00	25 to 32	High band active (low and mid bands ready)	Low	0xEB
8.00 to 10.10	32 to 40.4	High band active (low and mid bands ready)	High	0x6B

[1] MULT_x refers to the MULT_EN_MODE_x and MULT_SPI registers.

RECEIVERS

There are four independent receive channels, each with fully differential inputs and outputs. Each channel includes an RF LNA front end, a downconverting mixer, and a dedicated IF VGA. The inputs operate from 10 GHz to 40 GHz and are intended to be connected to dipole antennas, whereas the outputs operate from low frequency to 800 MHz and are meant to be directly connected to an ADC. The bias levels of the LNAs, mixers, and IF VGAs are adjustable through the SPI. There is one setting for all the LNAs (LNA_BIAS in Register 0x015), one setting for the mixers (MIX_BIAS in Register 0x015), and one setting for the IF VGAs (IFAMP_BIAS in Register 0x016). The IF VGAs also have a setting for V_{OCM} (IFAMP_CM in Register 0x017). See the Bias Points and Voltages section for more information.

Although normal operation envisages all four receive channels operating at one time, the programmability allows any combination of receive channels to be turned on or off simultaneously.

TEMPERATURE SENSOR

The ADAR2004 has an on-chip temperature sensor that feeds into a dedicated 8-bit ADC for monitoring the temperature of the chip. Use the following equation to calculate the approximate temperature in Celsius from the ADC output:

$$T_A = (1.05 \times ADC\_OUTPUT) - 80$$

where *ADC_OUTPUT* is the ADC output word in Register 0x031.

ADC AND ADC CLOCK

The ADAR2004 has an on-chip, 8-bit ADC and a variable clock input, each with their own enable control bits.

To take a measurement from the ADC, first write to the ADC_CTRL register, Register 0x030. This register contains the following bits:

- Bit 0: ADC_EOC (read only). This bit is a flag for when the ADC conversion is complete.
- Bit 4: ST_CONV (read/write). This bit is set to start an ADC conversion cycle.
- Bit 5: CLK_EN (read/write). This bit enables the ADC clock.
- Bit 6: ADC_EN (read/write). This bit enables the ADC.
- Bit 7: ADC_CLKFREQ_SEL (read/write). This bit is used to set the clock frequency. A low sets the clock to 2 MHz, whereas a high sets the clock to 250 kHz.

After the ADC_CTRL register is written, it must be polled to wait for the ADC_EOC bit to go high. When the ADC_EOC bit goes high, the measured value can be read out from the ADC_OUTPUT register, Register 0x031.

APPLICATIONS INFORMATION

SPI CONTROL

The ADAR2004 is designed to operate as part of a larger array. The built in state machines help to ease the control of many chips in parallel and to ensure that the fastest switching speeds are achieved. However, it is possible to operate every aspect of the ADAR2004 using the SPI port alone. When the state machines are disabled by setting MULT_SEQ_EN (Register 0x019, Bit 7) and RX_SEQ_EN (Register 0x018, Bit 7) low, the multiplier/filter and receiver blocks respond to the SPI controlled registers (Register 0x02B to Register 0x02F), rather than stepping through the programmed states.

MULT_SPI (Register 0x02F) controls the multiplier/filter block when in SPI mode and has all the same controls as a typical multiplier/filter mode.

Register 0x02B to Register 0x02E control the receiver block when in SPI mode and have all the same controls as a typical receiver mode, as well as individual enables for the LNAs, mixers, and IF VGAs. Note that when the ADAR2004 receiver block is in SPI mode, the channel enables do not turn on the desired channel unless each piece of the receiver signal chain (LNA, mixer, IF VGA) is enabled as well, which contrasts with the sequencer modes, where a channel enable turns on the entire channel. The sequencer does not have access to the individual enables.

Operating the ADAR2004 in this manner can be thought of as a manual, rather than an automatic, approach. With the sequencers disabled, any changes to the configuration of the chip must be made through an SPI write, because pulsing any of the sequencer control pins has no effect.

STATE MACHINE MODES vs. STATES

Both the multiplier/filter state machine and the receiver state machine have 16 modes available to set the configuration of their respective subcircuitry. The sequencers also have 16 states available to cycle through.

Within each mode of the multiplier/filter state machine, the user can define the following:

- The enabled status of the RF input buffer (on or off, one bit).
- The sleep, ready, or active state of each 4× multiplier band (two bits for each band, six bits in total). The two bits control the ready and active status, and if neither bit is high, the multiplier band is set to sleep. Both bits must be high to be fully active.
- The BPF status (on or off, 1 bit for all bands).

Within each mode of the receiver state machine, the user can define the following:

- The enabled status of each receive channel (one bit for each band, four bits in total). Each bit enables the entire channel, including the respective LNA, mixer, and IF VGA.
- The enabled status of the first 1:2 signal splitter (on or off, one bit).
- The enabled status of the 1:2 signal splitter feeding the mixers on Channel 1 and Channel 2 (on or off, one bit).
- The enabled status of the 1:2 signal splitter feeding the mixers on Channel 3 and Channel 4 (on or off, one bit).
- The gain of each channel (four bits for each, 16 total).

Each multiplier/filter state is used to select an operating mode. Each state bit field contains four bits, allowing selection of any mode between 0 and 15 (Register 0x070 to Register 0x07F). There are 16 multiplier/filter states available (Register 0x022 to Register 0x029). When the multiplier/filter state machine is enabled and the sequencer depth is set, the multiplier/filter state machine cycles through the states in order, up to the defined state machine depth.

Similarly, each receiver state is used to select an operating mode. Each state bit field has four bits, allowing the selection of any mode between 0 and 15 (Register 0x040 to Register 0x06F). There are 16 receiver states available (Register 0x01A to Register 0x021). When the receiver state machine is enabled and the sequencer depth is set, the receiver state machine cycles through the states in order, up to the defined state machine depth.

Figure 42 shows how the state machine pointer moves through a loop. In this diagram, n is the total number of states inside the loop. Because the sequencer depth bit field is 0 indexed, n is equal to one more than the value in the sequencer depth bit field.

$$n = MULT\_STATES + 1$$

where:
n = 1 to 16.
$MULT\_STATES$ is the multiplier sequencer depth.

$$n = RX\_STATES + 1$$

where:
n = 1 to 16.
RX_STATES is the receiver sequence depth.

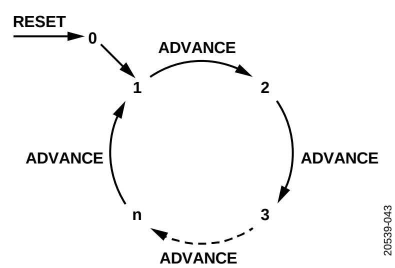


Figure 42. State Machine Position Loop

STATE MACHINE SETUP

Both state machines in the ADAR2004 have configuration registers that control various aspects of the state machine.

For the multiplier/filter sequencer, this register is Register 0x019 and contains the following bits:

- Bits 0 to Bit 3: MULT_STATES. These bits set the number of states in the loop (see Figure 42).

- Bit 4: MULT_CTL_LATCH_BYP. This bit bypasses the latch on MADV and MRST. If the latch is enabled, the next state is loaded up on the rising edge of a MRST or MADV pulse. The state is then latched to the device on the falling edge of the same pulse. If the latch is bypassed, everything is applied as soon as possible after the rising edge of the pulse, with no latching.
- Bit 5: MULT_SLP_HOLD. This bit prevents the multiplier/filter block from advancing when forced into a sleep state by the receiver block. This bit is used in conjunction with RX_SLP_CTRL (Register 0x018, Bit 6). See the Sequencer Sleep Hold section for more information.
- Bit 6: MULT_SLP_CTRL. This bit forces the multiplier/filter block to sleep whenever the receiver block is sleeping. See the Sequencer Sleep Control section for more information.
- Bit 7: MULT_SEQ_EN. This bit enables the multiplier/filter block. This bit must be set high for the block to operate with the external pins.

For the receiver sequencer, the control register is Register 0x018 and contains the following bits:

- Bit 0 to Bit 3: RX_STATES. These bits set the number of states in the loop (see Figure 42).
- Bit 4: RX_CTL_LATCH_BYP. This bit bypasses the latch on RxADV and RxRST. If the latch is enabled, the next state is loaded up on the rising edge of an RxRST or RxADV pulse. The state is then latched to the device on the falling edge of the same pulse. If the latch is bypassed, everything is applied as soon as possible after the rising edge of the pulse, with no latching.
- Bit 5: RX_SLP_HOLD. This bit prevents the receiver block from advancing when forced into a sleep state by the multiplier/filter block. This bit is used in conjunction with MULT_SLP_CTRL (Register 0x019, Bit 6). See the Sequencer Sleep Hold section for more information.
- Bit 6: RX_SLP_CTRL. This bit forces the receiver block to sleep whenever the multiplier/filter block is sleeping. See the Sequencer Sleep Control section for more information.
- Bit 7: RX_SEQ_EN. This bit enables the receiver block. This bit must be set high for the block to operate with the external pins.

MULTIPLIER/FILTER STATE MACHINE

A programmable state machine provides a convenient and fast control mechanism for the multiplier/filter block and avoids the need for SPI writes each time the block must be reconfigured.

To enable the state machine, set the MULT_SEQ_EN bit (Register 0x019, Bit 7) high.

Although only six multiplier/filter modes are required for a complete 9.6 GHz to 40.4 GHz sweep, as described in Table 7, a maximum state machine depth of 16 is provided for optimum flexibility.

Eight default modes can be assigned to any of the 16 states. These eight modes consist of a sleep mode, a ready mode, and the six modes required to complete a 9.6 GHz to 40.4 GHz sweep, as described in Table 7. It is possible to overwrite any of the multiplier/filter modes with a custom set of operating conditions by changing the bits in Register 0x070 to Register 0x07F.

After the modes are defined, set the order in which the sequencer moves through the desired modes by filling the state bits in Register 0x022 to Register 0x029 in order with the modes of interest. Any state can point to any mode, except State 0, which always points to Mode 0. Note that the sequencer moves through the states in order, up to the state machine depth.

Finally, the user must define how many states are used by setting the state machine depth (MULT_STATES, Register 0x019, Bits[3:0]). MULT_STATES is 0 indexed. Therefore, setting the depth to 0 leaves MULT_STATE_1 (Register 0x022, Bits[7:4]) as the only state in the loop.

After the multiplier/filter state machine is programmed and enabled, operation is controlled by the MRST and MADV pins. Alternatively, operation can be controlled through the SPI using the MULT_RST_SPI and MULT_ADV_SPI bits (Register 0x02A, Bit 3 and Bit 2, respectively). Note that using the SPI is slower than pulsing the sequencer pins directly.

MRST moves the pointer on the multiplier/filter state machine to State 0 regardless of the current position of the pointer and can be asserted at any time. State 0 always refers to Mode 0 and cannot be set to another mode. However, Mode 0 can be overwritten with any multiplier/filter configuration. Mode 0 is defined in Register 0x070.

MADV pulses advance the multiplier/filter state machine pointer one state at a time until the defined sequencer depth is cycled through. At that point, an additional MADV pulse moves the pointer back to State 1, which is normally set to a ready mode (however, State 1 can be set to any mode). State 1 applies the mode defined in the MULT_STATE_1 bits (Register 0x022, Bits[7:4]).

RECEIVER STATE MACHINE

Like the multiplier/filter state machine, the receiver state machine can be used to quickly cycle through receiver states without using the comparatively slower SPI.

To enable the state machine, set the RX_SEQ_EN bit (Register 0x018, Bit 7) high.

The receiver state machine controls the status of the four receive channels (each with an LNA, mixer, and IF VGA) and the status of the 1:4 splitter network by defining the desired modes of operation in Register 0x040 to Register 0x06F. Each mode outlines a custom set of operating conditions.

Although only one active state is required to enable all receive channels, a state machine depth of 16 is provided for optimum flexibility of the receiver sequencer and to lower the total number of control lines required to operate multiple ADAR2004 chips in parallel. It is possible to control up to 16 ADAR2004 ICs using the same four sequencer lines (MADV, MRST, RxADV, RxRST). See the Parallel Chip Control section for more information.

Following the mode definitions, the user must fill the state bits in Register 0x01A to Register 0x021 with the modes of interest. Any state can point to any mode, except State 0, which always points to Mode 0. Note that the sequencer moves through the states in order, up to the state machine depth.

After defining the states, the user must set the number of states to be used by the sequencer by changing the RX_STATES bits (Register 0x018, Bits[3:0]). RX_STATES is 0 indexed. Therefore, setting the depth to 0 leaves RX_STATE_1 as the only state in the loop.

After the multiplier/filter state machine is programmed and enabled, operation is controlled by the RxRST and RxADV pins. Alternatively, operation can be controlled through the SPI using the RX_RST_SPI and RX_ADV_SPI bits (Register 0x02A, Bits[1:0]). Note that using the SPI is slower than pulsing the sequencer pins directly.

RxRST moves the pointer on the receiver state machine to State 0 regardless of the current position of the pointer and can be asserted at any time. State 0 always refers to Mode 0 and cannot be set to another mode. However, Mode 0 can be overwritten with any receiver configuration. Mode 0 is defined in Register 0x040, Register 0x041, and Register 0x042.

RxADV pulses advance the receiver state machine pointer one state at a time until the defined sequencer depth is cycled through. At that point, an additional RxADV pulse moves the pointer back to State 1. State 1 applies the mode defined in the RX_STATE_1 bits (Register 0x01A, Bits[7:4]).

FREQUENCY SWEEP ALL CHANNELS

Figure 43 shows a method of operation that can be used during a 20 GHz to 40 GHz frequency sweep of all receive channels. As described in Table 7, three multiplier/filter states are required during a 20 GHz to 40 GHz sweep. In this example, the defined state machine depth, MULT_STATES (Register 0x019, Bits[3:0]), is 3 because there are four states inside the loop, and MULT_STATES is 0 indexed.

As shown in Figure 43,

- Multiplier/Filter State 0 = sleep (outside the loop)
- Multiplier/Filter State 1 = mid band multiplier ready
- Multiplier/Filter State 2 = output 20 GHz to 25 GHz to mixers
- Multiplier/Filter State 3 = output 25 GHz to 30 GHz to mixers
- Multiplier/Filter State 4 = output 30 GHz to 40 GHz to mixers

The initial state is the sleep state where power consumption is at a minimum. A pulse on MADV advances the state machine to the second state, which is defined as a ready state. By partially powering up the mid band multiplier with its BPF set high, an additional pulse on MADV makes this subcircuit path active in under 10 ns. By making use of the ready mode throughout the sweep, the settling time can be kept under 10 ns.

After the appropriate number of pulses is applied to MADV (4, in this case), the state machine automatically returns to the second state (ready mode).

SEQUENCER SLEEP CONTROL

To further simplify the control of the ADAR2004, it is possible to link the sleep states of the two state machines so that one sequencer going to sleep forces the other sequencer to sleep as well. This link helps to limit the total number of required states to achieve the desired type of operation. To use this feature, one of the two sleep control bits must be set, but not both.

For example, when the ADAR2004 is configured for a frequency sweep (as shown in Figure 43), if the RX_SLP_CTRL bit (Register 0x018, Bit 6) is set, when the multiplier/filter sequencer is reset, the receiver state machine is forced to sleep as well. This means that the receiver state machine does not require a state dedicated to sleep if it only needs to sleep when the multiplier/filter sleeps. Furthermore, because the multiplier/filter sleep state is controlling the sleep state of the receiver, bringing the multiplier/filter out of sleep also brings the receiver out of sleep. This routine is controlled with either the SPI or one external line (MADV).

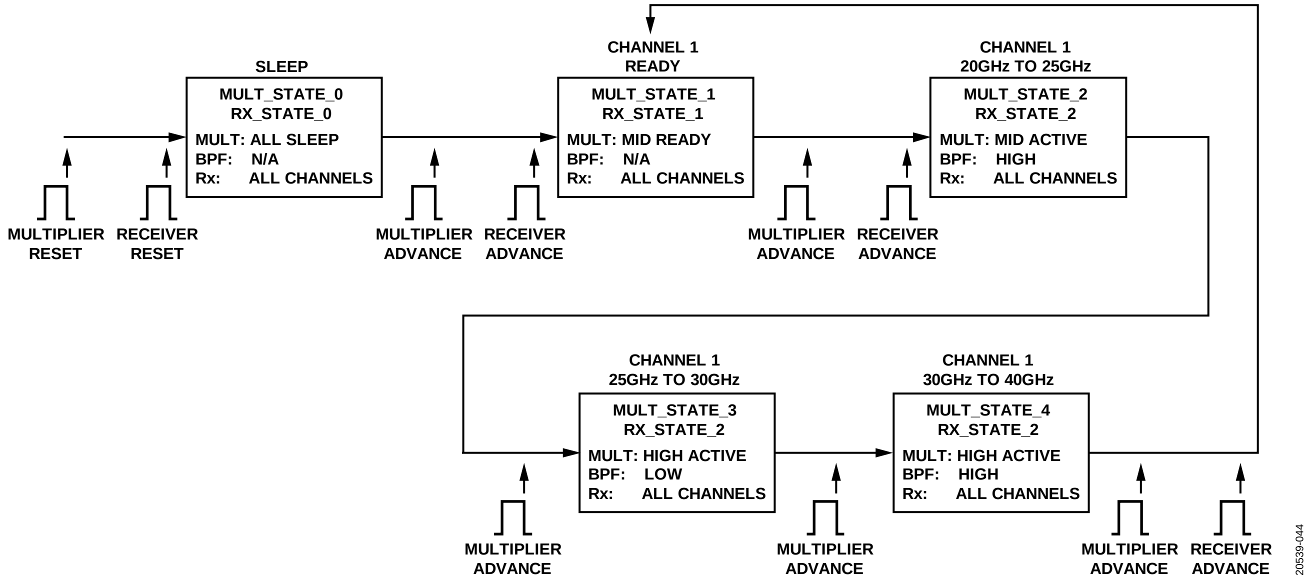


Figure 43. Multiplier State Machine Operating Example for a Frequency Sweep of All Receiver Channels Simultaneously From 20 GHz to 40 GHz (N/A Means Not Applicable)

SEQUENCER SLEEP HOLD

By default, when one of the sequencers is forced asleep using one of the sleep control bits (MULT_SLP_CTRL or RX_SLP_CTRL), the counter for the sequencer being controlled can still be advanced. Because of this behavior, it is possible for a state machine to be put to sleep in one condition and brought out of sleep in another, depending on whether the sequencer advance or reset signals were exercised while the sequencer was sleeping.

If this behavior is undesired, the sleep hold bits (MULT_SLP_HOLD and RX_SLP_HOLD) can be asserted to force the associated state machine counter to ignore any inputs on the sequencer advance line. The counter also ignores advance signals coming from the SPI.

Note that the counter always responds to a reset signal, even when the sleep hold bit is high.

When sleep hold is used, take care when bringing the state machines out of sleep mode to ensure that the desired modes are reached. If the advance pins for both sequencers are pulsed too closely together under this condition, it is possible for the sequencer being controlled to not move into the expected state. To prevent this issue, stagger the advance pulses so that the rising edges are separated by a minimum of 3 ns with the pulse of the controlled sequencer coming second. See Figure 44 for an example of how to pulse the sequencers under this condition.

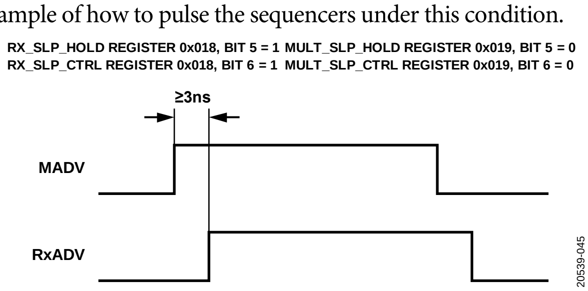


Figure 44. Example of How to Pulse the Sequencer Advance Pins to Ensure Advancement With Receiver State Machine Sleep Hold Enabled

SEQUENCER CONTROL LATCH BYPASS

Typically, when a sequencer control line is pulsed, the upcoming state is loaded on the rising edge of the control pulse and latched to the various signal blocks on the falling edge of the same pulse. The latching helps to line up all the internal control signals so that the changes take place simultaneously.

It is possible to bypass the latching of the internal control signals by setting the bypass bits (RX_CTL_LATCH_BYP and MULT_CTL_LATCH_BYP) in the sequencer setup registers (Register 0x018, Bit 4 and Register 0x019, Bit 4).

Bypassing the latch results in the new state taking effect as soon as possible after the rising edge. Because the internal control signals are not aligned, it is possible that the overall switching time between states increases when compared to using the latch. Also, glitches are more likely to occur in the internal control signals, resulting in undesired transients in the RF blocks.

Note that this latch is the last check before any new data is sent to the various individual blocks. Therefore, when using the ADAR2004 in manual or SPI mode (sequencers disabled), the latching must be bypassed. If the latching is not bypassed, the blocks do not receive the new instructions unless the external sequencer pins are pulsed. However, this issue is uncommon because the sequencers are disabled in this mode of operation.

PARALLEL CHIP CONTROL

Up to 16 devices (a total of 64 channels) can be driven by a single set of four state machine control lines, three common SPI lines, and a $\overline{CS}$ line for each chip. Using this method, the total number of digital control lines is 7 + N, where N is the number of ADAR2004 ICs (see Figure 45 for a basic diagram). Parallel chip control can be used to minimize the total number of digital control lines. The SPI lines can be reduced to two common lines if 3-wire mode is selected by setting the SDOACTIVE and SDOACTIVE_ bits (Register 0x000, Bit 4 and Bit 3, respectively) low. If 3-wire SPI mode is used, the total number of digital lines is 6 + N.

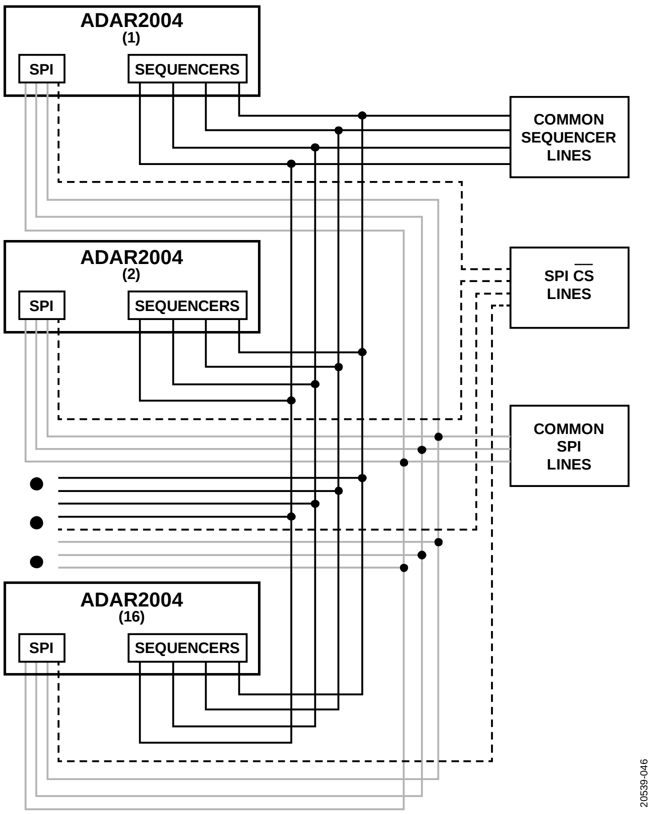


Figure 45. SPI and State Machine Digital Lines For Addressing and Controlling Up to 16 ADAR2004 Devices

MULTICHIP FREQUENCY SWEEP

Figure 46 shows an example of how the two state machines can be used to complete a multichip frequency sweep from 10 GHz to 16 GHz (that is, receive on all four channels on a single chip while at a fixed frequency range, move to the next chip and receive on all channels, moving through 16 chips in total, and then move to the next frequency and repeat the process). This example assumes that the state machine control lines are connected in parallel for up to 16 devices (64 channels, see Figure 45).

Initially, pulses on RxRST and MRST put both state machines in State 0, which in this case, is a sleep mode.

Next, pulses on MADV and RxADV advance both state machines to their first active state (receiving on all channels of ADAR2004 IC 1).

After ADAR2004 IC 1 receives the signal, an additional pulse on RxADV activates all channels on ADAR2004 IC 2 while putting the multiplier/filter of the first chip into a ready mode and the receivers of that chip into a sleep mode to prevent disrupting the multiplier/filter signal before the receiver turns off. This sequence continues until all 16 ADAR2004 devices receive at the first frequency or range.

At that point, a pulse is applied to both MADV and RxADV to advance the multiplier/filter to the next frequency range of interest and set the ADAR2004 IC 1 back into an active mode. Another series of RxADV pulses follow until ADAR2004 IC 16 is receiving the new frequency range.

Table 8 describes how the receiver state machine for each ADAR2004 can be set up to work in sequence. Each device is turned fully on for only one state, but these states are all offset from each other. To run this sequence, where up to 16 devices are swept with all state machines driven in parallel, 16 receive states are used inside the loop, with the sleep state (State 0) used as a reset condition.

If there were more tiles of 16 chips in the array that need to receive after the tile described in Table 8, this tile can have a reset pulse sent to put the sequencers into the initial sleep mode to wait for their turn to receive again.

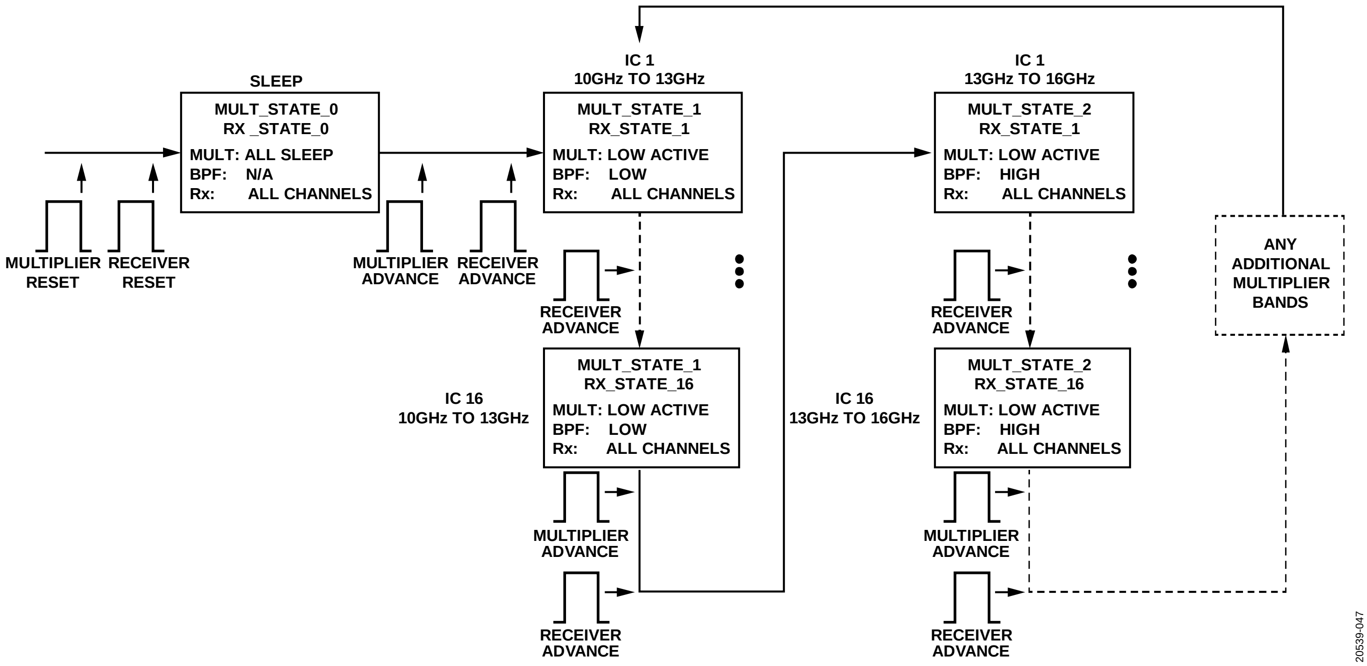


Figure 46. State Machine Loop Example For a 16-Chip Frequency Sweep (N/A Means Not Applicable)

Table 8. Receiver Sequencer Settings for Controlling 16 ADAR2004 Devices In Parallel[1]

	ADAR2004 Chip Number																
Rx State	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**Function**
0 (Reset)	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All sleep
1	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 1 receiving
2	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 2 receiving
3	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 3 receiving
4	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 4 receiving
5	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 5 receiving
6	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 6 receiving
7	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 7 receiving
8	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 8 receiving
9	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 9 receiving
10	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	SLP	Chip 10 receiving
11	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	SLP	Chip 11 receiving
12	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	SLP	Chip 12 receiving
13	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	SLP	Chip 13 receiving
14	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	SLP	Chip 14 receiving
15	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	SLP	Chip 15 receiving
16	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All	Chip 16 receiving

[1] SLP is the sleep state (State 0)

BIAS POINTS AND VOLTAGES

Table 9. Default Bias Points

Register Address	Register Name	Bit Field Name(s)	Register Bit(s)	Default Value	Description
0x011	BIAS_CURRENT_MULT1			0x55	Low and mid band multiplier bias current
		MULT_LOW_BIAS	[3:0]	0x5	Low band multiplier bias current
		MULT_MID_BIAS	[7:4]	0x5	Mid band multiplier bias current
0x012	BIAS_CURRENT_MULT2			0x07	High band multiplier bias current
		MULT_HIGH_BIAS	[3:0]	0x7	High band multiplier bias current
0x013	BIAS_CURRENT_LOAMP			0x78	LO buffer amplifier bias current
		LO_AMP1_BIAS	[3:0]	0x08	LO buffer input stage bias current
		LO_AMP2_BIAS	[7:4]	0x07	LO buffer output stage bias current
0x014	BIAS_CURRENT_SPLT			0x7A	Active splitter bias current
		SPLT1_BIAS	[3:0]	0xA	First stage active splitter bias current
		SPLT2_BIAS	[7:4]	0x7	Second stage active splitter bias current
0x015	BIAS_CURRENT_LNAMIX			0x2A	LNA and mixer bias current
		LNA_BIAS	[3:0]	0xA	LNA bias current
		MIX_BIAS	[7:4]	0x2	Mixer bias current
0x016	BIAS_CURRENT_IFAMP			0xC0	IF amplifier bias current
		IFAMP_BIAS	[7:4]	0xC	IF amplifier bias current
0x017	IFAMP_CM			0x04	IF amplifier output common-mode voltage
		IFAMP_CM	[3:0]	0x4	IF amplifier output common-mode voltage

REGISTER SUMMARY

Table 10. ADAR2004 Register Summary

Address	Name	Bits	Bit Name	Description	Reset	Access
0x000	INTERFACE_CONFIG_A	7	SOFTRESET	Soft Reset	0x0	R/W
		6	LSB_FIRST	LSB First	0x0	R/W
		5	ADDR_ASCN	Address Ascension	0x0	R/W
		4	SDOACTIVE	SDO Active	0x1	R/W
		3	SDOACTIVE_	SDO Active	0x1	R/W
		2	ADDR_ASCN_	Address Ascension	0x0	R/W
		1	LSB_FIRST_	LSB First	0x0	R/W
		0	SOFTRESET_	Soft Reset	0x0	R/W
0x001	INTERFACE_CONFIG_B	7	SINGLE_INSTRUCTION	Single Instruction	0x0	R/W
		6	$\overline{\text{CS}}$_STALL	$\overline{\text{CS}}$ Stall	0x0	R/W
		5	MASTER_SLAVE_RB	Master Slave Readback	0x0	R/W
		4	SLOW_INTERFACE_CTRL	Slow Interface Control	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:1]	SOFT_RESET	Soft Reset	0x0	R/W
		0	RESERVED	Reserved	0x0	R
0x002	DEV_CONFIG	[7:4]	DEV_STATUS	Device Status	0x1	R/W
		[3:2]	CUST_OPERATING_MODE	Custom Operating Modes	0x0	R/W
		[1:0]	NORM_OPERATING_MODE	Normal Operating Modes	0x0	R/W
0x003	CHIP_TYPE	[7:0]	CHIP_TYPE	Chip Type	0x0	R
0x004	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]	Product ID High	0x0	R
0x005	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]	Product ID Low	0x0	R
0x00A	SCRATCH_PAD	[7:0]	SCRATCHPAD	Scratch Pad	0x0	R/W
0x00B	SPI_REV	[7:0]	SPI_REV	SPI Revision	0x0	R
0x00C	VENDOR_ID_H	[7:0]	VENDOR_ID[15:8]	Vendor ID High	0x0	R
0x00D	VENDOR_ID_L	[7:0]	VENDOR_ID[7:0]	Vendor ID Low	0x0	R
0x00F	TRANSFER_REG	[7:1]	RESERVED	Reserved	0x0	R
		0	MASTER_SLAVE_XFER	Master Slave Transfer	0x0	R/W
0x010	PWRON	[7:1]	RESERVED	Reserved	0x0	R
		0	PWRON	Chip Power-Up	0x1	R/W
0x011	BIAS_CURRENT_MULT1	[7:4]	MULT_MID_BIAS	Mid Band 4× Bias Current Setting	0x5	R/W
		[3:0]	MULT_LOW_BIAS	Low Band 4× Bias Current Setting	0x5	R/W
0x012	BIAS_CURRENT_MULT2	[7:4]	RESERVED	Reserved	0x0	R/W
		[3:0]	MULT_HIGH_BIAS	High Band 4× Bias Current Setting	0x7	R/W
0x013	BIAS_CURRENT_LOAMP	[7:4]	LO_AMP2_BIAS	LO Amp Output Stage Bias Current Setting	0x7	R/W
		[3:0]	LO_AMP1_BIAS	LO Amp Input Stage Bias Current Setting	0x8	R/W
0x014	BIAS_CURRENT_SPLT	[7:4]	SPLT2_BIAS	Second Active Splitter Stages Bias Current Setting	0x7	R/W
		[3:0]	SPLT1_BIAS	First Active Splitter Stage Bias Current Setting	0xA	R/W
0x015	BIAS_CURRENT_LNAMIX	[7:4]	MIX_BIAS	Mixer Bias Current Setting	0x2	R/W
		[3:0]	LNA_BIAS	LNA Bias Current Setting	0xA	R/W
0x016	BIAS_CURRENT_IFAMP	[7:4]	IFAMP_BIAS	IF Output Amp Bias Current Setting	0xC	R/W
		[3:0]	RESERVED	Reserved	0x0	R/W
0x017	IFAMP_CM	[7:4]	RESERVED	Reserved	0x0	R
		[3:0]	IFAMP_CM	IF Output Amp Common-Mode Voltage Setting	0x4	R/W
0x018	RX_SEQUENCER_SETUP	7	RX_SEQ_EN	Enables Receiver Sequencer	0x0	R/W
		6	RX_SLP_CTRL	Sets Receiver Sleep Mode Control	0x0	R/W
		5	RX_SLP_HOLD	Holds the Receiver Sequencer State When Multiplier Is in Sleep Mode	0x0	R/W
		4	RX_CTL_LATCH_BYP	Bypasses the Control Latch for Receiver Controls	0x1	R/W
		[3:0]	RX_STATES	Sets Number of Receiver Sequencer States	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x019	MULT_SEQUENCER_SETUP	7	MULT_SEQ_EN	Enables Frequency Sequencer	0x0	R/W
		6	MULT_SLP_CTRL	Sets Multiplier Sleep Mode Control	0x0	R/W
		5	MULT_SLP_HOLD	Holds the Multiplier Sequencer State When Receiver Is in Sleep Mode	0x0	R/W
		4	MULT_CTL_LATCH_BYP	Bypasses the Control Latch for Multiplier Controls	0x1	R/W
		[3:0]	MULT_STATES	Sets Number of Multiplier/Filter Sequencer States	0x0	R/W
0x01A	RX_STATES_1_2	[7:4]	RX_STATE_1	Mode Select for Receiver Sequencer State 1	0x0	R/W
		[3:0]	RX_STATE_2	Mode Select for Receiver Sequencer State 2	0x0	R/W
0x01B	RX_STATES_3_4	[7:4]	RX_STATE_3	Mode Select for Receiver Sequencer State 3	0x0	R/W
		[3:0]	RX_STATE_4	Mode Select for Receiver Sequencer State 4	0x0	R/W
0x01C	RX_STATES_5_6	[7:4]	RX_STATE_5	Mode Select for Receiver Sequencer State 5	0x0	R/W
		[3:0]	RX_STATE_6	Mode Select for Receiver Sequencer State 6	0x0	R/W
0x01D	RX_STATES_7_8	[7:4]	RX_STATE_7	Mode Select for Receiver Sequencer State 7	0x0	R/W
		[3:0]	RX_STATE_8	Mode Select for Receiver Sequencer State 8	0x0	R/W
0x01E	RX_STATES_9_10	[7:4]	RX_STATE_9	Mode Select for Receiver Sequencer State 9	0x0	R/W
		[3:0]	RX_STATE_10	Mode Select for Receiver Sequencer State 10	0x0	R/W
0x01F	RX_STATES_11_12	[7:4]	RX_STATE_11	Mode Select for Receiver Sequencer State 11	0x0	R/W
		[3:0]	RX_STATE_12	Mode Select for Receiver Sequencer State 12	0x0	R/W
0x020	RX_STATES_13_14	[7:4]	RX_STATE_13	Mode Select for Receiver Sequencer State 13	0x0	R/W
		[3:0]	RX_STATE_14	Mode Select for Receiver Sequencer State 14	0x0	R/W
0x021	RX_STATES_15_16	[7:4]	RX_STATE_15	Mode Select for Receiver Sequencer State 15	0x0	R/W
		[3:0]	RX_STATE_16	Mode Select for Receiver Sequencer State 16	0x0	R/W
0x022	MULT_STATES_1_2	[7:4]	MULT_STATE_1	Mode Select for Multiplier Sequencer State 1	0x0	R/W
		[3:0]	MULT_STATE_2	Mode Select for Multiplier Sequencer State 2	0x0	R/W
0x023	MULT_STATES_3_4	[7:4]	MULT_STATE_3	Mode Select for Multiplier Sequencer State 3	0x0	R/W
		[3:0]	MULT_STATE_4	Mode Select for Multiplier Sequencer State 4	0x0	R/W
0x024	MULT_STATES_5_6	[7:4]	MULT_STATE_5	Mode Select for Multiplier Sequencer State 5	0x0	R/W
		[3:0]	MULT_STATE_6	Mode Select for Multiplier Sequencer State 6	0x0	R/W
0x025	MULT_STATES_7_8	[7:4]	MULT_STATE_7	Mode Select for Multiplier Sequencer State 7	0x0	R/W
		[3:0]	MULT_STATE_8	Mode Select for Multiplier Sequencer State 8	0x0	R/W
0x026	MULT_STATES_9_10	[7:4]	MULT_STATE_9	Mode Select for Multiplier Sequencer State 9	0x0	R/W
		[3:0]	MULT_STATE_10	Mode Select for Multiplier Sequencer State 10	0x0	R/W
0x027	MULT_STATES_11_12	[7:4]	MULT_STATE_11	Mode Select for Multiplier Sequencer State 11	0x0	R/W
		[3:0]	MULT_STATE_12	Mode Select for Multiplier Sequencer State 12	0x0	R/W
0x028	MULT_STATES_13_14	[7:4]	MULT_STATE_13	Mode Select for Multiplier Sequencer State 13	0x0	R/W
		[3:0]	MULT_STATE_14	Mode Select for Multiplier Sequencer State 14	0x0	R/W
0x029	MULT_STATES_15_16	[7:4]	MULT_STATE_15	Mode Select for Multiplier Sequencer State 15	0x0	R/W
		[3:0]	MULT_STATE_16	Mode Select for Multiplier Sequencer State 16	0x0	R/W
0x02A	SEQUENCER_CTRL_SPI	[7:4]	RESERVED	Reserved	0x0	R
		3	MULT_RST_SPI	Resets Frequency Sequencer	0x0	R/W
		2	MULT_ADV_SPI	Advances Multiplier Sequencer State	0x0	R/W
		1	RX_RST_SPI	Resets Receiver Sequencer	0x0	R/W
		0	RX_ADV_SPI	Advances Receiver Sequencer State	0x0	R/W
0x02B	RX_EN_SPI	7	LNA_EN_SPI	SPI Mode LNA Enable	0x0	R/W
		6	MIX_EN_SPI	SPI Mode Mixer Enable	0x0	R/W
		5	IFAMP_EN_SPI	SPI Mode IF Amp Enable	0x0	R/W
		4	RESERVED	Reserved	0x0	R/W
		3	CH1_EN_SPI	SPI Mode Channel 1 Enable	0x0	R/W
		2	CH2_EN_SPI	SPI Mode Channel 2 Enable	0x0	R/W
		1	CH3_EN_SPI	SPI Mode Channel 3 Enable	0x0	R/W
		0	CH4_EN_SPI	SPI Mode Channel 4 Enable	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x02C	RX_GAIN12_SPI	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_SPI	SPI Mode Channel 1 Gain Setting	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_SPI	SPI Mode Channel 2 Gain Setting	0x0	R/W
0x02D	RX_GAIN34_SPI	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_SPI	SPI Mode Channel 3 Gain Setting	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_SPI	SPI Mode Channel 4 Gain Setting	0x0	R/W
0x02E	SPLT_EN_SPI	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_SPI	SPI Mode Active Splitter 1 Enable	0x0	R/W
		1	SPLT12_EN_SPI	SPI Mode Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		0	SPLT34_EN_SPI	SPI Mode Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
0x02F	MULT_SPI	7	BPF_SPI	SPI Mode BPF Select	0x0	R/W
		6	LOAMP_EN_SPI	SPI Mode LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_SPI	SPI Mode Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_SPI	SPI Mode Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_SPI	SPI Mode Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_SPI	SPI Mode Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_SPI	SPI Mode High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_SPI	SPI Mode High Band Active Enable	0x0	R/W
0x030	ADC_CTRL	7	ADC_CLKFREQ_SEL	ADC Clock Frequency Selection	0x0	R/W
		6	ADC_EN	Turns on Comparator and Resets State Machine	0x0	R/W
		5	CLK_EN	Turns on Clock Oscillator	0x0	R/W
		4	ST_CONV	Pulse Triggers Conversion Cycle	0x0	R/W
		[3:1]	RESERVED	Reserved	0x0	R/W
		0	ADC_EOC	ADC End of Conversion Signal	0x0	R
0x031	ADC_OUTPUT	[7:0]	ADC	ADC Output Word	0x0	R
0x032	RX_STATUS	[7:4]	RX_CURR_STATE	Read Back Current Receiver Sequencer Count	0x0	R
		[3:0]	RX_CURR_MODE	Read Back Current Receiver Mode	0x0	R
0x033	MULT_STATUS	[7:4]	MULT_CURR_STATE	Read Back Current Multiplier/Filter Sequencer Count	0x0	R
		[3:0]	MULT_CURR_MODE	Read Back Current Mode	0x0	R
0x034	REV_ID	[7:0]	REV_ID	Chip Revision ID	0x0	R
0x040	RX_EN_MODE_0	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD0	Receiver Mode 0 Active Splitter 1 Enable	0x0	R/W
		5	SPLT12_EN_MD0	Receiver Mode 0 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD0	Receiver Mode 0 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD0	Receiver Mode 0 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD0	Receiver Mode 0 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD0	Receiver Mode 0 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD0	Receiver Mode 0 Channel 4 Enable	0x0	R/W
0x041	RX_GAIN12_MODE_0	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD0	Receiver Mode 0 Channel 1 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD0	Receiver Mode 0 Channel 2 Gain	0x0	R/W
0x042	RX_GAIN34_MODE_0	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD0	Receiver Mode 0 Channel 3 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD0	Receiver Mode 0 Channel 4 Gain	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x043	RX_EN_MODE_1	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD1	Receiver Mode 1 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD1	Receiver Mode 1 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD1	Receiver Mode 1 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD1	Receiver Mode 1 Channel 1 Enable	0x1	R/W
		2	CH2_EN_MD1	Receiver Mode 1 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD1	Receiver Mode 1 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD1	Receiver Mode 1 Channel 4 Enable	0x0	R/W
0x044	RX_GAIN12_MODE_1	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD1	Receiver Mode 1 Channel 1 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD1	Receiver Mode 1 Channel 2 Gain	0x7	R/W
0x045	RX_GAIN34_MODE_1	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD1	Receiver Mode 1 Channel 3 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD1	Receiver Mode 1 Channel 4 Gain	0x7	R/W
0x046	RX_EN_MODE_2	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD2	Receiver Mode 2 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD2	Receiver Mode 2 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD2	Receiver Mode 2 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD2	Receiver Mode 2 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD2	Receiver Mode 2 Channel 2 Enable	0x1	R/W
		1	CH3_EN_MD2	Receiver Mode 2 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD2	Receiver Mode 2 Channel 4 Enable	0x0	R/W
0x047	RX_GAIN12_MODE_2	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD2	Receiver Mode 2 Channel 1 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD2	Receiver Mode 2 Channel 2 Gain	0x7	R/W
0x048	RX_GAIN34_MODE_2	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD2	Receiver Mode 2 Channel 3 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD2	Receiver Mode 2 Channel 4 Gain	0x7	R/W
0x049	RX_EN_MODE_3	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD3	Receiver Mode 3 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD3	Receiver Mode 3 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD3	Receiver Mode 3 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD3	Receiver Mode 3 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD3	Receiver Mode 3 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD3	Receiver Mode 3 Channel 3 Enable	0x1	R/W
		0	CH4_EN_MD3	Receiver Mode 3 Channel 4 Enable	0x0	R/W
0x04A	RX_GAIN12_MODE_3	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD3	Receiver Mode 3 Channel 1 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD3	Receiver Mode 3 Channel 2 Gain	0x7	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x04B	RX_GAIN34_MODE_3	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD3	Receiver Mode 3 Channel 3 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD3	Receiver Mode 3 Channel 4 Gain	0x7	R/W
0x04C	RX_EN_MODE_4	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD4	Receiver Mode 4 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD4	Receiver Mode 4 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD4	Receiver Mode 4 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD4	Receiver Mode 4 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD4	Receiver Mode 4 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD4	Receiver Mode 4 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD4	Receiver Mode 4 Channel 4 Enable	0x1	R/W
0x04D	RX_GAIN12_MODE_4	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD4	Receiver Mode 4 Channel 1 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD4	Receiver Mode 4 Channel 2 Gain	0x7	R/W
0x04E	RX_GAIN34_MODE_4	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD4	Receiver Mode 4 Channel 3 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD4	Receiver Mode 4 Channel 4 Gain	0x7	R/W
0x04F	RX_EN_MODE_5	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD5	Receiver Mode 5 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD5	Receiver Mode 5 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD5	Receiver Mode 5 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD5	Receiver Mode 5 Channel 1 Enable	0x1	R/W
		2	CH2_EN_MD5	Receiver Mode 5 Channel 2 Enable	0x1	R/W
		1	CH3_EN_MD5	Receiver Mode 5 Channel 3 Enable	0x1	R/W
		0	CH4_EN_MD5	Receiver Mode 5 Channel 4 Enable	0x1	R/W
0x050	RX_GAIN12_MODE_5	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD5	Receiver Mode 5 Channel 1 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD5	Receiver Mode 5 Channel 2 Gain	0x7	R/W
0x051	RX_GAIN34_MODE_5	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD5	Receiver Mode 5 Channel 3 Gain	0x7	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD5	Receiver Mode 5 Channel 4 Gain	0x7	R/W
0x052	RX_EN_MODE_6	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD6	Receiver Mode 6 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD6	Receiver Mode 6 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD6	Receiver Mode 6 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD6	Receiver Mode 6 Channel 1 Enable	0x1	R/W
		2	CH2_EN_MD6	Receiver Mode 6 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD6	Receiver Mode 6 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD6	Receiver Mode 6 Channel 4 Enable	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x053	RX_GAIN12_MODE_6	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD6	Receiver Mode 6 Channel 1 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD6	Receiver Mode 6 Channel 2 Gain	0x4	R/W
0x054	RX_GAIN34_MODE_6	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD6	Receiver Mode 6 Channel 3 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD6	Receiver Mode 6 Channel 4 Gain	0x4	R/W
0x055	RX_EN_MODE_7	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD7	Receiver Mode 7 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD7	Receiver Mode 7 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD7	Receiver Mode 7 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD7	Receiver Mode 7 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD7	Receiver Mode 7 Channel 2 Enable	0x1	R/W
		1	CH3_EN_MD7	Receiver Mode 7 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD7	Receiver Mode 7 Channel 4 Enable	0x0	R/W
0x056	RX_GAIN12_MODE_7	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD7	Receiver Mode 7 Channel 1 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD7	Receiver Mode 7 Channel 2 Gain	0x4	R/W
0x057	RX_GAIN34_MODE_7	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD7	Receiver Mode 7 Channel 3 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD7	Receiver Mode 7 Channel 4 Gain	0x4	R/W
0x058	RX_EN_MODE_8	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD8	Receiver Mode 8 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD8	Receiver Mode 8 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD8	Receiver Mode 8 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD8	Receiver Mode 8 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD8	Receiver Mode 8 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD8	Receiver Mode 8 Channel 3 Enable	0x1	R/W
		0	CH4_EN_MD8	Receiver Mode 8 Channel 4 Enable	0x0	R/W
0x059	RX_GAIN12_MODE_8	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD8	Receiver Mode 8 Channel 1 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD8	Receiver Mode 8 Channel 2 Gain	0x4	R/W
0x05A	RX_GAIN34_MODE_8	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD8	Receiver Mode 8 Channel 3 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD8	Receiver Mode 8 Channel 4 Gain	0x4	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x05B	RX_EN_MODE_9	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD9	Receiver Mode 9 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD9	Receiver Mode 9 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD9	Receiver Mode 9 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD9	Receiver Mode 9 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD9	Receiver Mode 9 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD9	Receiver Mode 9 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD9	Receiver Mode 9 Channel 4 Enable	0x1	R/W
0x05C	RX_GAIN12_MODE_9	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD9	Receiver Mode 9 Channel 1 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD9	Receiver Mode 9 Channel 2 Gain	0x4	R/W
0x05D	RX_GAIN34_MODE_9	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD9	Receiver Mode 9 Channel 3 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD9	Receiver Mode 9 Channel 4 Gain	0x4	R/W
0x05E	RX_EN_MODE_10	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD10	Receiver Mode 10 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD10	Receiver Mode 10 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD10	Receiver Mode 10 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD10	Receiver Mode 10 Channel 1 Enable	0x1	R/W
		2	CH2_EN_MD10	Receiver Mode 10 Channel 2 Enable	0x1	R/W
		1	CH3_EN_MD10	Receiver Mode 10 Channel 3 Enable	0x1	R/W
		0	CH4_EN_MD10	Receiver Mode 10 Channel 4 Enable	0x1	R/W
0x05F	RX_GAIN12_MODE_10	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD10	Receiver Mode 10 Channel 1 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD10	Receiver Mode 10 Channel 2 Gain	0x4	R/W
0x060	RX_GAIN34_MODE_10	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD10	Receiver Mode 10 Channel 3 Gain	0x4	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD10	Receiver Mode 10 Channel 4 Gain	0x4	R/W
0x061	RX_EN_MODE_11	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD11	Receiver Mode 11 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD11	Receiver Mode 11 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD11	Receiver Mode 11 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD11	Receiver Mode 11 Channel 1 Enable	0x1	R/W
		2	CH2_EN_MD11	Receiver Mode 11 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD11	Receiver Mode 11 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD11	Receiver Mode 11 Channel 4 Enable	0x0	R/W
0x062	RX_GAIN12_MODE_11	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD11	Receiver Mode 11 Channel 1 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD11	Receiver Mode 11 Channel 2 Gain	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x063	RX_GAIN34_MODE_11	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD11	Receiver Mode 11 Channel 3 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD11	Receiver Mode 11 Channel 4 Gain	0x0	R/W
0x064	RX_EN_MODE_12	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD12	Receiver Mode 12 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD12	Receiver Mode 12 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD12	Receiver Mode 12 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
		3	CH1_EN_MD12	Receiver Mode 12 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD12	Receiver Mode 12 Channel 2 Enable	0x1	R/W
		1	CH3_EN_MD12	Receiver Mode 12 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD12	Receiver Mode 12 Channel 4 Enable	0x0	R/W
0x065	RX_GAIN12_MODE_12	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD12	Receiver Mode 12 Channel 1 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD12	Receiver Mode 12 Channel 2 Gain	0x0	R/W
0x066	RX_GAIN34_MODE_12	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD12	Receiver Mode 12 Channel 3 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD12	Receiver Mode 12 Channel 4 Gain	0x0	R/W
0x067	RX_EN_MODE_13	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD13	Receiver Mode 13 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD13	Receiver Mode 13 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD13	Receiver Mode 13 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD13	Receiver Mode 13 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD13	Receiver Mode 13 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD13	Receiver Mode 13 Channel 3 Enable	0x1	R/W
		0	CH4_EN_MD13	Receiver Mode 13 Channel 4 Enable	0x0	R/W
0x068	RX_GAIN12_MODE_13	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD13	Receiver Mode 13 Channel 1 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD13	Receiver Mode 13 Channel 2 Gain	0x0	R/W
0x069	RX_GAIN34_MODE_13	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD13	Receiver Mode 13 Channel 3 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD13	Receiver Mode 13 Channel 4 Gain	0x0	R/W
0x06A	RX_EN_MODE_14	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD14	Receiver Mode 14 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD14	Receiver Mode 14 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		4	SPLT34_EN_MD14	Receiver Mode 14 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD14	Receiver Mode 14 Channel 1 Enable	0x0	R/W
		2	CH2_EN_MD14	Receiver Mode 14 Channel 2 Enable	0x0	R/W
		1	CH3_EN_MD14	Receiver Mode 14 Channel 3 Enable	0x0	R/W
		0	CH4_EN_MD14	Receiver Mode 14 Channel 4 Enable	0x1	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x06B	RX_GAIN12_MODE_14	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD14	Receiver Mode 14 Channel 1 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD14	Receiver Mode 14 Channel 2 Gain	0x0	R/W
0x06C	RX_GAIN34_MODE_14	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD14	Receiver Mode 14 Channel 3 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD14	Receiver Mode 14 Channel 4 Gain	0x0	R/W
0x06D	RX_EN_MODE_15	7	RESERVED	Reserved	0x0	R
		6	SPLT1_EN_MD15	Receiver Mode 15 Active Splitter 1 Enable	0x1	R/W
		5	SPLT12_EN_MD15	Receiver Mode 15 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		4	SPLT34_EN_MD15	Receiver Mode 15 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
		3	CH1_EN_MD15	Receiver Mode 15 Channel 1 Enable	0x1	R/W
		2	CH2_EN_MD15	Receiver Mode 15 Channel 2 Enable	0x1	R/W
		1	CH3_EN_MD15	Receiver Mode 15 Channel 3 Enable	0x1	R/W
		0	CH4_EN_MD15	Receiver Mode 15 Channel 4 Enable	0x1	R/W
0x06E	RX_GAIN12_MODE_15	7	RESERVED	Reserved	0x0	R
		[6:4]	CH1_GAIN_MD15	Receiver Mode 15 Channel 1 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH2_GAIN_MD15	Receiver Mode 15 Channel 2 Gain	0x0	R/W
0x06F	RX_GAIN34_MODE_15	7	RESERVED	Reserved	0x0	R
		[6:4]	CH3_GAIN_MD15	Receiver Mode 15 Channel 3 Gain	0x0	R/W
		3	RESERVED	Reserved	0x0	R
		[2:0]	CH4_GAIN_MD15	Receiver Mode 15 Channel 4 Gain	0x0	R/W
0x070	MULT_EN_MODE_0	7	BPF_MD0	Multiplier Mode 0 BPF Select	0x0	R/W
		6	LOAMP_EN_MD0	Multiplier Mode 0 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD0	Multiplier Mode 0 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD0	Multiplier Mode 0 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD0	Multiplier Mode 0 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD0	Multiplier Mode 0 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD0	Multiplier Mode 0 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD0	Multiplier Mode 0 High Band Active Enable	0x0	R/W
0x071	MULT_EN_MODE_1	7	BPF_MD1	Multiplier Mode 1 BPF Select	0x0	R/W
		6	LOAMP_EN_MD1	Multiplier Mode 1 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD1	Multiplier Mode 1 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD1	Multiplier Mode 1 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD1	Multiplier Mode 1 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD1	Multiplier Mode 1 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD1	Multiplier Mode 1 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD1	Multiplier Mode 1 High Band Active Enable	0x0	R/W
0x072	MULT_EN_MODE_2	7	BPF_MD2	Multiplier Mode 2 BPF Select	0x1	R/W
		6	LOAMP_EN_MD2	Multiplier Mode 2 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD2	Multiplier Mode 2 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD2	Multiplier Mode 2 Low Band Active Enable	0x1	R/W
		3	MULT_MID_RDY_MD2	Multiplier Mode 2 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD2	Multiplier Mode 2 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD2	Multiplier Mode 2 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD2	Multiplier Mode 2 High Band Active Enable	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x073	MULT_EN_MODE_3	7	BPF_MD3	Multiplier Mode 3 BPF Select	0x0	R/W
		6	LOAMP_EN_MD3	Multiplier Mode 3 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD3	Multiplier Mode 3 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD3	Multiplier Mode 3 Low Band Active Enable	0x1	R/W
		3	MULT_MID_RDY_MD3	Multiplier Mode 3 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD3	Multiplier Mode 3 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD3	Multiplier Mode 3 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD3	Multiplier Mode 3 High Band Active Enable	0x0	R/W
0x074	MULT_EN_MODE_4	7	BPF_MD4	Multiplier Mode 4 BPF Select	0x1	R/W
		6	LOAMP_EN_MD4	Multiplier Mode 4 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD4	Multiplier Mode 4 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD4	Multiplier Mode 4 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD4	Multiplier Mode 4 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD4	Multiplier Mode 4 Mid Band Active Enable	0x1	R/W
		1	MULT_HIGH_RDY_MD4	Multiplier Mode 4 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD4	Multiplier Mode 4 High Band Active Enable	0x0	R/W
0x075	MULT_EN_MODE_5	7	BPF_MD5	Multiplier Mode 5 BPF Select	0x0	R/W
		6	LOAMP_EN_MD5	Multiplier Mode 5 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD5	Multiplier Mode 5 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD5	Multiplier Mode 5 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD5	Multiplier Mode 5 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD5	Multiplier Mode 5 Mid Band Active Enable	0x1	R/W
		1	MULT_HIGH_RDY_MD5	Multiplier Mode 5 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD5	Multiplier Mode 5 High Band Active Enable	0x0	R/W
0x076	MULT_EN_MODE_6	7	BPF_MD6	Multiplier Mode 6 BPF Select	0x1	R/W
		6	LOAMP_EN_MD6	Multiplier Mode 6 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD6	Multiplier Mode 6 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD6	Multiplier Mode 6 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD6	Multiplier Mode 6 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD6	Multiplier Mode 6 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD6	Multiplier Mode 6 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD6	Multiplier Mode 6 High Band Active Enable	0x1	R/W
0x077	MULT_EN_MODE_7	7	BPF_MD7	Multiplier Mode 7 BPF Select	0x0	R/W
		6	LOAMP_EN_MD7	Multiplier Mode 7 LO Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD7	Multiplier Mode 7 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD7	Multiplier Mode 7 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD7	Multiplier Mode 7 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD7	Multiplier Mode 7 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD7	Multiplier Mode 7 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD7	Multiplier Mode 7 High Band Active Enable	0x1	R/W
0x078	MULT_EN_MODE_8	7	BPF_MD8	Multiplier Mode 8 BPF Select	0x0	R/W
		6	LOAMP_EN_MD8	Multiplier Mode 8 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD8	Multiplier Mode 8 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD8	Multiplier Mode 8 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD8	Multiplier Mode 8 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD8	Multiplier Mode 8 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD8	Multiplier Mode 8 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD8	Multiplier Mode 8 High Band Active Enable	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x079	MULT_EN_MODE_9	7	BPF_MD9	Multiplier Mode 9 BPF Select	0x0	R/W
		6	LOAMP_EN_MD9	Multiplier Mode 9 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD9	Multiplier Mode 9 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD9	Multiplier Mode 9 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD9	Multiplier Mode 9 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD9	Multiplier Mode 9 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD9	Multiplier Mode 9 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD9	Multiplier Mode 9 High Band Active Enable	0x0	R/W
0x07A	MULT_EN_MODE_10	7	BPF_MD10	Multiplier Mode 10 BPF Select	0x0	R/W
		6	LOAMP_EN_MD10	Multiplier Mode 10 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD10	Multiplier Mode 10 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD10	Multiplier Mode 10 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD10	Multiplier Mode 10 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD10	Multiplier Mode 10 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD10	Multiplier Mode 10 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD10	Multiplier Mode 10 High Band Active Enable	0x0	R/W
0x07B	MULT_EN_MODE_11	7	BPF_MD11	Multiplier Mode 11 BPF Select	0x0	R/W
		6	LOAMP_EN_MD11	Multiplier Mode 11 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD11	Multiplier Mode 11 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD11	Multiplier Mode 11 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD11	Multiplier Mode 11 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD11	Multiplier Mode 11 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD11	Multiplier Mode 11 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD11	Multiplier Mode 11 High Band Active Enable	0x0	R/W
0x07C	MULT_EN_MODE_12	7	BPF_MD12	Multiplier Mode 12 BPF Select	0x0	R/W
		6	LOAMP_EN_MD12	Multiplier Mode 12 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD12	Multiplier Mode 12 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD12	Multiplier Mode 12 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD12	Multiplier Mode 12 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD12	Multiplier Mode 12 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD12	Multiplier Mode 12 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD12	Multiplier Mode 12 High Band Active Enable	0x0	R/W
0x07D	MULT_EN_MODE_13	7	BPF_MD13	Multiplier Mode 13 BPF Select	0x0	R/W
		6	LOAMP_EN_MD13	Multiplier Mode 13 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD13	Multiplier Mode 13 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD13	Multiplier Mode 13 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD13	Multiplier Mode 13 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD13	Multiplier Mode 13 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD13	Multiplier Mode 13 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD13	Multiplier Mode 13 High Band Active Enable	0x0	R/W
0x07E	MULT_EN_MODE_14	7	BPF_MD14	Multiplier Mode 14 BPF Select	0x0	R/W
		6	LOAMP_EN_MD14	Multiplier Mode 14 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD14	Multiplier Mode 14 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD14	Multiplier Mode 14 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD14	Multiplier Mode 14 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD14	Multiplier Mode 14 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD14	Multiplier Mode 14 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD14	Multiplier Mode 14 High Band Active Enable	0x0	R/W

Address	Name	Bits	Bit Name	Description	Reset	Access
0x07F	MULT_EN_MODE_15	7	BPF_MD15	Multiplier Mode 15 BPF Select	0x0	R/W
		6	LOAMP_EN_MD15	Multiplier Mode 15 LO Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD15	Multiplier Mode 15 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD15	Multiplier Mode 15 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD15	Multiplier Mode 15 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD15	Multiplier Mode 15 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD15	Multiplier Mode 15 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD15	Multiplier Mode 15 High Band Active Enable	0x0	R/W
0x100	SCAN_MODE_EN	[7:1]	RESERVED	Reserved	0x0	R
		0	SCAN_MODE_EN	Scan Mode Enable	0x0	R/W

OUTLINE DIMENSIONS

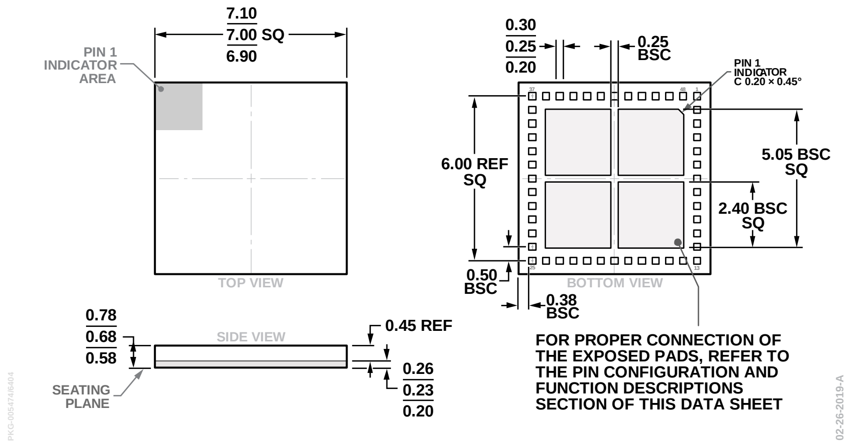


Figure 47. 48-Terminal Land Grid Array [LGA] Package
7 mm × 7 mm Body and 0.68 mm Package Height
(CC-48-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAR2004ACCZ	−40°C to +85°C	48-Terminal Land Grid Array [LGA], Tray	CC-48-2
ADAR2004ACCZ-R7	−40°C to +85°C	48-Terminal Land Grid Array [LGA], 7” Tape and Reel	CC-48-2
ADAR2004-EVALZ		Evaluation Board	

[1] Z = RoHS compliant part.